INTEGRATED CIRCUITS

DATA HANDBOOK

General-Purpose/ Linear ICs

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Preface

General Purpose/Linear ICs

Thank you for your interest in General Purpose/Linear IC products from Philips Semiconductors-Signetics. As a leading supplier to the electronics market, we offer a wide range of linear semiconductor components.

This General Purpose/Linear IC handbook includes information on the current range of General Purpose/Linear products from Philips Semiconductors-Signetics. The products are used in a wide range of consumer and industrial applications.

This book is one of many data books available from Philips Semiconductors-Signetics, each one covering a different range of product lines.

For a complete listing of available data books, please refer to the back of this book. For additional information regarding these or any of our other products, please contact your local Philips Semiconductors-Signetics sales office, also listed in the back of this book.

Product Status

General-Purpose/Linear ICs

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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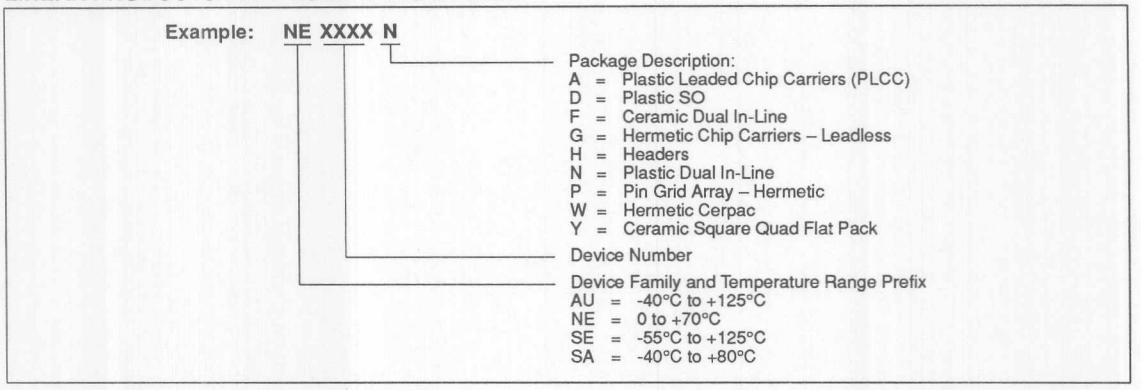
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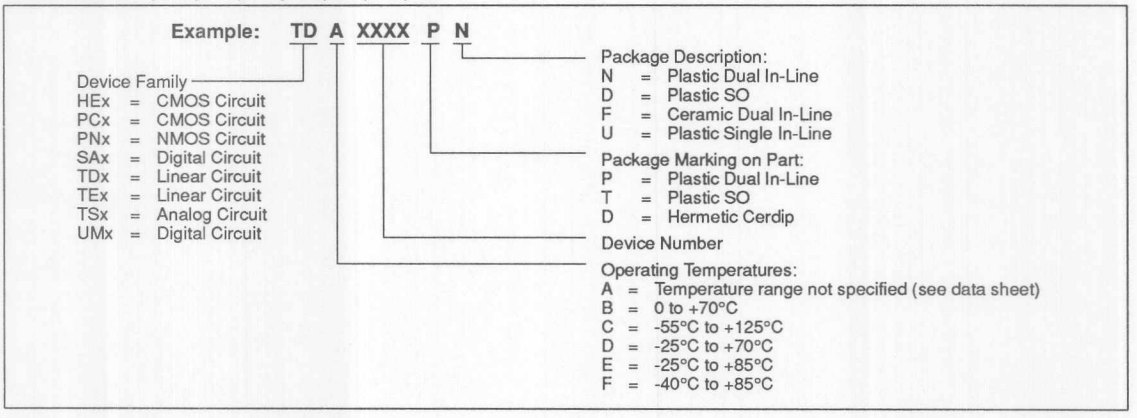
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Ordering Information

LINEAR PRODUCTS PART NUMBERING SYSTEM



PHILIPS PRODUCTS PART NUMBERING SYSTEM
PREFIXES HE, PC, PN, SA, TD, TE, TS, UM



PHILIPS PRODUCTS PART NUMBERING SYSTEM

PREFIXES HE, PC, PA, SA, TD, TE, TS, UA

LINEAR PRODUCTS PART NUMBERING SYSTEM

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Operational Amplifiers

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Section 1
Operational Amplifiers

Low power quad op amps

LM124/224/324/324A/ SA534/LM2902

DESCRIPTION

The LM124/SA534/LM2902 series consists of four independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

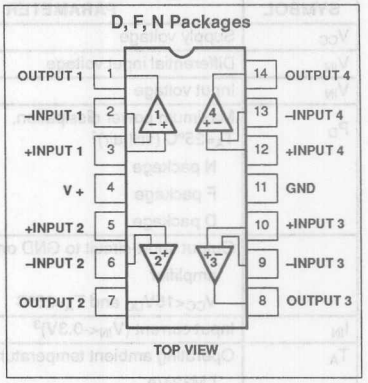
In the linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain crossover frequency and the input bias current are temperature-compensated.

FEATURES

- Internally frequency-compensated for unity gain
- Large DC voltage gain: 100dB
- Wide bandwidth (unity gain): 1MHz (temperature-compensated)
- Wide power supply range Single supply: $3V_{DC}$ to $30V_{DC}$ or dual supplies: $\pm1.5V_{DC}$ to $\pm15V_{DC}$
- Very low supply current drain: essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)
- Low input biasing current: $45nA_{DC}$ (temperature-compensated)
- Low input offset voltage: $2mV_{DC}$ and offset current: $5nA_{DC}$
- Differential input voltage range equal to the power supply voltage
- Large output voltage: $0V_{DC}$ to V_{CC}-$1.5V_{DC}$ swing

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	-55°C to +125°C	LM124N
14-Pin Ceramic DIP	-55°C to +125°C	LM124F
14-Pin Plastic DIP	-25°C to +85°C	LM224N
14-Pin Ceramic DIP	-25°C to +85°C	LM224F
14-Pin Plastic DIP	0°C to +70°C	LM324N
14-Pin Ceramic DIP	0°C to +70°C	LM324F
14-Pin Plastic SO	0°C to +70°C	LM324D
14-Pin Plastic DIP	0°C to +70°C	LM324AN
14-Pin Plastic SO	0°C to +70°C	LM324AD
14-Pin Plastic DIP	-40°C to +85°C	SA534N
14-Pin Ceramic DIP	-40°C to +85°C	SA534F
14-Pin Plastic SO	-40°C to +85°C	SA534D
14-Pin Plastic SO	-40°C to +85°C	LM2902D
14-Pin Plastic DIP	-40°C to +85°C	LM2902N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	32 or ±16	V_{DC}
V_{IN}	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	-0.3 to +32	V_{DC}
P_D	Maximum power dissipation, T_A=25°C (still-air)[1]		
	N package	1420	mW
	F package	1190	mW
	D package	1040	mW
	Output short-circuit to GND one amplifier V_{CC}<15V_{DC} and T_A=25°C	Continuous	
I_{IN}	Input current (V_{IN}<-0.3V)[3]	50	mA
T_A	Operating ambient temperature range		
	LM324/A	0 to +70	°C
	LM224	-25 to +85	°C
	SA534/LM2902	-40 to +85	°C
	LM124	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C
2. Short-circuits from the output to V_{CC}+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA, independent of the magnitude of V_{CC}. At values of supply voltage in excess of +15V_{DC} continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input bias clamps. In addition, there is also lateral NPN parasitic transistor action on the IC chip. This action can cause the output voltages of the op amps to go to the V+ rail (or to ground for a large overdrive) during the time that the input is driven negative.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=5V, T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM124/LM224			LM324/SA534/LM2902			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω		±2	±5		±2	±7	mV
		R_S=0Ω, over temp.			±7			±9	mV
$\Delta V_{OS}/\Delta T$	Temperature drift	R_S=0Ω, over temp.		7			7		µV/°C
I_{BIAS}	Input current[2]	I_{IN}(+) or I_{IN}(-)		45	150		45	250	nA
		I_{IN}(+) or I_{IN}(-), over temp.		40	300		40	500	nA
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50			50		pA/°C
I_{OS}	Offset current	I_{IN}(+)-I_{IN}(-)		±3	±30		±5	±50	nA
		I_{IN}(+)-I_{IN}(-), over temp.			±100			±150	nA
V_{OS}	Offset voltage[1]	R_S = 0Ω		±2	±5		±2	±7	mV
		R_S = 0Ω, over temp.			±7			±9	mV
$\Delta V_{OS}/\Delta T$	Temperature drift	R_S = 0Ω, over temp.		7			7		µV/°C
I_{BIAS}	Input current[2]	I_{IN} (+) or I_{IN} (–)		45	150		45	250	nA
		I_{IN} (+) or I_{IN} (–), over temp.		40	300		40	500	nA
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50			50		pA/°C
I_{OS}	Offset current	I_{IN} (+) – I_{IN} (–)		±3	±30		±5	±50	nA
		I_{IN} (+) – I_{IN} (–), over temp.			±100			±150	nA
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10			10		pA/°C
V_{CM}	Common-mode voltage range[3]	V_{CC}≤30V	0		V_{CC}-1.5	0		V_{CC}-1.5	V
		V_{CC}≤30V, over temp.	0		V_{CC}-2	0		V_{CC}-2	V
CMRR	Common-mode rejection ratio	V_{CC}=30V	70	85		65	70		dB
V_{OUT}	Output voltage swing	R_L=2kΩ, V_{CC}=30V, over temp.	26			26			V
V_{OH}	Output voltage high	R_L≤10kΩ, V_{CC}=30V, over temp.	27	28		27	28		V
V_{OL}	Output voltage low	R_L≤10kΩ, V_{CC}=5V, over temp.		5	20		5	20	mV
I_{CC}	Supply current	R_L=∞, V_{CC}=30V, over temp.		1.5	3		1.5	3	mA
		R_L=∞, V_{CC}=5V, over temp.		0.7	1.2		0.7	1.2	mA
A_{VOL}	Large-signal voltage gain	V_{CC}=15V (for large V_O swing), R_L≥2kΩ	50	100		25	100		V/mV
		V_{CC}=15V (for large V_O swing), R_L≥2kΩ, over temp.	25			15			V/mV
	Amplifier-to-amplifier coupling[5]	f=1kHz to 20kHz, input referred		-120			-120		dB
PSRR	Power supply rejection ratio	R_S≤0Ω	65	100		65	100		dB
I_{OUT}	Output current source	V_{IN}+=+1V, V_{IN}-=0V, V_{CC}=15V	20	40		20	40		mA
		V_{IN}+=+1V, V_{IN}-=0V, V_{CC}=15V, over temp.	10	20		10	20		mA
	sink	V_{IN}-=+1V, V_{IN}+=0V, V+=15V	10	20		10	20		mA
		V_{IN}-=+1V, V_{IN}+=0V, V_{CC}=15V, over temp.	5	8		5	8		mA
		V_{IN}-=+1V, V_{IN}+=0V, V_O=200mV	12	50		12	50		µA
I_{SC}	Short-circuit current[4]		10	40	60	10	40	60	mA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LM124/LM224			LM324/SA534/LM2902			UNIT
			Min	Typ	Max	Min	Typ	Max	
GBW	Unity gain bandwidth			1			1		MHz
SR	Slew rate			0.3			0.3		V/μs
V_{NOISE}	Input noise voltage	f=1kHz		40			40		nV/√Hz
V_{DIFF}	Differential input voltage[3]				V_{CC}			V_{CC}	V

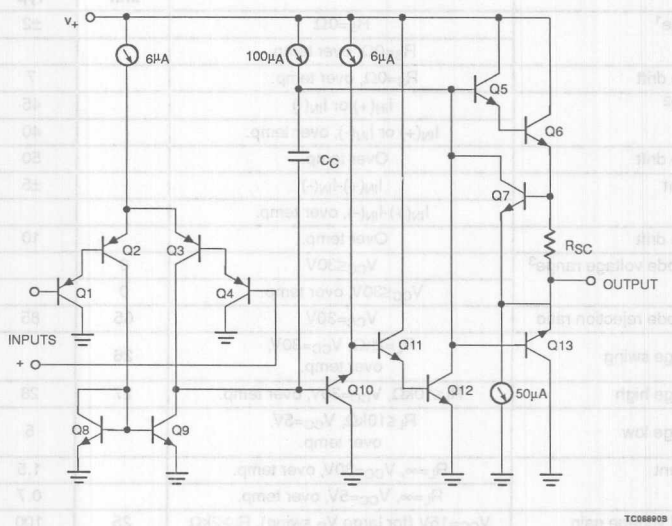
DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LM324A			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω		±2	±3	mV
		R_S=0Ω, over temp.			±5	mV
$\Delta V_{OS}/\Delta T$	Temperature drift	R_S=0Ω, over temp.		7	30	µV/°C
I_{BIAS}	Input current[2]	I_{IN}(+) or I_{IN}(-)		45	100	nA
		I_{IN}(+) or I_{IN}(-), over temp.		40	200	nA
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50		pA/°C
I_{OS}	Offset current	I_{IN}(+)-I_{IN}(-)		±5	±30	nA
		I_{IN}(+)-I_{IN}(-), over temp.			±75	nA
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10	300	pA/°C
V_{CM}	Common-mode voltage range[3]	V_{CC}≤30V	0		V_{CC}-1.5	V
		V_{CC}≤30V, over temp.	0		V_{CC}-2	V
CMRR	Common-mode rejection ratio	V_{CC}=30V	65	85		dB
V_{OUT}	Output voltage swing	R_L=2kΩ, V_{CC}=30V, over temp.	26			V
V_{OH}	Output voltage high	R_L≤10kΩ, V_{CC}=30V, over temp.	27	28		V
V_{OL}	Output voltage low	R_L≤10kΩ, V_{CC}=5V, over temp.		5	20	mV
I_{CC}	Supply current	R_L=∞, V_{CC}=30V, over temp.		1.5	3	mA
		R_L=∞, V_{CC}=5V, over temp.		0.7	1.2	mA
A_{VOL}	Large-signal voltage gain	V_{CC}=15V (for large V_O swing), R_L≥2kΩ	25	100		V/mV
		V_{CC}=15V (for large V_O swing), R_L≥2kΩ, over temp.	15			V/mV
	Amplifier-to-amplifier coupling[5]	f=1kHz to 20kHz, input referred		-120		dB
PSRR	Power supply rejection ratio	R_S≤0Ω	65	100		dB
I_{OUT}	Output current source	V_{IN}+=+1V, V_{IN}-=0V, V_{CC}=15V	20	40		mA
		V_{IN}+=+1V, V_{IN}-=0V, V_{CC}=15V, over temp.	10	20		mA
	sink	V_{IN}-=+1V, V_{IN}+=0V, V+=15V	10	20		mA
		V_{IN}-=+1V, V_{IN}+=0V, V_{CC}=15V, over temp.	5	8		mA
		V_{IN}-=+1V, V_{IN}+=0V, V_O=200mV	12	50		µA
I_{SC}	Short-circuit current[4]		10	40	60	mA
V_{DIFF}	Differential input voltage[3]				V_{CC}	V
GBW	Unity gain bandwidth			1		MHz
SR	Slew rate			0.3		V/µs
V_{NOISE}	Input noise voltage	f=1kHz		40		nV/√Hz

NOTES:

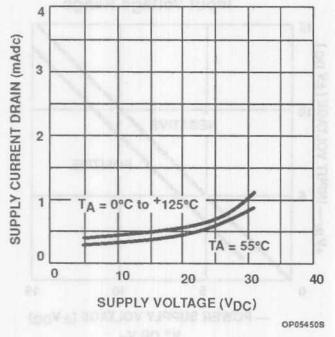
1. $V_O \approx 1.4V_{DC}$, R_S=0Ω with V_{CC} from 5V to 30V and over full input common-mode range ($0V_{DC}$+ to V_{CC} -1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC} -1.5, but either or both inputs can go to +32V without damage.
4. Short-circuits from the output to V_{CC} can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of coupling increases at higher frequencies.

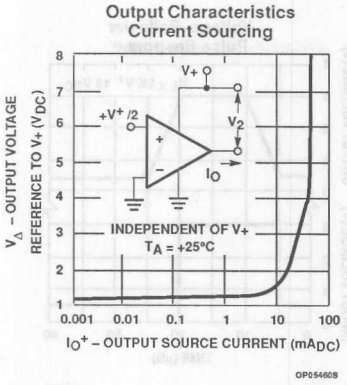
EQUIVALENT CIRCUIT

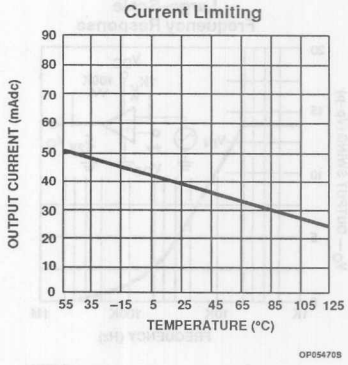


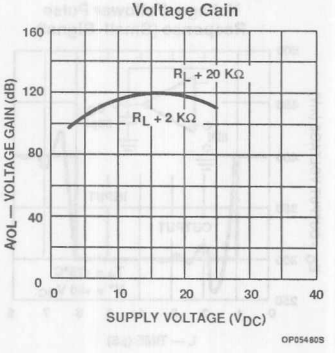
EQUIVALENT SCHEMATIC

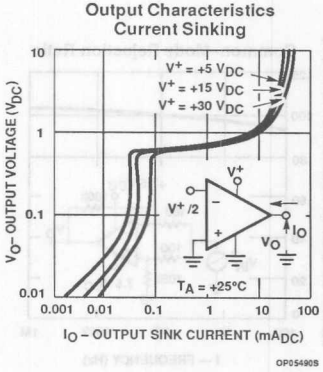
TYPICAL PERFORMANCE CHARACTERISTICS

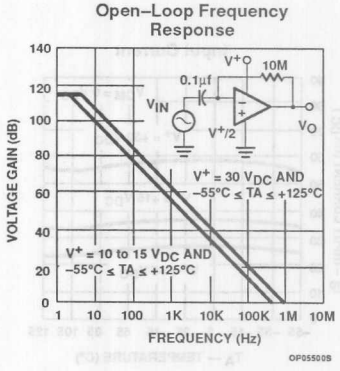






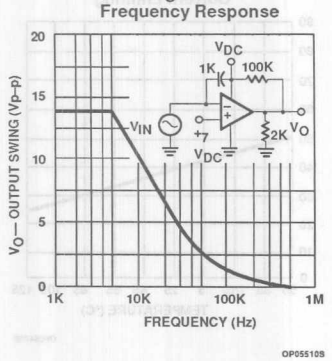




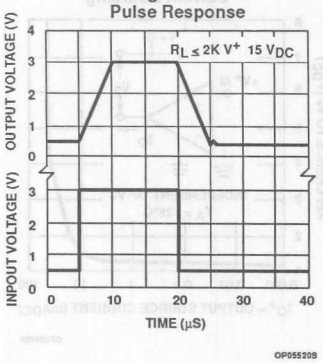


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

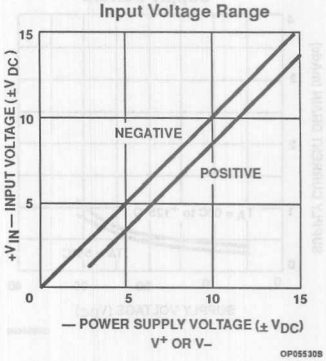
Large–Scale Frequency Response



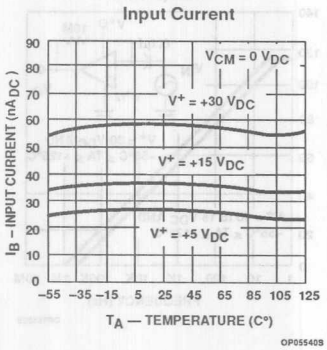
Voltage–Follower Pulse Response



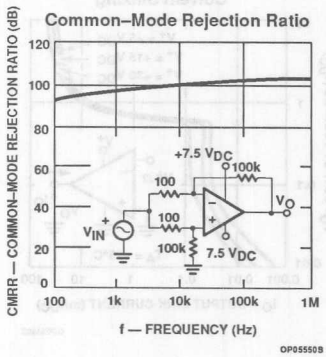
Input Voltage Range



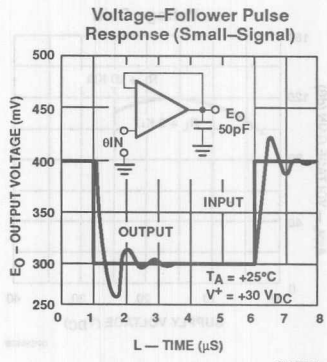
Input Current



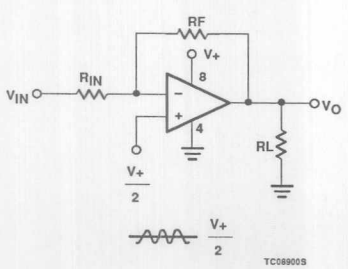
Common–Mode Rejection Ratio



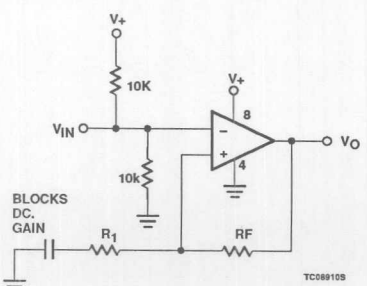
Voltage–Follower Pulse Response (Small–Signal)



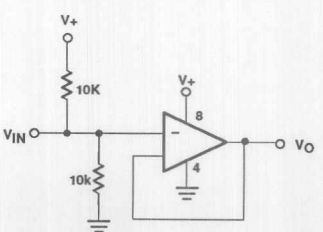
TYPICAL APPLICATIONS



Single Supply Inverting Amplifier



Non–Inverting Amplifier



Input Biasing Voltage–Follower

Low power quad operational amplifier AU2902

DESCRIPTION

The AU2902 consists of four independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

In the linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

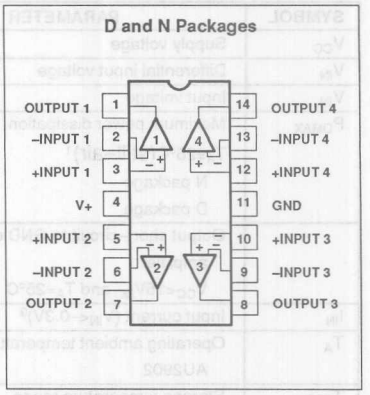
The unity gain crossover frequency and the input bias current are temperature-compensated.

FEATURES

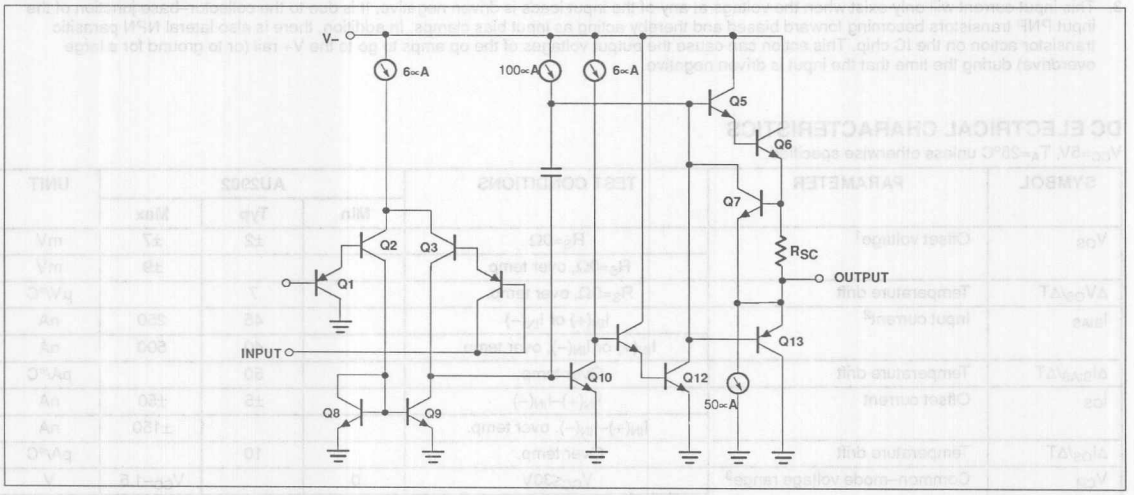
- Internally frequency-compensated for unity gain
- Large DC voltage gain: 100dB
- Wide bandwidth (unity gain): 1MHz (temperature-compensated)
- Wide power supply range Single supply: $3V_{DC}$ to $30V_{DC}$ or dual supplies: $\pm1.5V_{DC}$ to $\pm15V_{DC}$
- Very low supply current drain: essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)
- Low input bias current: $45nA_{DC}$ (temperature-compensated)
- Low input offset voltage: $2mV_{DC}$ and offset current: $5nA_{DC}$
- Differential input voltage range equal to the power supply voltage
- Large output voltage: $0V_{DC}$ to V_{CC}-$1.5V_{DC}$ swing

PIN CONFIGURATION

D and N Packages



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	32 or ±16	V_{DC}
V_{IN}	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	–0.3 to +32	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A=25°C(still–air)[1]		
	N package	1420	mW
	D package	1040	mW
	Output short–circuit to GND one amplifier V_{CC}<15V_{DC} and T_A=25°C	Continuous	
I_{IN}	Input current (V_{IN}<–0.3V)[3]	50	mA
T_A	Operating ambient temperature range AU2902	–40 to +125	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C at the following rates:
   N package at 11.4mW/°C
   D package at 8.3mW/°C
2. Short–circuits from the output to V_{CC}+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA, independent of the magnitude of V_{CC}. At values of supply voltage in excess of +15V_{DC} continuous short–circuits can exceed the power dissipation ratings and cause eventual destruction.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector–base junction of the input PNP transistors becoming forward biased and thereby acting as input bias clamps. In addition, there is also lateral NPN parasitic transistor action on the IC chip. This action can cause the output voltages of the op amps to go to the V+ rail (or to ground for a large overdrive) during the time that the input is driven negative.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=5V, T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	AU2902			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω		±2	±7	mV
		R_S=0Ω, over temp.			±9	mV
$\Delta V_{OS}/\Delta T$	Temperature drift	R_S=0Ω, over temp.		7		µV/°C
I_{BIAS}	Input current[2]	I_{IN}(+) or I_{IN}(–)		45	250	nA
		I_{IN}(+) or I_{IN}(–), over temp.		40	500	nA
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50		pA/°C
I_{OS}	Offset current	I_{IN}(+)–I_{IN}(–)		±5	±50	nA
		I_{IN}(+)–I_{IN}(–), over temp.			±150	nA
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10		pA/°C
V_{CM}	Common–mode voltage range[3]	V_{CC}≤30V	0		V_{CC}–1.5	V
		V_{CC}≤30V, over temp.	0		V_{CC}–2	V
CMRR	Common–mode rejection ratio	V_{CC}=30V	65	70		dB
V_{OUT}	Output voltage swing	R_L=2kΩ, V_{CC}=30V, over temp.	26			V
V_{OH}	Output voltage high	R_L≥10kΩ, V_{CC}=30V, over temp.	27	28		V
V_{OL}	Output voltage low	R_L≤10kΩ, V_{CC}=5V, over temp.		5	20	mV

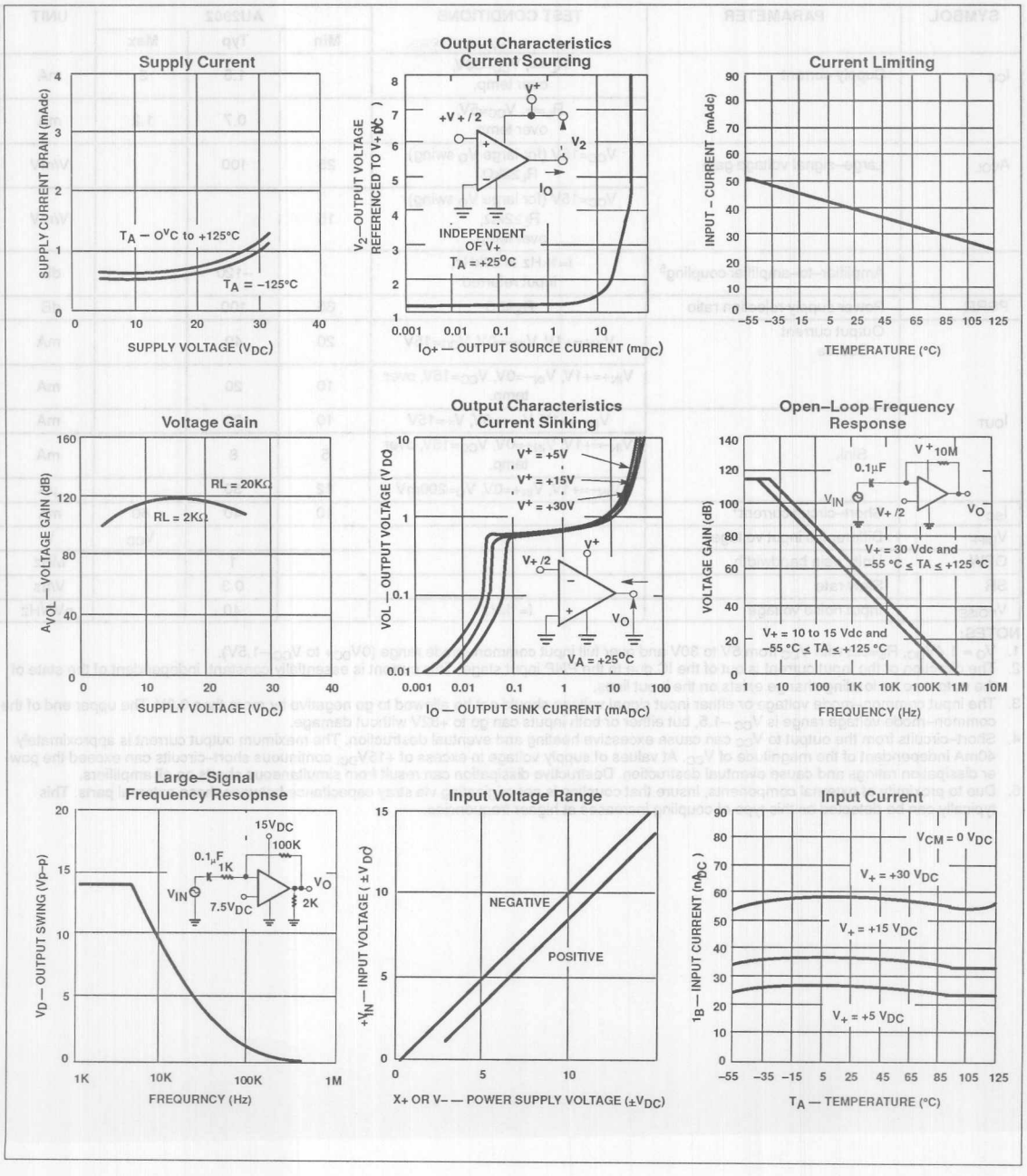
DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	AU2902			UNIT
			Min	Typ	Max	
I_{CC}	Supply current	R_L=∞, V_{CC}=30V, over temp.		1.5	3	mA
		R_L=∞, V_{CC}=5V, over temp.		0.7	1.2	mA
A_{VOL}	Large–signal voltage gain	V_{CC}=15V (for large V_O swing), R_L≥2kΩ	25	100		V/mV
		V_{CC}=15V (for large V_O swing), R_L≥2kΩ, over temp.	15			V/mV
	Amplifier–to–amplifier coupling[5]	f=1kHz to 20kHz, input referred		–120		dB
PSRR	Power supply rejection ratio	R_S=0Ω	65	100		dB
I_{OUT}	Output current Source	V_{IN}+=+1V, V_{IN}–=0V, V_{CC}=15V	20	40		mA
		V_{IN}+=+1V, V_{IN}–=0V, V_{CC}=15V, over temp.	10	20		mA
	Sink	V_{IN}–=+1V, V_{IN}+=0V, V+=15V	10	20		mA
		V_{IN}–=+1V, V_{IN}+=0V, V_{CC}=15V, over temp.	5	8		mA
		V_{IN}–=+1V, V_{IN}+=0V, V_O=200mV	12	50		µA
I_{SC}	Short–circuit current[4]		10	40	60	mA
V_{DIFF}	Differential input voltage[3]				V_{CC}	V
GBW	Unity gain bandwidth			1		MHz
SR	Slew rate			0.3		V/µs
V_{NOISE}	Input noise voltage	f=1kHz		40		nV/√Hz

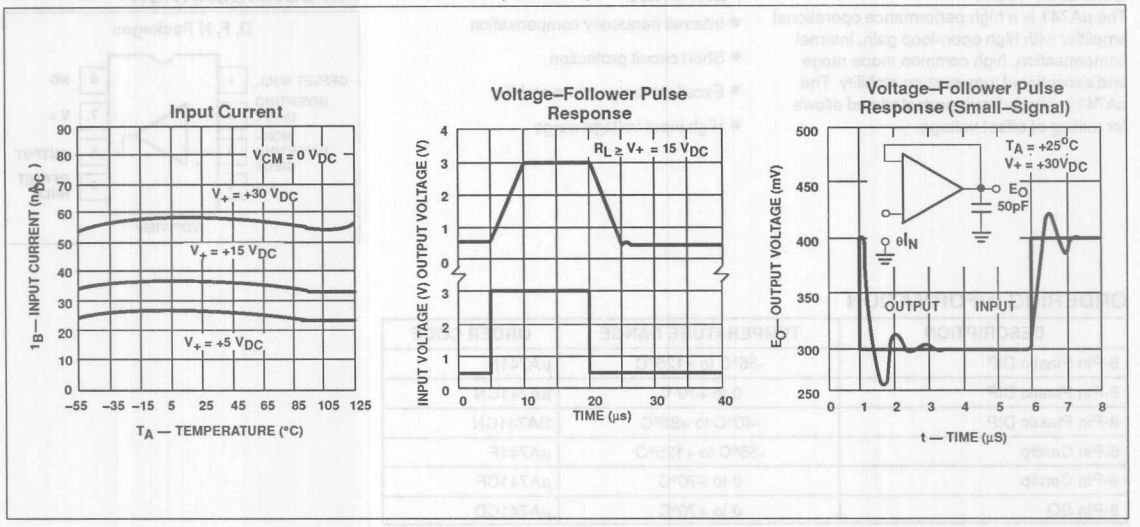
NOTES:

1. V_O ≈ 1.4V_{DC}, R_S=0Ω with V_{CC} from 5V to 30V and over full input common–mode range (0V_{DC}+ to V_{CC} –1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common–mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common–mode voltage range is V_{CC} –1.5, but either or both inputs can go to +32V without damage.
4. Short–circuits from the output to V_{CC} can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. At values of supply voltage in excess of +15V_{DC}, continuous short–circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of coupling increases at higher frequencies.

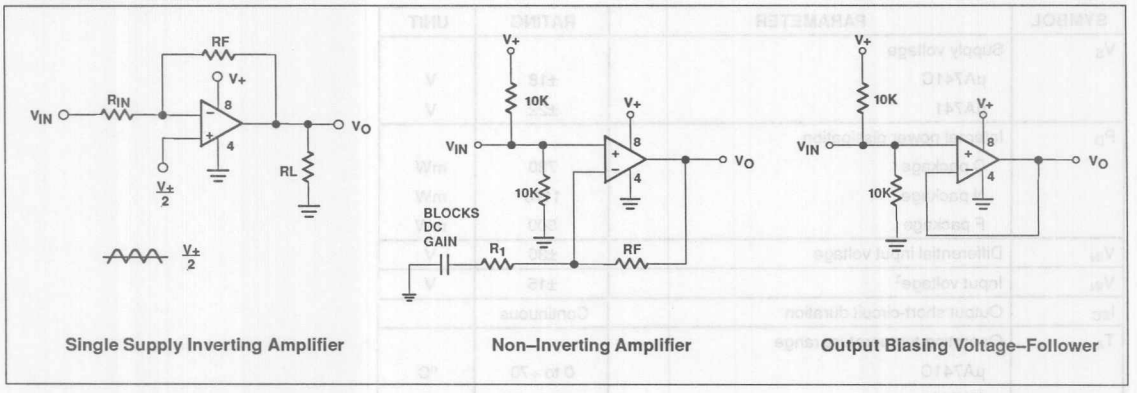
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TYPICAL APPLICATIONS



General purpose operational amplifier μA741/μA741C/SA741C

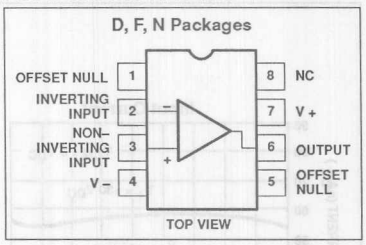
DESCRIPTION

The μA741 is a high performance operational amplifier with high open-loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit-protected and allows for nulling of offset voltage.

FEATURES

- Internal frequency compensation
- Short circuit protection
- Excellent temperature stability
- High input voltage range

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	-55°C to +125°C	μA741N
8-Pin Plastic DIP	0 to +70°C	μA741CN
8-Pin Plastic DIP	-40°C to +85°C	SA741CN
8-Pin Cerdip	-55°C to +125°C	μA741F
8-Pin Cerdip	0 to +70°C	μA741CF
8-Pin SO	0 to +70°C	μA741CD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage		
	μA741C	±18	V
	μA741	±22	V
P_D	Internal power dissipation		
	D package	780	mW
	N package	1170	mW
	F package	800	mW
V_{IN}	Differential input voltage	±30	V
V_{IN}	Input voltage[1]	±15	V
I_{SC}	Output short-circuit duration	Continuous	
T_A	Operating temperature range		
	μA741C	0 to +70	°C
	SA741C	-40 to +85	°C
	μA741	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

DC ELECTRICAL CHARACTERISTICS

(μA741, μA741C) T_A = 25°C, V_S = ±15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	μA741			μA741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	R_S=10kΩ		1.0	5.0		2.0	6.0	mV
		R_S=10kΩ, over temp.		1.0	6.0			7.5	mV
$\Delta V_{OS}/\Delta T$				10			10		μV/°C
I_{OS}	Offset current			20	200		20	200	nA
		Over temp.						300	nA
		T_A=+125°C		7.0	200				nA
		T_A=-55°C		20	500				nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temp.						800	nA
		T_A=+125°C		30	500				nA
		T_A=-55°C		300	1500				nA
$\Delta I_B/\Delta T$				1			1		nA/°C
V_{OUT}	Output voltage swing	R_L=10kΩ	±12	±14		±12	±14		V
		R_L=2kΩ, over temp.	±10	±13		±10	±13		V
A_{VOL}	Large-signal voltage gain	R_L=2kΩ, V_O=±10V	50	200		20	200		V/mV
		R_L=2kΩ, V_O=±10V, over temp.	25			15			V/mV
	Offset voltage adjustment range			±30			±30		mV
PSRR	Supply voltage rejection ratio	R_S≤10kΩ					10	150	μV/V
		R_S≤10kΩ, over temp.		10	150				μV/V
CMRR	Common-mode rejection ratio					70	90		dB
		Over temp.	70	90					dB
I_{CC}	Supply current			1.4	2.8		1.4	2.8	mA
		T_A=+125°C		1.5	2.5				mA
		T_A=-55°C		2.0	3.3				mA
V_{IN}	Input voltage range	(μA741, over temp.)	±12	±13		±12	±13		V
R_{IN}	Input resistance		0.3	2.0		0.3	2.0		MΩ
P_D	Power consumption			50	85		50	85	mW
		T_A=+125°C		45	75				mW
		T_A=-55°C		45	100				mW
R_{OUT}	Output resistance			75			75		Ω
I_{SC}	Output short-circuit current		10	25	60	10	25	60	mA

DC ELECTRICAL CHARACTERISTICS

(SA741C)T_A = 25°C, V_S = ±15V, unless otherwise specified.

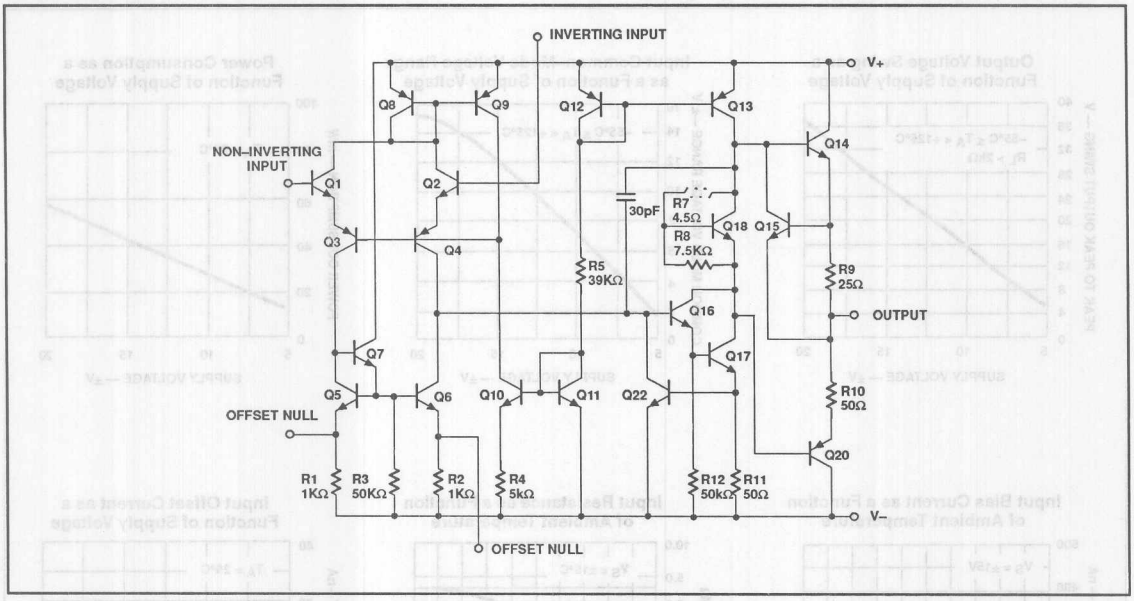
SYMBOL	PARAMETER	TEST CONDITIONS	SA741C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	R_S=10kΩ		2.0	6.0	mV
		R_S=10kΩ, over temp.			7.5	mV
$\Delta V_{OS}/\Delta T$				10		μV/°C
I_{OS}	Offset current			20	200	nA
		Over temp.			500	nA
$\Delta I_{OS}/\Delta T$				200		pA/°C
I_{BIAS}	Input bias current			80	500	nA
		Over temp.			1500	nA
$\Delta I_B/\Delta T$				1		nA/°C
V_{OUT}	Output voltage swing	R_L=10kΩ	±12	±14		V
		R_L=2kΩ, over temp.	±10	±13		V
A_{VOL}	Large-signal voltage gain	R_L=2kΩ, V_O=±10V	20	200		V/mV
		R_L=2kΩ, V_O=±10V, over temp.	15			V/mV
	Offset voltage adjustment range			±30		mV
PSRR	Supply voltage rejection ratio	R_S≤10kΩ		10	150	μV/V
CMRR	Common mode rejection ration		70	90		dB
V_{IN}	Input voltage range	Over temp.	±12	±13		V
R_{IN}	Input resistance		0.3	2.0		MΩ
P_d	Power consumption			50	85	mW
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current			25		mA

AC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_S = ±15V, unless otherwise specified.

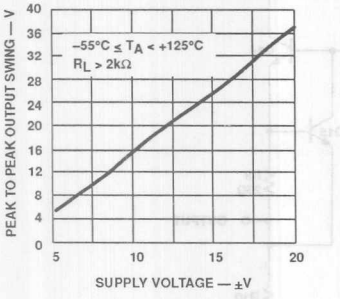
SYMBOL	PARAMETER	TEST CONDITIONS	μA741, μA741C			UNIT
			Min	Typ	Max	
R_{IN}	Parallel input resistance	Open-loop, f=20Hz	0.3			MΩ
C_{IN}	Parallel input capacitance	Open-loop, f=20Hz		1.4		pF
	Unity gain crossover frequency	Open-loop		1.0		MHz
	Transient response unity gain	V_{IN}=20mV, R_L=2kΩ, C_L≤100pF				
t_R	Rise time			0.3		μs
	Overshoot			5.0		%
SR	Slew rate	C≤100pF, R_L≥2kΩ, V_{IN}=±10V		0.5		V/μs

EQUIVALENT SCHEMATIC

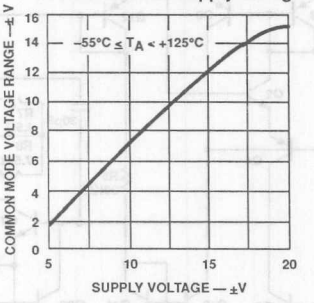


TYPICAL PERFORMANCE CHARACTERISTICS

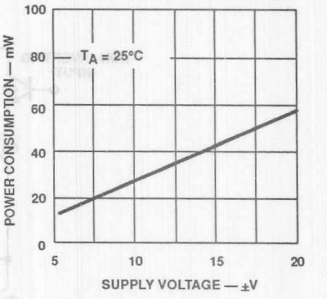
Output Voltage Swing as a Function of Supply Voltage



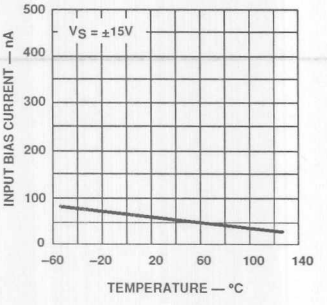
Input Common–Mode Voltage Range as a Function of Supply Voltage



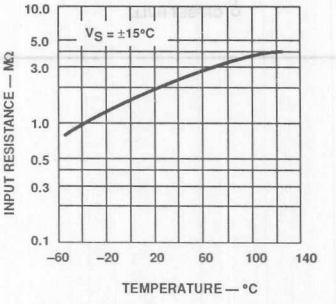
Power Consumption as a Function of Supply Voltage



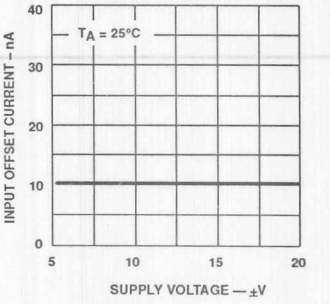
Input Bias Current as a Function of Ambient Temperature



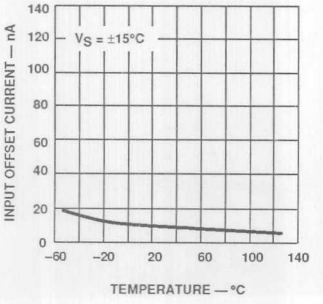
Input Resistance as a Function of Ambient Temperature



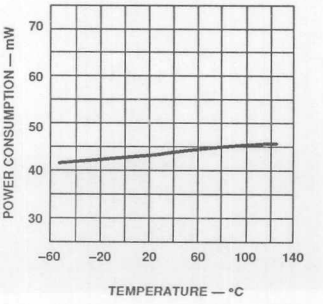
Input Offset Current as a Function of Supply Voltage



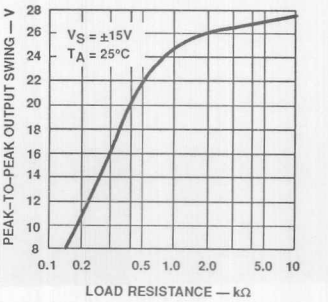
Input Offset Current as a Function of Ambient Temperature



Power Consumption as a Function of Ambient Temperature

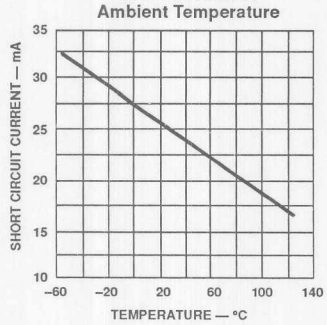


Output Voltage Swing as a Function of Load Resistance

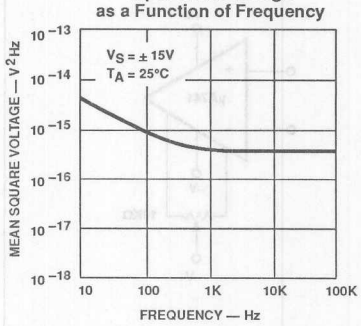


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

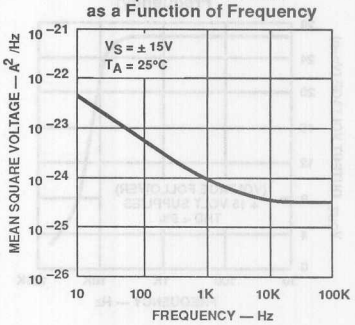
Output Short–Circuit Current as a Function of Ambient Temperature



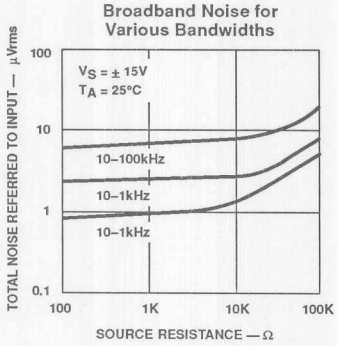
Input Noise Voltage as a Function of Frequency



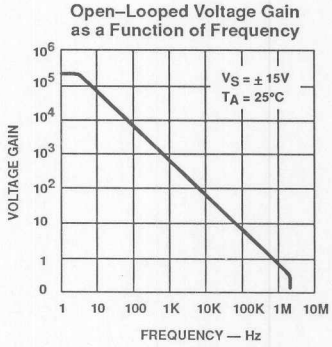
Input Noise Current as a Function of Frequency



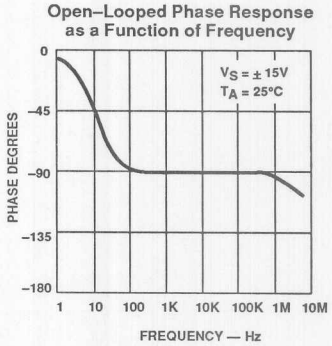
Broadband Noise for Various Bandwidths



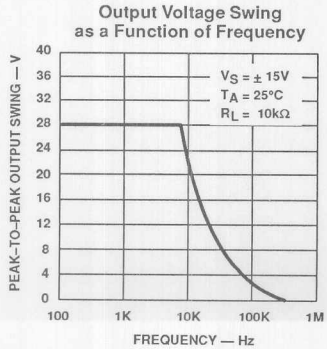
Open–Looped Voltage Gain as a Function of Frequency



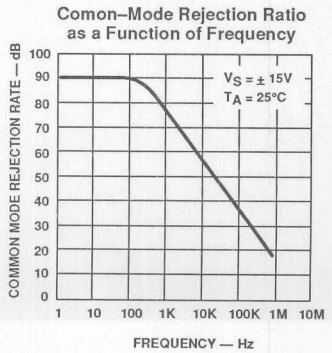
Open–Looped Phase Response as a Function of Frequency



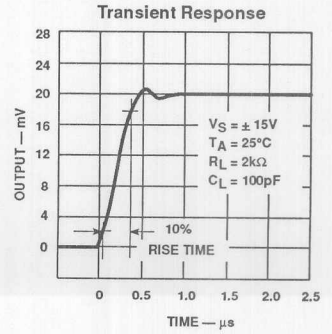
Output Voltage Swing as a Function of Frequency



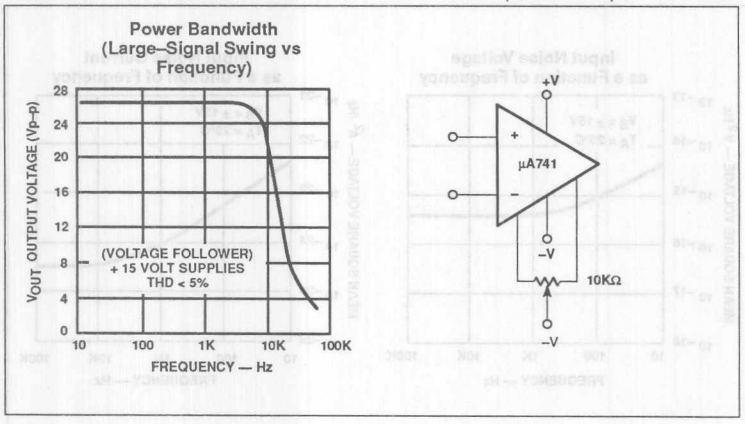
Comon–Mode Rejection Ratio as a Function of Frequency



Transient Response



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Dual operational amplifier — μA747C

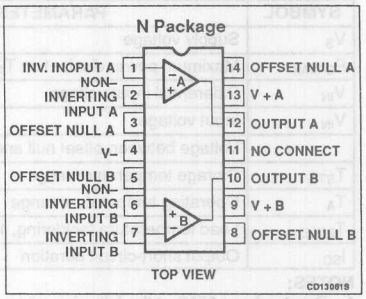
DESCRIPTION

The 747 is a pair of high-performance monolithic operational amplifiers constructed on a single silicon chip. High common-mode voltage range and absence of "latch-up" make the 747 ideal for use as a voltage-follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The 747 is short-circuit protected and requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed-loop applications. For single amplifier performance, see μA741 data sheet.

FEATURES

- No frequency compensation required
- Short-circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch-up

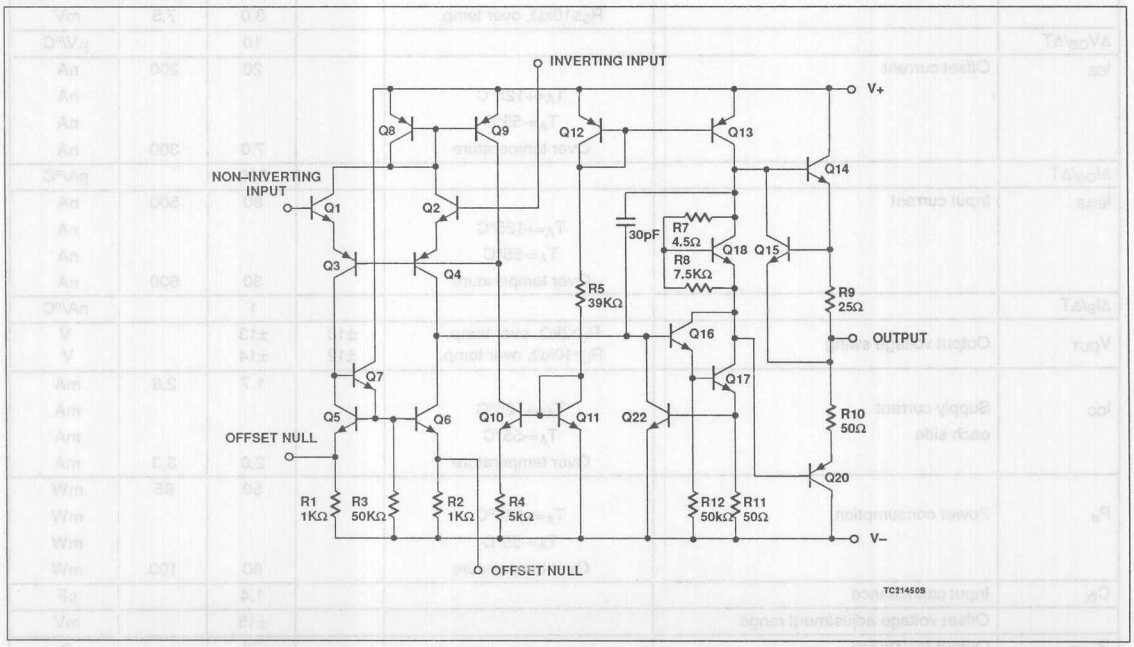
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0°C to 70°C	μA747CN

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±18	V
$P_{D\ MAX}$	Maximum power dissipation T_A=25°C (still air)[1]	1500	mW
V_{IN}	Differential input voltage	±30	V
V_{IN}	Input voltage[2]	±15	V
	Voltage between offset null and V-	±0.5	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating temperature range	0 to +70	°C
T_{SOLD}	Lead temperature (soldering, 10sec)	300	°C
I_{SC}	Output short-circuit duration	Indefinite	

NOTES:
1. Derate above 25°C at the following rates:
   N package at 12mW/°C
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC} = ±15V unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	μA747C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	R_S≤10kΩ		2.0	6.0	mV
		R_S≤10kΩ, over temp.		3.0	7.5	mV
$\Delta V_{OS}/\Delta T$				10		μV/°C
I_{OS}	Offset current			20	200	nA
		T_A=+125°C				nA
		T_A=-55°C				nA
		Over temperature		7.0	300	nA
$\Delta I_{OS}/\Delta T$				200		pA/°C
I_{BIAS}	Input current			80	500	nA
		T_A=+125°C				nA
		T_A=-55°C				nA
		Over temperature		30	800	nA
$\Delta I_B/\Delta T$				1		nA/°C
V_{OUT}	Output voltage swing	R_L≥2kΩ, over temp.	±10	±13		V
		R_L≥10kΩ, over temp.	±12	±14		V
I_{CC}	Supply current each side			1.7	2.8	mA
		T_A=+125°C				mA
		T_A=-55°C				mA
		Over temperature		2.0	3.3	mA
P_d	Power consumption			50	85	mW
		T_A=+125°C				mW
		T_A=-55°C				mW
		Over temperature		60	100	mW
C_{IN}	Input capacitance			1.4		pF
	Offset voltage adjustment range			±15		mV
R_{OUT}	Output resistance			75		Ω
	Channel separation			120		dB
PSRR	Supply voltage rejection ratio	R_S≤10kΩ, over temp.		30	150	μV/V
A_{VOL}	*Large-signal voltage gain (DC)*	R_L≥2kΩ, V_{OUT}=±10V	25,000			V/V
		Over temperature	15,000			V/V
CMRR	Common-mode rejection ratio	R_S≤10kΩ, V_{CM}=±12V Over temperature	70			dB

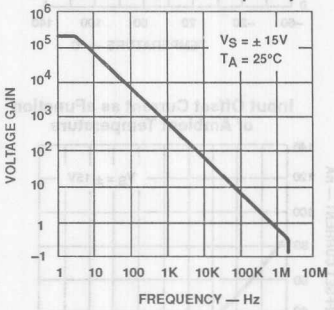
AC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_S = ±15V unless otherwise specified.

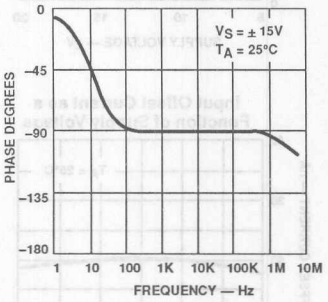
SYMBOL	PARAMETER	TEST CONDITIONS	μA747C			UNIT
			Min	Typ	Max	
t_R	Transient response	V_{IN}=20mV, R_L=2kΩ, C_L<100pF				
	Rise time	Unity gain C_L≤100pF		0.3		μs
	Overshoot	Unity gain C_L≤100pF		5.0		%
SR	Slew rate	R_L>2kΩ		0.5		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

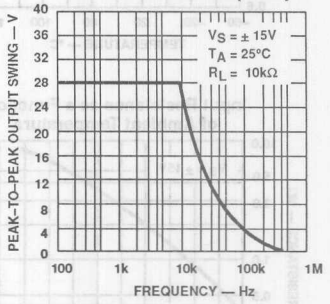
Open–Looped Voltage Gain as a Function of Frequency



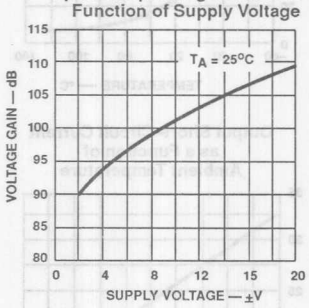
Open–Looped Voltage Response as a Function of Frequency



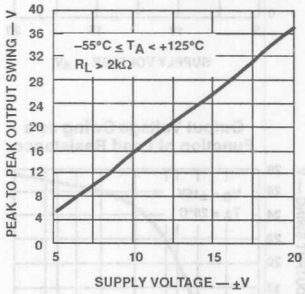
Output Voltage Swing as a Function of Frequency



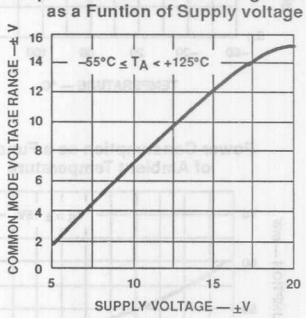
Open–Loop Voltage Gain as a Function of Supply Voltage



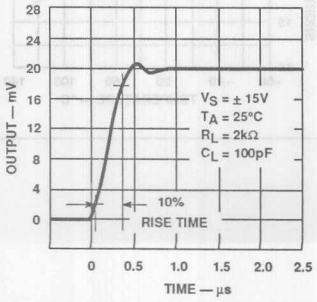
Output Voltage Swing as a Function of Supply Voltage



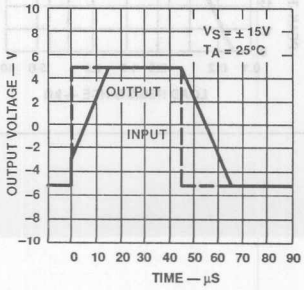
Input Common–Mode Voltage Range as a Funtion of Supply voltage



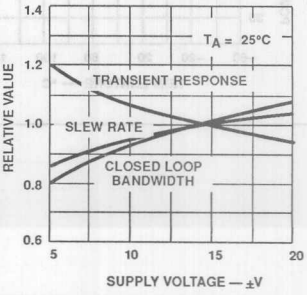
Transient Response



Voltage–follower Large–Signal Pulse Response

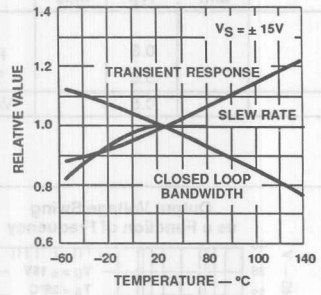


Frequency Characteristics as a Function of Supply Voltage

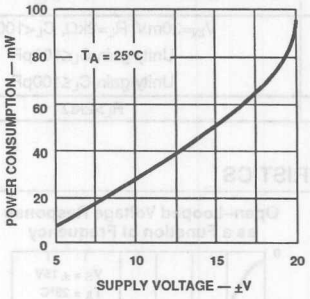


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

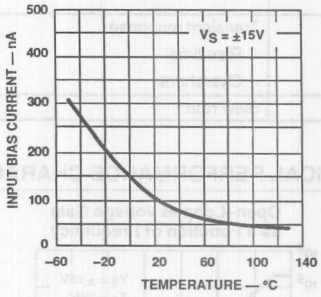
Frequency Characteristics as a Function of Ambient Temperature



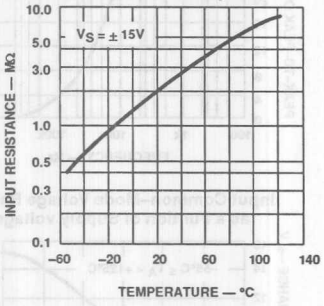
Power Consumption as a Function of Supply Voltage



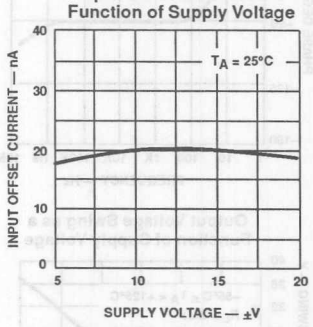
Input Bias Current as a Function of Ambient Temperature



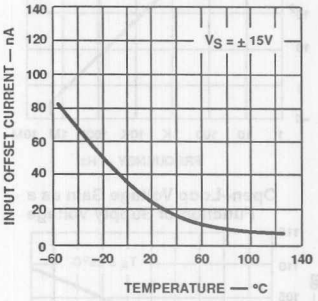
Input Resistance as a Function of Ambient Temperature



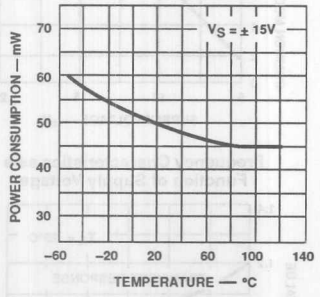
Input Offset Current as a Function of Supply Voltage



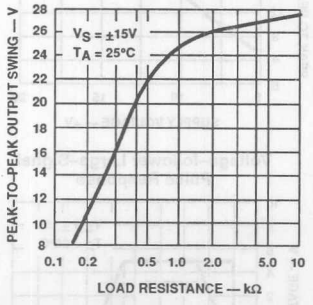
Input Offset Current as aFunction of Ambient Temperature



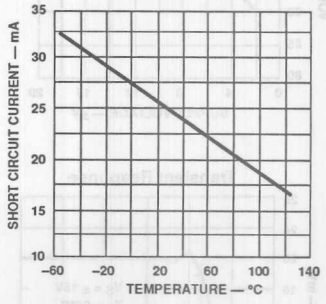
Power Consumption as a Function of Ambient Temperature



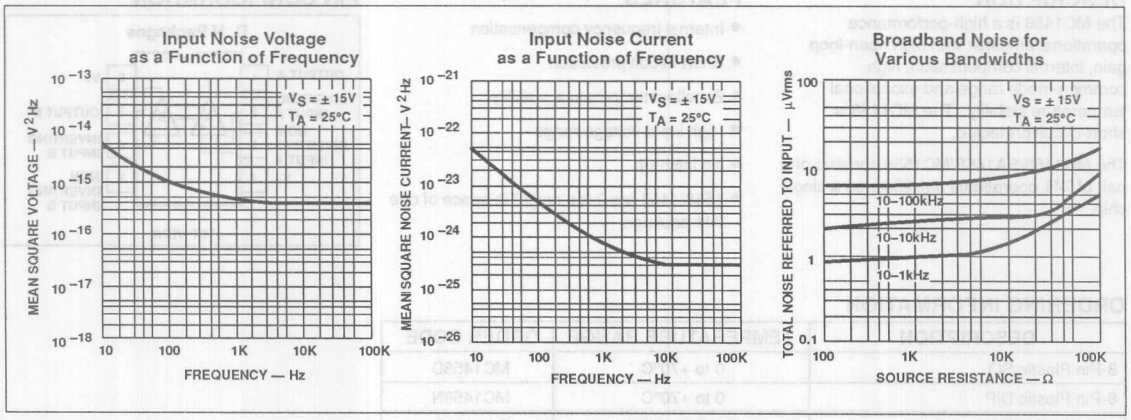
Output Voltage Swing as a Function of Load Resistance



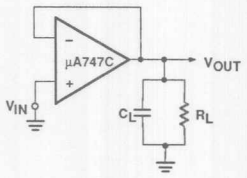
Output Short–Circuit Current as a Function of Ambient Temperature



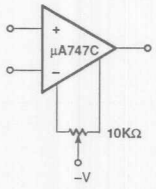
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TEST CIRCUITS



Transient Response Test Circuit



Voltage Offset Null Circuit

General purpose operational amplifier — MC/SA1458/MC1558

DESCRIPTION

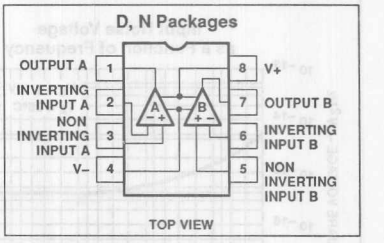
The MC1458 is a high-performance operational amplifier with high open-loop gain, internal compensation, high common-mode range and exceptional temperature stability. The MC1458 is short-circuit protected.

The MC1458/SA1458/MC1558 consists of a pair of 741 operational amplifiers on a single chip.

FEATURES

- Internal frequency compensation
- Short-circuit protection
- Excellent temperature stability
- High input voltage range
- No latch-up
- 1558/1458 are 2 "op amps" in space of one 741 package

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	MC1458D
8-Pin Plastic DIP	0 to +70°C	MC1458N
8-Pin Plastic SO	-40°C to +85°C	SA1458D
8-Pin Plastic DIP	-55°C to +125°C	MC1558N

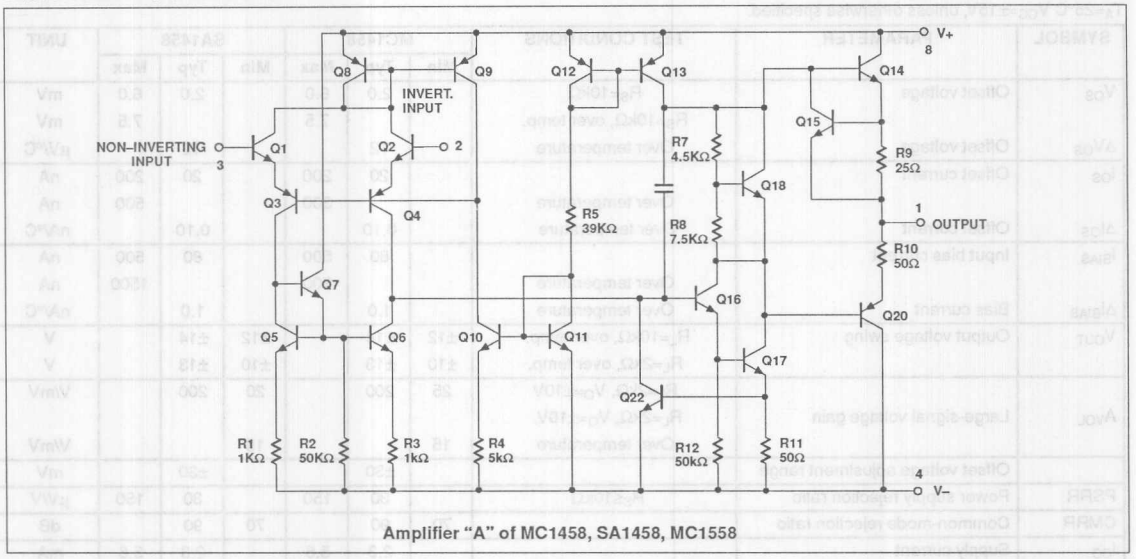
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage		
	MC1458	±18	V
	SA1458	±18	V
	MC1558	±22	V
T_J	Junction temperature	+150	°C
$P_{D\,MAX}$	Maximum power dissipation, T_A=25°C (still-air)[1]		
	N package	1160	mW
	D package	780	mW
V_{DIFF}	Differential input voltage	±30	V
V_{IN}	Input voltage[2]	±15	V
	Output short-circuit duration	Continuous	
T_A	Operating ambient temperature range		
	MC1458	0 to +70	°C
	SA1458	-40 to +85	°C
	MC1558	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. The following derating factors should be applied above 25°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC



Amplifier "A" of MC1458, SA1458, MC1558

DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_S=±15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1558			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	R_S=10kΩ		1.0	5.0	mV
		R_S=10kΩ, over temperature			6.0	mV
ΔV_{OS}	Offset voltage	Over temperature		10		µV/°C
I_{OS}	Offset current			20	200	nA
		Over temperature			500	nA
ΔI_{OS}	Offset current	Over temperature		0.10		nA/°C
I_{BIAS}	Input bias current			80	500	nA
		Over temperature			1500	nA
ΔI_{BIAS}	Bias current	Over temperature		1.0		nA/°C
V_{OUT}	Output voltage swing	R_L=10kΩ, over temperature	±12	±14		V
		R_L=2kΩ, over temperature	±10	±13		V
A_{VOL}	Large-signal voltage gain	R_L=2kΩ,V_O=±10V	50	100		V/mV
		R_L=2kΩ, V_O=± temperature	20			V/mV
	Offset voltage adjustment range			±30		mV
PSRR	Power supply rejection ratio	R_S≤10kΩ		30	150	µV/V
CMRR	Common mode rejection ratio		70	90		dB
I_{CC}	Supply current			2.3	5.0	mA
V_{IN}	Input voltage range		±12	±13		V
P_D	Power consumption			70	150	mW
	Channel separation			120		dB
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current		10	25	60	mA

DC ELECTRICAL CHARACTERISTICS (Continued)

T_A=25°C V_{CC}=±15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1458			SA1458			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	R_S=10kΩ		2.0	6.0		2.0	6.0	mV
		R_S=10kΩ, over temp.			7.5			7.5	mV
ΔV_{OS}	Offset voltage	Over temperature		12			12		µV/°C
I_{OS}	Offset current			20	200		20	200	nA
		Over temperature			300			500	nA
ΔI_{OS}	Offset current	Over temperature		0.10			0.10		nA/°C
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temperature			800			1500	nA
ΔI_{BIAS}	Bias current	Over temperature		1.0			1.0		nA/°C
V_{OUT}	Output voltage swing	R_L=10kΩ, over temp.	±12	±14		±12	±14		V
		R_L=2kΩ, over temp.	±10	±13		±10	±13		V
A_{VOL}	Large-signal voltage gain	R_L=2kΩ, V_O=±10V	25	200		20	200		V/mV
		R_L=2kΩ, V_O=±10V, Over temperature	15			15			V/mV
	Offset voltage adjustment range			±30			±30		mV
PSRR	Power supply rejection ratio	R_S≤10kΩ		30	150		30	150	µV/V
CMRR	Common-mode rejection ratio		70	90		70	90		dB
I_{CC}	Supply current			2.3	5.6		2.3	5.6	mA
V_{IN}	Input voltage range		±12	±13		±12	±13		V
R_{IN}	Input resistance		0.3	1		0.3	1		MΩ
P_D	Power consumption			70	170		70	170	mW
	Channel separation			120			120		dB
I_{SC}	Output short-circuit current			25			25		mA

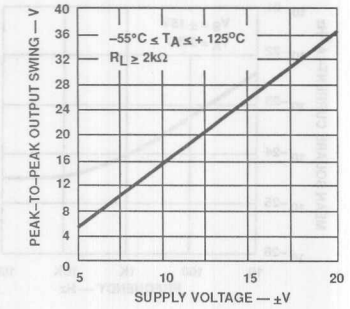
AC ELECTRICAL CHARACTERISTICS

T_A=25°C V_S=±15V, unless otherwise specified.

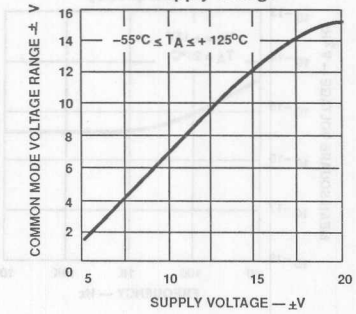
SYMBOL	PARAMETER	TEST CONDITIONS	MC1458, SA1458, MC1558			UNIT
			Min	Typ	Max	
R_{IN}	Parallel input resistance	Open-loop, f=20Hz	0.3			MΩ
	Common-mode input impedance	f=20Hz		200		MΩ
	Equivalent input noise voltage	A_V=100, R_S=10kΩ, BW=1.0kHz, f=1.0kHz		30		$nV/\sqrt{Hz}$
BW	Power bandwidth	A_V=1, R_L=2.0kΩ, THD≤5%, V_{OUT}=20V_{P-P}		14		kHz
	Phase margin			65		degrees
A_V	Gain margin			11		dB
	Unity gain crossover frequency	Open loop		1.0		MHz
	Transient response unity gain	V_{IN}=20mV, R_L=2kΩ, C_L≤100pF				
t_R	Rise time			0.3		µs
	Overshoot			5.0		%
SR	Slew rate	C_L≤100pF, R_L≥2kΩ, V_{IN}=±10V		0.8		V/µs

TYPICAL PERFORMANCE CHARACTERISTICS

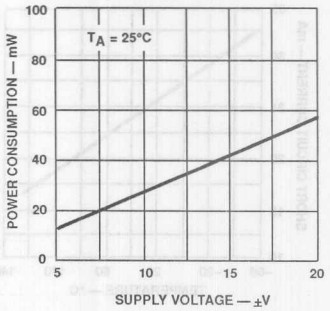
Output Voltage Swing as a Function of Supply Voltage



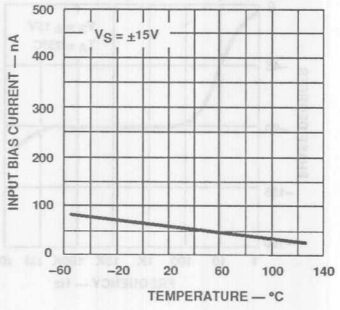
Input Common–Mode Range as a Function of Supply Voltage



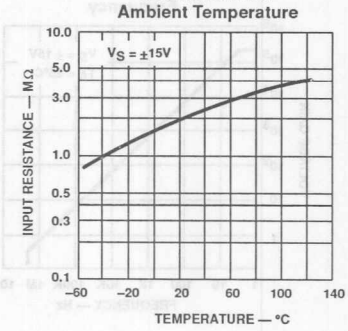
Power Consumption as a Function of Supply Voltage



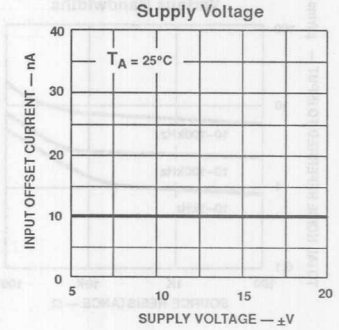
Input Bias Current as a Function Of Ambient Temperature



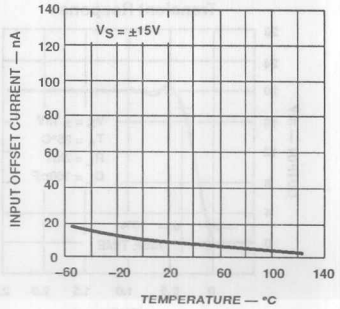
Input Resistance as a function of Ambient Temperature



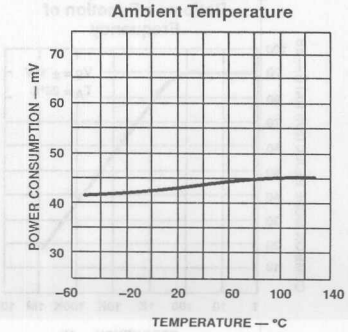
Input Offset Current as a Function of Supply Voltage



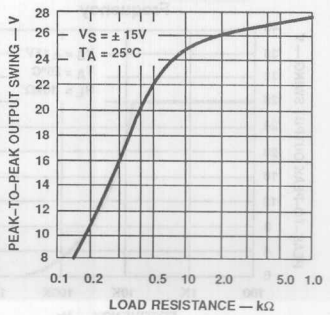
Input Offset Current as a Function of Ambient Temperature



Power Consumption as a Function of Ambient Temperature

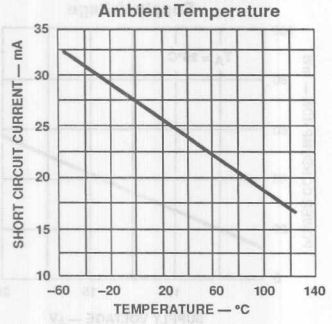


Output Voltage Swing as a Function of Load Resistance

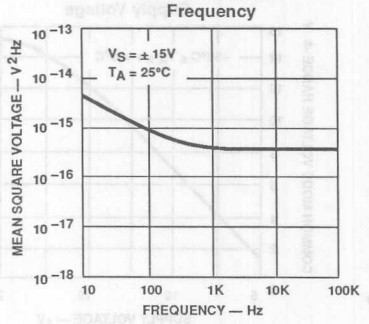


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

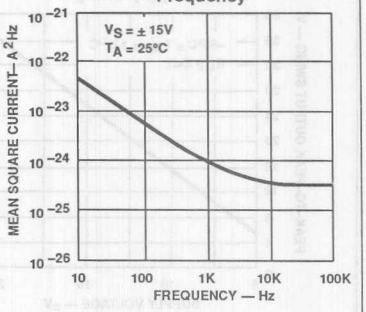
Output Short–Circuit Current as a Function of Ambient Temperature



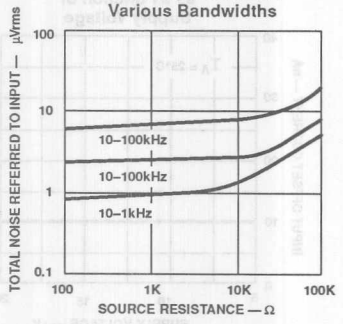
Input Noise Voltage as a Function of Frequency



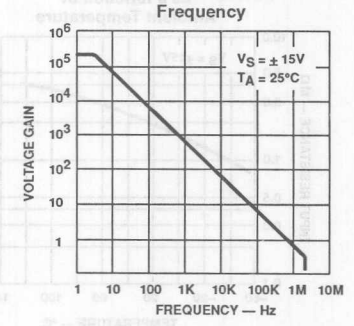
Input Noise Current as a Function of Frequency



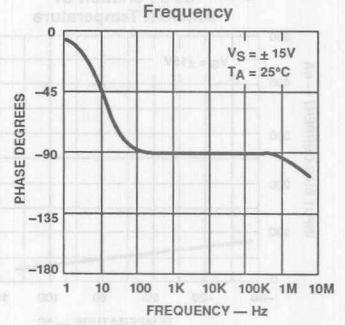
Broadband Noise for Various Bandwidths



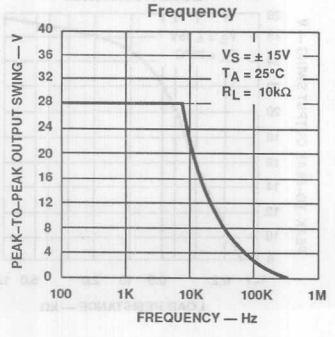
Open–Looped Voltage Gain as a Function of Frequency



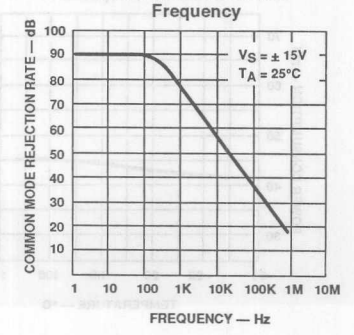
Open-Looped Phase Response as a Function of Frequency



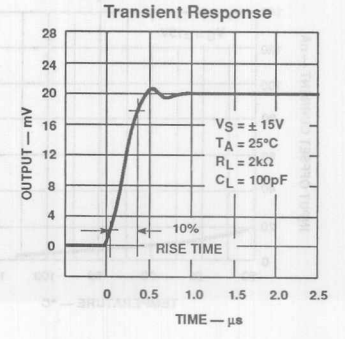
Output Voltage Swing as a Function of Frequency



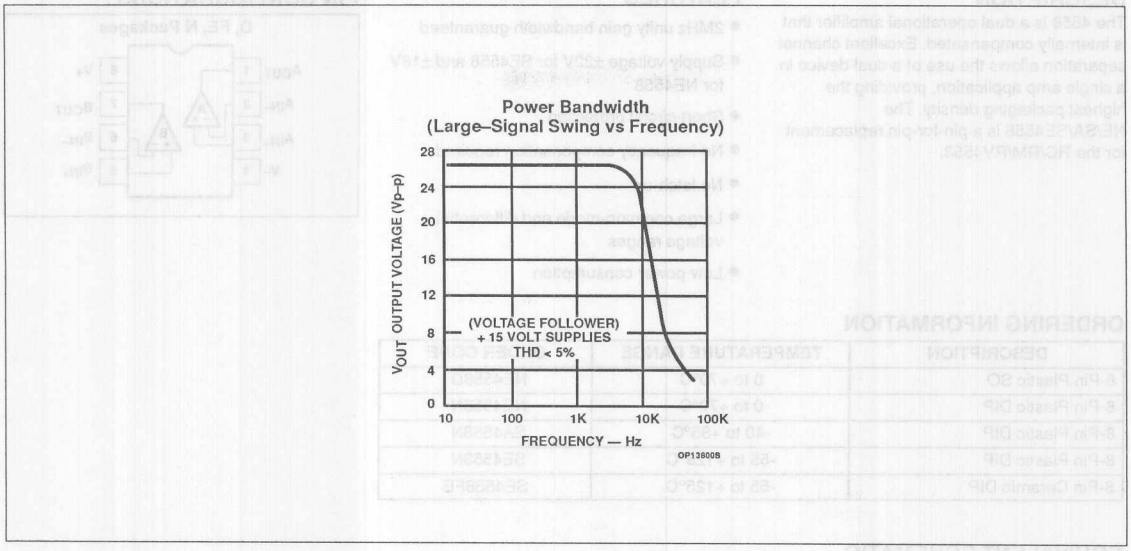
Comon–Mode Rejection Ratio as a Function of Frequency



Transient Response



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Dual general-purpose operational amplifier NE/SA/SE4558

DESCRIPTION

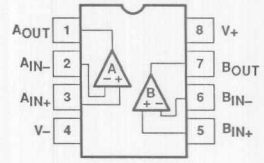
The 4558 is a dual operational amplifier that is internally compensated. Excellent channel separation allows the use of a dual device in a single amp application, providing the highest packaging density. The NE/SA/SE4558 is a pin-for-pin replacement for the RC/RM/RV4558.

FEATURES

- 2MHz unity gain bandwidth guaranteed
- Supply voltage ±22V for SE4558 and ±18V for NE4558
- Short-circuit protection
- No frequency compensation required
- No latch-up
- Large common-mode and differential voltage ranges
- Low power consumption

PIN CONFIGURATIONS

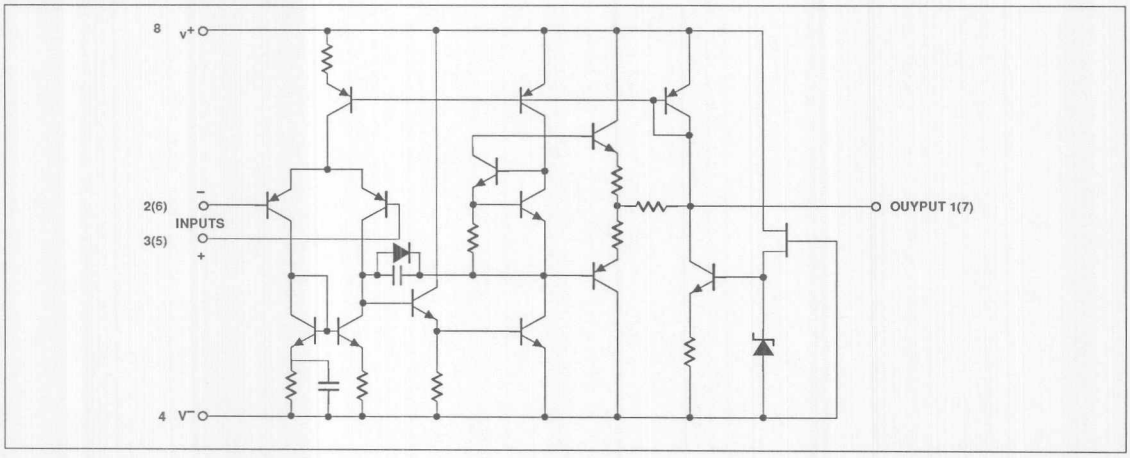
D, FE, N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE4558D
8-Pin Plastic DIP	0 to +70°C	NE4558N
8-Pin Plastic DIP	-40 to +85°C	SA4558N
8-Pin Plastic DIP	-55 to +125°C	SE4558N
8-Pin Ceramic DIP	-55 to +125°C	SE4558FE

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	SE4558	±22	V
	NE4558, SA4558	±18	V
$P_{D\ MAX}$	Maximum power dissipation, T_A=25°C (Still air)[1]		
	FE package	780	mW
	N package	1160	mW
	D package	780	mW
	Differential input voltage	±30	V
V_{IN}	Input voltage[2]	±15	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range		
	SE4558	-55 to +125	°C
	SA4558	-40 to +85	°C
	NE4558	0 to +70	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
	Output short-circuit duration[3]	Indefinite	

NOTES:
1. Derate above 25°C at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground on one amp only. Rating applies to +125°C case temperature or +75°C ambient temperature for NE4558 and to +85°C ambient temperature for SA4558.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=+15V, TA= 25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE4558			SA/NE4558			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	R_S≤10kΩ		1.0	5.0		2.0	6.0	mV
	$\Delta V_{OS}/\Delta T$	Over temp.		4			4		µV/°C
I_{OS}	Input offset current			50	200		30	200	nA
	$\Delta I_{OS}/\Delta T$	Over temp.		20			20		pA/°C
I_{BIAS}	Input bias current			40	500		200	500	nA
	$\Delta I_B/\Delta T$	Over temp.		40			40		pA/°C
R_{IN}	Input resistance		0.3	1.0		0.3	1.0		MΩ
A_V	Large-signal voltage gain	R_L≥2kΩ V_{OUT}=±10V	50,000	300,000		20,000	300,000		V/V
	Output voltage swing	R_L≥10kΩ R_L≥2kΩ	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
V_{IN}	Input voltage range		±12	±13		±12	±13		V
CMRR	<80>Common-mode rejection ratio	R_S≤10kΩ	70	100		70	100		dB
PSRR	Power supply rejection ratio	R_S≤10kΩ		10	150		10	150	µV/V
I_{SC}	Short-circuit current		5	25	60	5	25	60	mA
	Power consumption (all amplifiers)	R_L=∞		120	170		120	170	mW

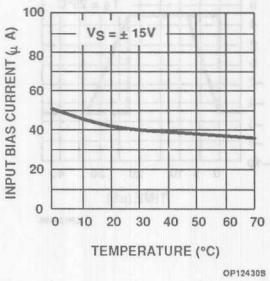
DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	SE4558			SA/NE4558			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Transient response (unity gain)	V_{IN}=20mV R_L=2kΩ C_L≤100pF							
t_R	Rise time			100			100		ns
	Overshoot			15.0			15.0		%
SR	Slew rate (unity gain)	R_L≥2kΩ		1.0			1.0		V/μs
	Channel separation (gain=100)	f=10kHz R_S=1kΩ		90			90		dB
GBW	Unity gain bandwidth (gain=1)		2.0	3.0		2.0	3.0		MHz
θ_M	Phase margin			45			45		De-gree
V_{NOISE}	Input noise voltage	f=1kΩ		25			25		nV/√Hz
NOTE: The following specifications apply over operating temperature range.									
V_{OS}	Input offset voltage	R_S≤10kΩ			6.0			7.5	mV
I_{OS}	Input offset current				500			300/500[1]	nA
I_{BIAS}	Input bias current				1500			800/1500[1]	nA
A_V	Large-signal voltage gain	R_L≥2kΩ V_{OUT}=±10V	25,000			15,000			V/V
	Output voltage swing	R_L≥2kΩ	±10			±10			V
P_C	Power consumption	T_A=HIGH T_A=LOW		105 125	150 200		115 120	150 200	mW mW

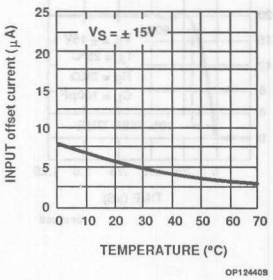
NOTES:
1. SA4558 only.

TYPICAL PERFORMANCE CURVES

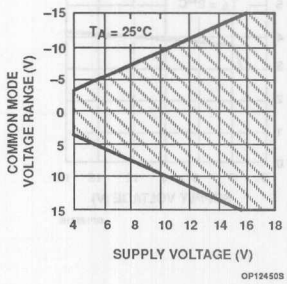
Input Bias as a Funtion of Ambient Temperature



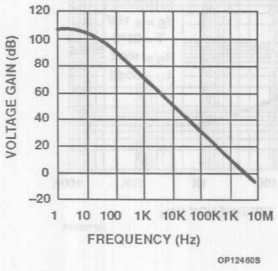
Input Offset Current as as a Funtion of Ambient Temperature



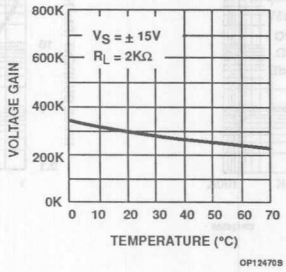
Common–Mode Range as a Funtion of Supply Voltage



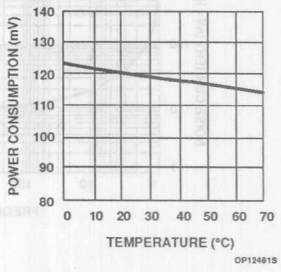
Open–Loop Voltage Gain as a Funtion of Frequency



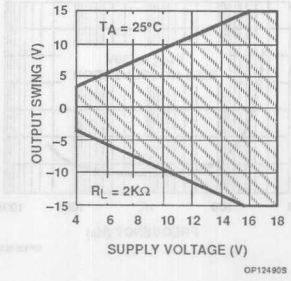
Open–Loop Gain as a Funtion of Temperature



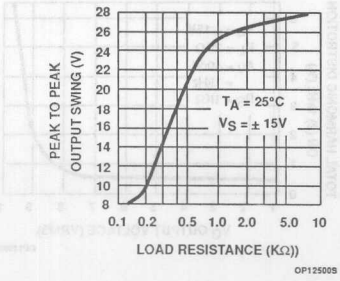
Power Consumption as a Funtion of Ambient Temperature



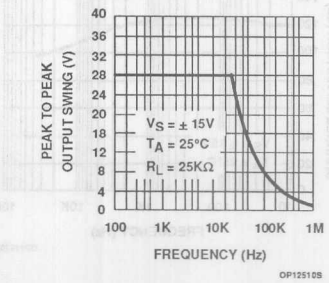
Typical Output Voltage as a Funtion of Supply Voltage



Output Voltage Swing as a Funtion of Load Resistance)

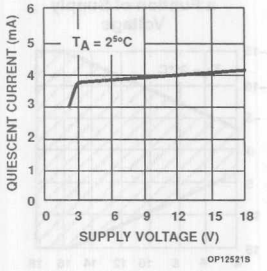


Output Voltage Swing as a Funtion of Frequency

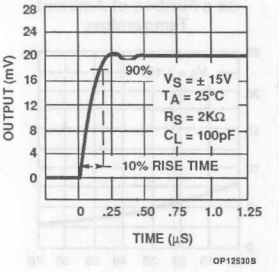


TYPICAL PERFORMANCE CURVES (Continued)

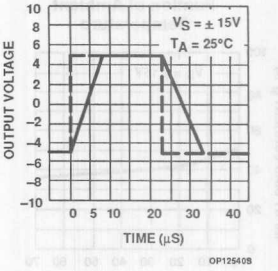
Quiescent Current as a Funtion of Supply Voltage



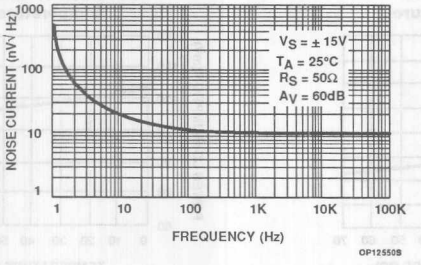
Transient Response



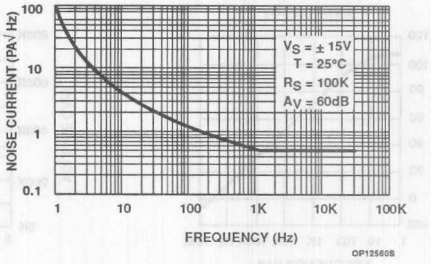
Voltage–Follower Large–Signal Pulse Response



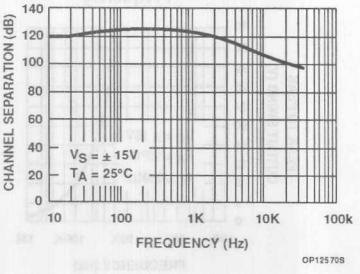
Input Noise Voltage as a Funtion of Frequency



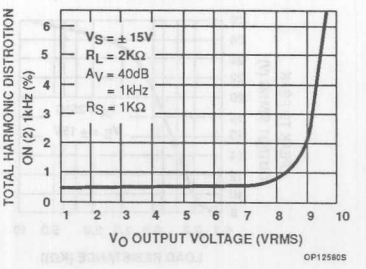
Input Noise Current as a Funtion of Frequency



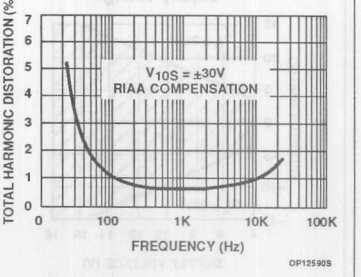
Channel Separation



Total Harmonic Distortion vs Output Voltage



Distortion vs Frequency V_O = 1V_{RMS}



High slew rate operational amplifier NE/SE531

DESCRIPTION

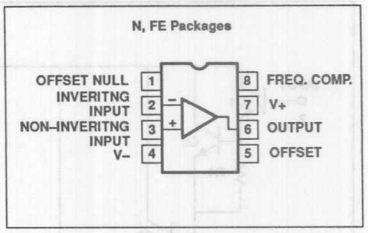
The 531 is a fast slewing high performance operational amplifier which retains DC performance equal to the best general purpose types while providing far superior large-signal AC performance. A unique input stage design allows the amplifier to have a large-signal response nearly identical to its small-signal response. The amplifier is compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large-signal bandwidths are required, the amplifier out-performs conventional designs which have much better small-signal response. Also, because the small-signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation, and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

FEATURES

- 35V/µs slew rate at unity gain
- Pin-for-pin replacement for µA709, µA748, or LM101
- Compensated with a single capacitor
- Same low drift offset null circuitry as µA741
- Small-signal bandwidth 1MHz
- Large-signal bandwidth 500kHz
- True op amp DC characteristics make the 531 the ideal answer to all slew rate limited operational amplifier applications

PIN CONFIGURATIONS

N, FE Packages



ORDERING INFORMATION

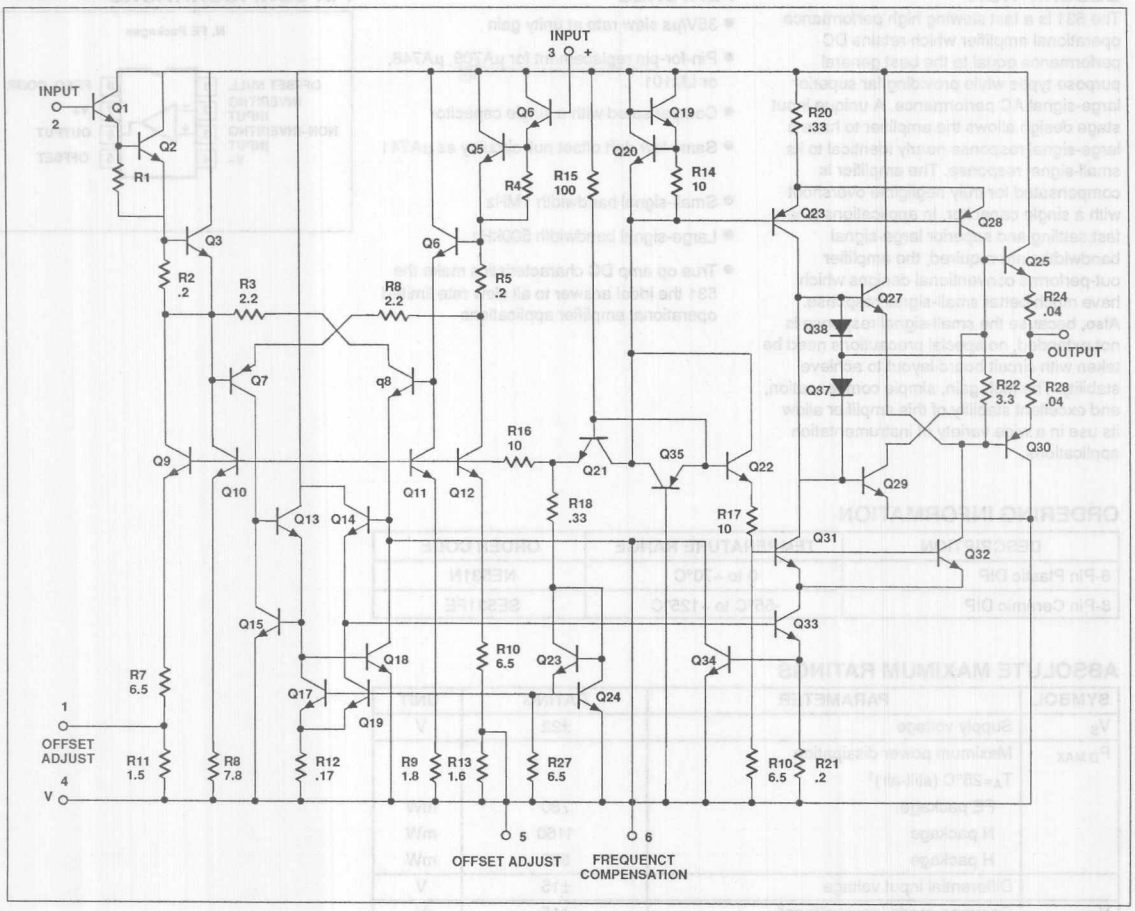
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE531N
8-Pin Ceramic DIP	-55°C to +125°C	SE531FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
$P_{D\ MAX}$	Maximum power dissipation T_A=25°C (still-air)[1]		
	FE package	780	mW
	N package	1160	mW
	H package	830	mW
	Differential input voltage	±15	V
V_{CM}	Common-mode input voltage[2]	±15	V
	Voltage between offset null and V-	±0.5	V
T_A	Operating ambient temperature range		
	NE531	0 to +70	°C
	SE531	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
	Output short-circuit duration[3]	indefinite	

NOTES:
1. The following derating factors should be applied above 25°C:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or either supply. Rating applies to +125°C case temperature or to +75°C ambient temperature.

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

V_S=±15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE531			NE531			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	R_S≤10kΩ, T_A=25°C		2.0	5.0		2.0	6.0	mV
		R_S310kΩ, over temp			6.0			7.5	mV
ΔV_{OS}		Over temp		10			10		µV/°C
I_{OS}	Offset current	T_A=25°C		30	200		50	200	nA
		T_A=High			200			200	nA
		T_A=Low			500			300	nA
ΔI_{OS}		Over temp		0.4			0.4		nA/°C
I_{BIAS}	Input bias current	T=25°C		300	500		400	1500	nA
		T_A=High			500			1500	nA
		T_A=Low			1500			2000	nA
ΔI_{BIAS}		Over temp		2			2		nA/°C
V_{CM}	80Common-mode voltage range	T_A=25°C	±10			±10			V
CMRR	<80>Common-mode rejection ratio	T_A=25°C, R_S≤10kΩ				70	100		dB
		Over temp R_S≤10kΩ	70	90					dB
R_{IN}	Input resistance	T_A=25°C		20			20		MΩ
V_{OUT}	Output voltage swing	R_L≥10kΩ, over temp	±10	±13		±10	±13		V
I_{CC}	Supply current	T_A=25°C			7.0			10	mA
		T_{MAX}			7.0			10	mA
P_D	Power consumption	T_A=25°C			210			300	mW
PSRR	Power supply rejection ratio	R_S≤10kΩ, T_A=25°C					10	150	µV/V
		R_S≤10kΩ, over temp		10	150				µV/V
R_{OUT}	Output resistance	T_A=25°C		75			75		Ω
A_{VOL}	Large-signal voltage gain	T_A=25°C, R_L≥10kΩ, V_{OUT}=±10V	50	100		20	60		V/mV
		R_L≥10kΩ, V_{OUT}=±10V, over temp	25			15			V/mV
V_{INN}	Input noise voltage	25°C f=1kHz		20			20		nV/√Hz
I_{SC}	Short-circuit current	25°C	5	15	45	5	15	45	mA

AC ELECTRICAL CHARACTERISTICS

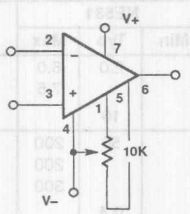
T_A=25°C V_S=+15V, unless otherwise specified.[1]

SYMBOL	PARAMETER	TEST CONDITIONS	NE531			SE531			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Full power bandwidth			500			500		kHz
t_S	Settling time (1%)	A_V=+1, V_{IN}=±10V		1.5			1.5		µs
	(0.1%)			2.5			2.5		µs
	Large-signal overshoot	A_V=+1, V_{IN}=±10V		2			2		%
	Small-signal overshoot	A_V=+1, V_{IN}=400mV		5			5		%
t_R	Small-signal rise time	A_V=+1, V_{IN}=400mV		300			300		ns
SR	Slew rate	A_V=100		35			35		V/µs
		A_V=10		35			35		V/µs
		A_V=1 (non-inverting)		30		20	30		V/µs
		A_V=1 (inverting)		35		25	35		V/µs

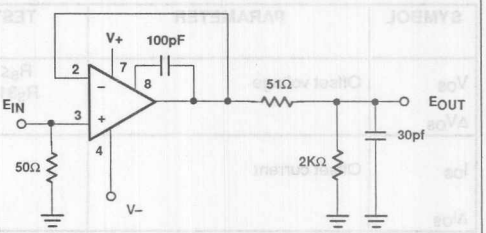
NOTES:

1. All AC testing is performed in the transient response test circuit.

TEST LOAD CIRCUITS

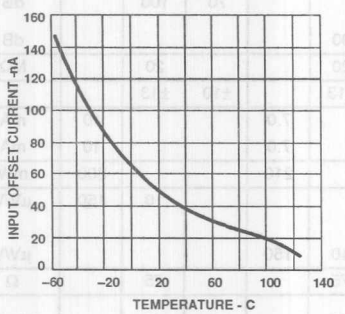


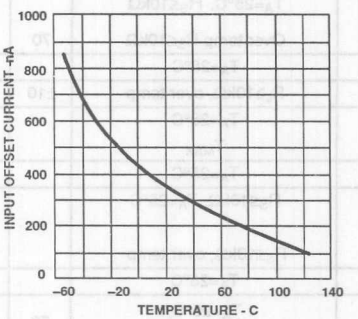
Offset Null Circuit

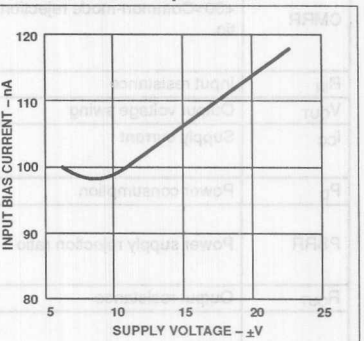


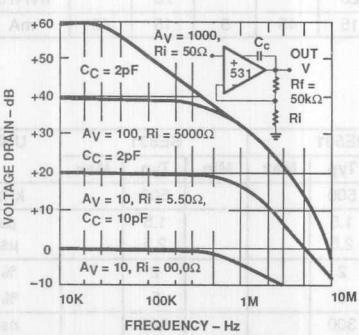
Transient Response Circuit

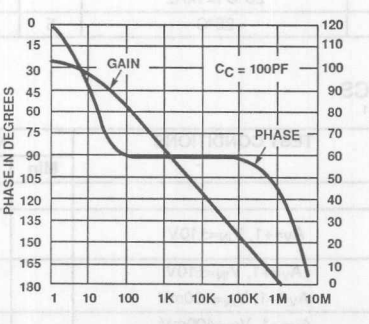
TYPICAL PERFORMANCE CHARACTERISTICS $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise specified.

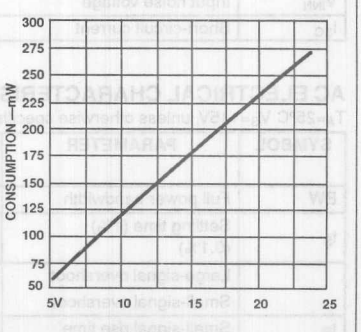




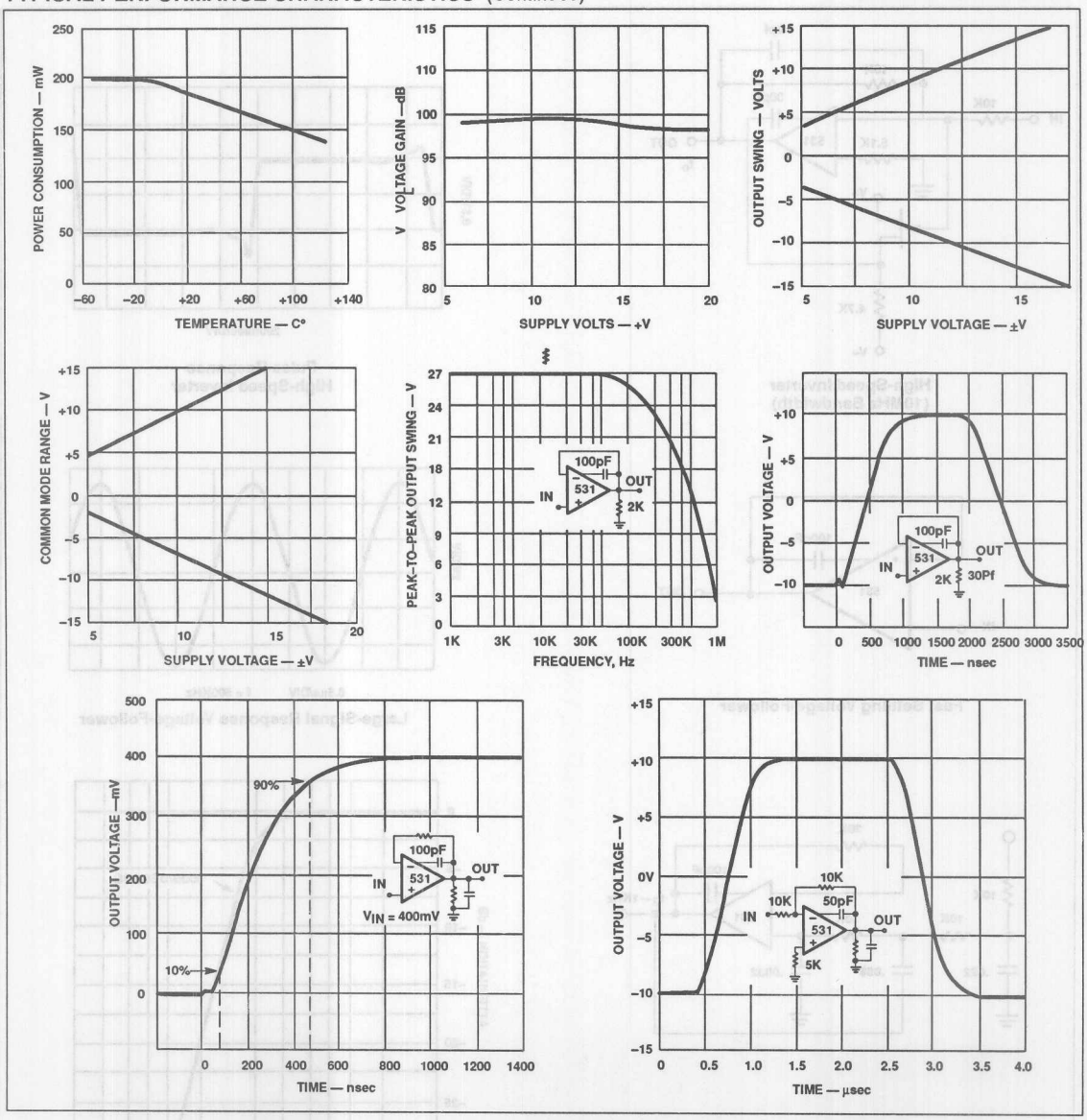




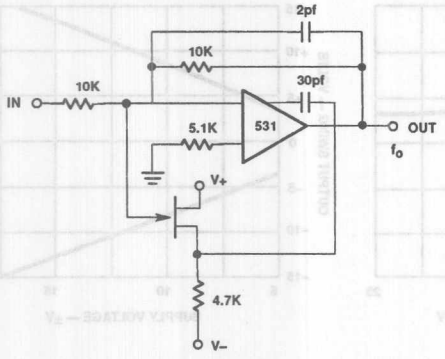




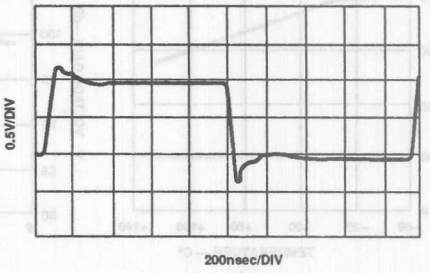
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



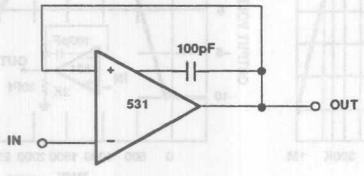
TYPICAL APPLICATIONS



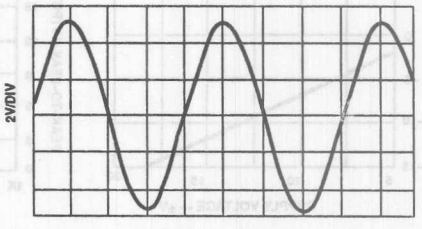
High-Speed Inverter
(10MHz Bandwidth)



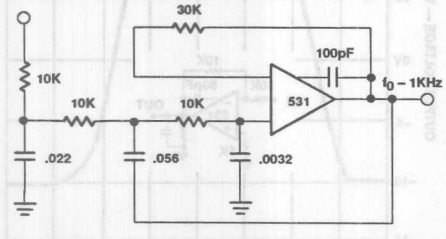
Pulse Response
High-Speed Inverter



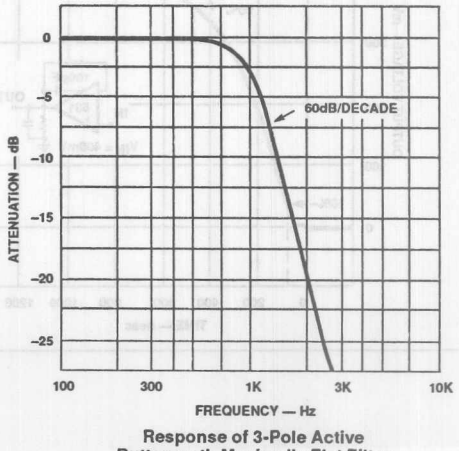
Fast Settling Voltage-Follower



Large-Signal Response Voltage-Follower

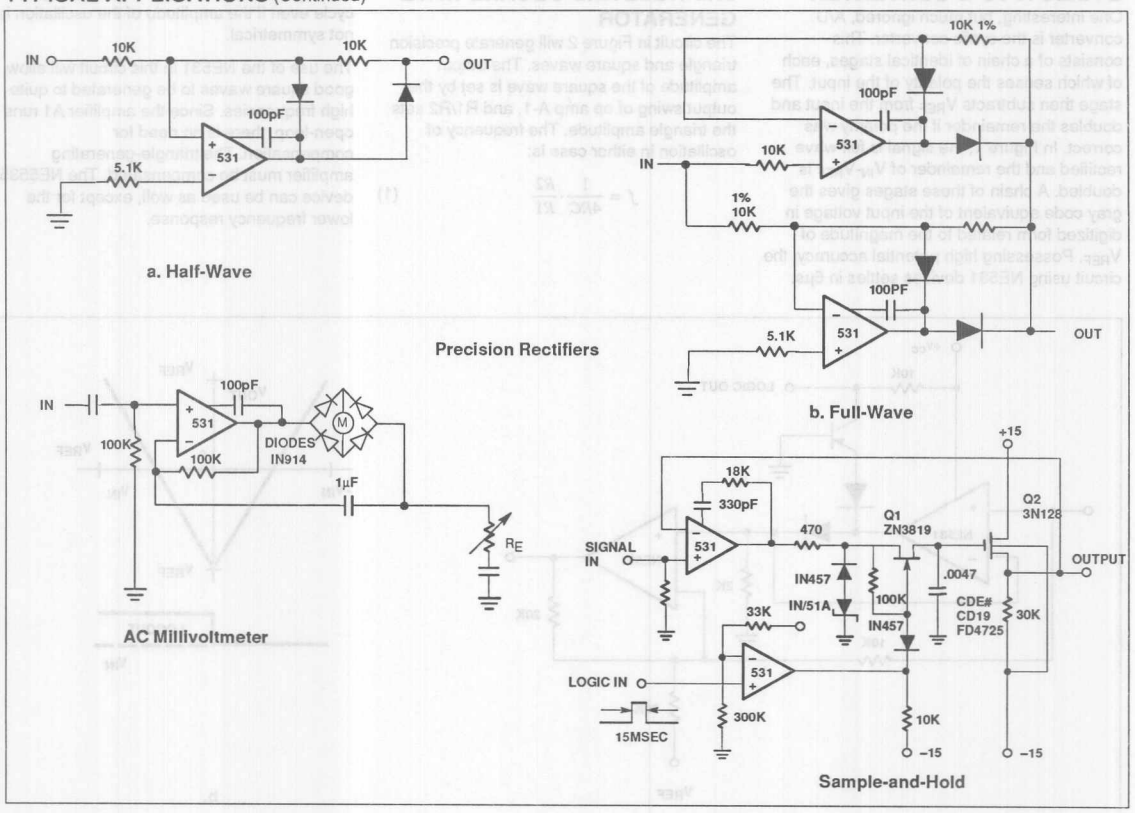


Three-Pole Active Low-Pass Filter Butterworth
Maximally Flat Response[1]



Response of 3-Pole Active
Butterworth Maximally Flat Filter

TYPICAL APPLICATIONS (Continued)



CYCLIC A-TO-D CONVERTER

One interesting, but much ignored, A/D converter is the cyclic converter. This consists of a chain of identical stages, each of which senses the polarity of the input. The stage then subtracts V_{REF} from the input and doubles the remainder if the polarity was correct. In Figure 1, the signal is full-wave rectified and the remainder of V_{IN}-V_{REF} is doubled. A chain of these stages gives the gray code equivalent of the input voltage in digitized form related to the magnitude of V_{REF}. Possessing high potential accuracy, the circuit using NE531 devices settles in 5µs.

TRIANGLE AND SQUARE WAVE GENERATOR

The circuit in Figure 2 will generate precision triangle and square waves. The output amplitude of the square wave is set by the output swing of op amp A-1, and R1/R2 sets the triangle amplitude. The frequency of oscillation in either case is:

$$f = \frac{1}{4RC} \cdot \frac{R2}{R1} \quad (1)$$

The square wave will maintain 50% duty cycle even if the amplitude of the oscillation is not symmetrical.

The use of the NE531 in this circuit will allow good square waves to be generated to quite high frequencies. Since the amplifier A1 runs open-loop, there is no need for compensation. The triangle-generating amplifier must be compensated. The NE5535 device can be used as well, except for the lower frequency response.

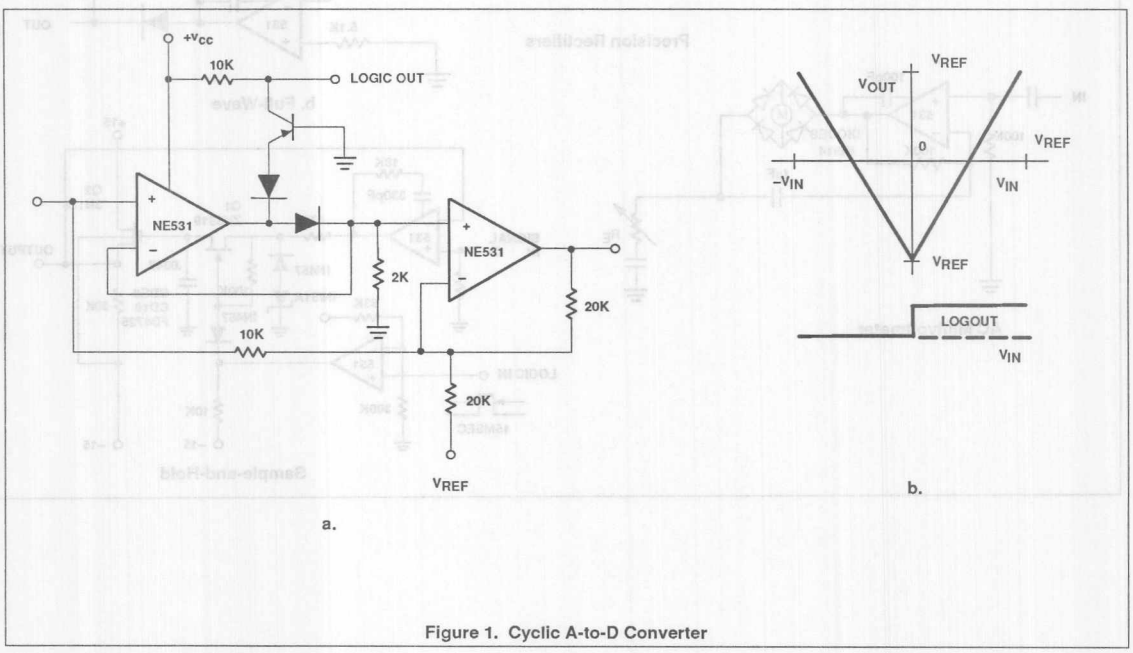


Figure 1. Cyclic A-to-D Converter

Dual high-performance operational amplifier NE/SA/SE5512

DESCRIPTION

The 5512 series of high-performance operational amplifiers provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector-to-emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability, yet have low supply quiescent current.

APPLICATIONS

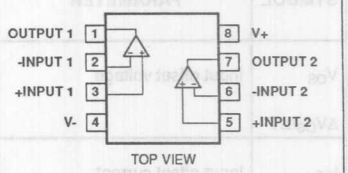
- AC amplifiers
- RC active filters
- Transducer amplifiers
- DC gain block
- Battery operation
- Instrumentation amplifiers

FEATURES

- Low input bias < ±20nA
- Low input offset current < ±20nA
- Low input offset voltage <1mV
- Low VOS temperature drift 5µV/°C
- Low input bias temperature drift 40pA/°C
- Low input voltage noise 30nV/√Hz
- Low supply current 1.5mA/amp
- High slew rate 1.0V/µs
- High CMRR 100dB
- High input impedance 100MΩ
- High PSRR 110dB
- High differential input voltage limit
- No crossover distortion
- Indefinite output short circuit protection
- Internally-compensated for unity gain
- 600Ω drive capability
- MIL-STD processing available

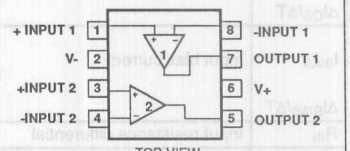
PIN CONFIGURATIONS

N Package



TOP VIEW

D Package[1]



TOP VIEW

NOTE:
1. The D package pinout is not functionally identical to the FE or N pinout.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to 70°C	NE5512D
8-Pin Plastic DIP	0 to 70°C	NE5512N
8-Pin Plastic SO	-40 to +85°C	SA5512D
8-Pin Plastic DIP	-40 to +85°C	SA5512N
8-Pin Plastic DIP	-55 to +125°C	SE5512N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±16	V
$P_{D\,MAX}$	Maximum power dissipation, T_A=25°C (still air)[1]		
	FE package	850	mW
	N package	1212	mW
	D package	800	mW
T_A	Operating ambient temperature range		
	NE5512	0 to +70	°C
	SA5512	-40 to +85	°C
	SE5512	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. The following derating factors should be applied above 25°C
   N package at 9.7mW/°C
   D package at 6.4mW/°C

ELECTRICAL PERFORMANCE CHARACTERISTICS

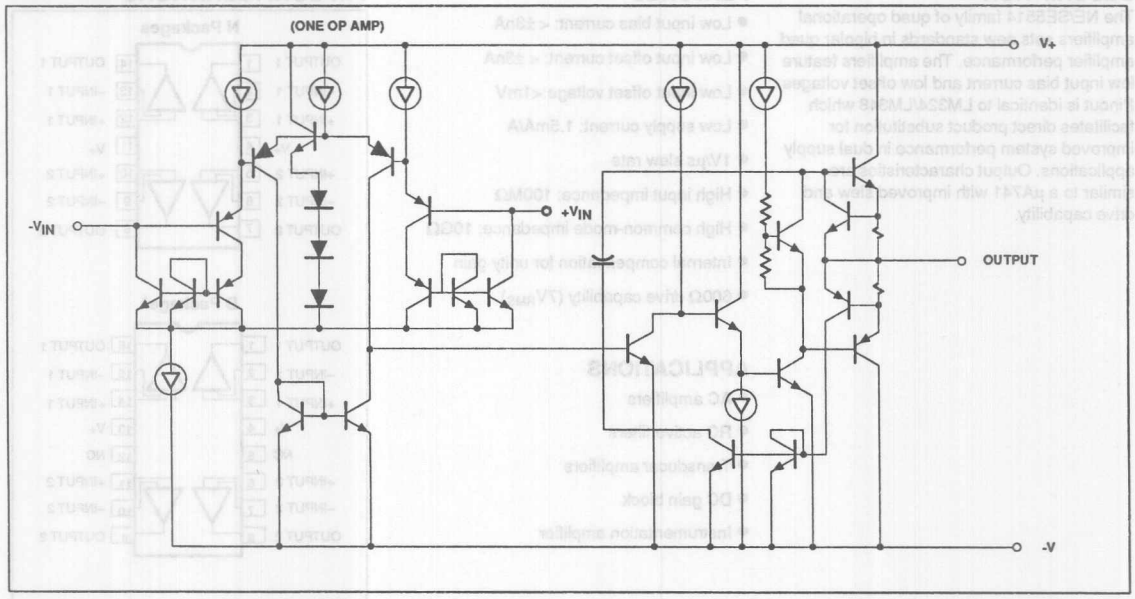
V_{CC} = ±15V, T_A = 25°C over temperature range, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5512			NE/SA5512			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	R_S=100Ω T_A=+25°C Over temp.		0.7 1	2 3		1 1.5	5 6	mV
$\Delta V_{OS}/\Delta T$				4			5		µV/°C
I_{OS}	Input offset current	R_S=100kΩ T_A=+25°C Over temp.		3 4	10 20		6 8	20 30	nA
$\Delta I_{OS}/\Delta T$				30			40		pA/°C
I_{BIAS}	Input bias current	R_S=100kΩ T_A=+25°C Over temp.		3 4	10 20		6 8	20 30	nA
$\Delta I_{BIAS}/\Delta T$				30			40		pA/°C
R_{IN}	Input resistance differential	T_A=+25°C		100			100		MΩ
V_{CM}	Input common mode range	T_A=+25°C Over temp.	±13.5 ±13	±13.7 ±13.2		±13.5 ±13	±13.7 ±13.2		V
CMRR	Input common-mode rejection ratio	V_{CC}=±15V V_{IN}=±13.5V T_A=+25°C V_{IN}=±13V Over temp.	70	100		70	100		dB
A_V	Large-signal voltage gain	R_L=2kΩ T_A=25°C V_O=±10V over temp.	50 25	200		50 25	200		V/mV
SR	Slew rate	T_A=25°C	0.6	1			1		V/µs
GBW	Small-signal unity gain bandwidth	T_A=25°C		3			3		MHz
θ_M	Phase margin	T_A=25°C		45			45		degree
V_{OUT}	Output voltage swing	R_L=2kΩ T_A=25°C Over temp.	±13 ±12.5	±13.5 ±13		±13 ±12.5	±13.5 ±13		V
V_{OUT}	Output voltage swing	R_L=600Ω[1] T_A=25°C Over temp.	±10 ±7.5	±11.5 ±9		±10 ±8	±11.5 ±9		V
I_{CC}	Power supply current	R_L=Open T_A=25°C Over temp.		3.4 3.6	5 5.5		3.4 3.6	5 5.5	mA
PSRR	Power supply rejection ratio	Over temp.	80	100		80	100		dB
AA	Amplifier-to-amplifier coupling	f=1kHz to 20kHz, T_A=25°C		-120			-120		dB
THD	Total harmonic distortion	f=10kHz T_A=25°C V_O=7V_{RMS}		0.01			0.01		%
V_{NOISE}	Input noise voltage	f=1kHz T_A=25°C		30			30		nV/√Hz
I_{NOISE}	Input noise current	f=1kHz T_A=25°C		0.2			0.2		pA/√Hz
I_{SC}	Short-circuit current	±15V, T_A=25°C		40			40		mA

NOTES:

1. Not to exceed maximum package power dissipation.

EQUIVALENT SCHEMATIC



Quad high-performance operational amplifier NE/SE5514

DESCRIPTION

The NE/SE5514 family of quad operational amplifiers sets new standards in bipolar quad amplifier performance. The amplifiers feature low input bias current and low offset voltages. Pinout is identical to LM324/LM348 which facilitates direct product substitution for improved system performance in dual supply applications. Output characteristics are similar to a µA741 with improved slew and drive capability.

FEATURES

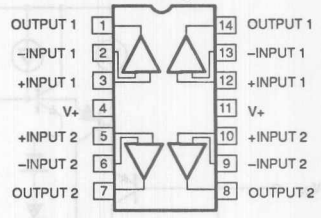
- Low input bias current: < ±3nA
- Low input offset current: < ±3nA
- Low input offset voltage:<1mV
- Low supply current: 1.5mA/A
- 1V/µs slew rate
- High input impedance: 100MΩ
- High common-mode impedance: 10GΩ
- Internal compensation for unity gain
- 600Ω drive capability ($7V_{RMS}$)

APPLICATIONS

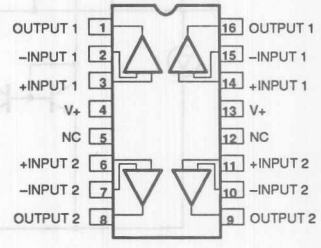
- AC amplifiers
- RC active filters
- Transducer amplifiers
- DC gain block
- Instrumentation amplifier

PIN CONFIGURATIONS

N Packages



D Package[1]

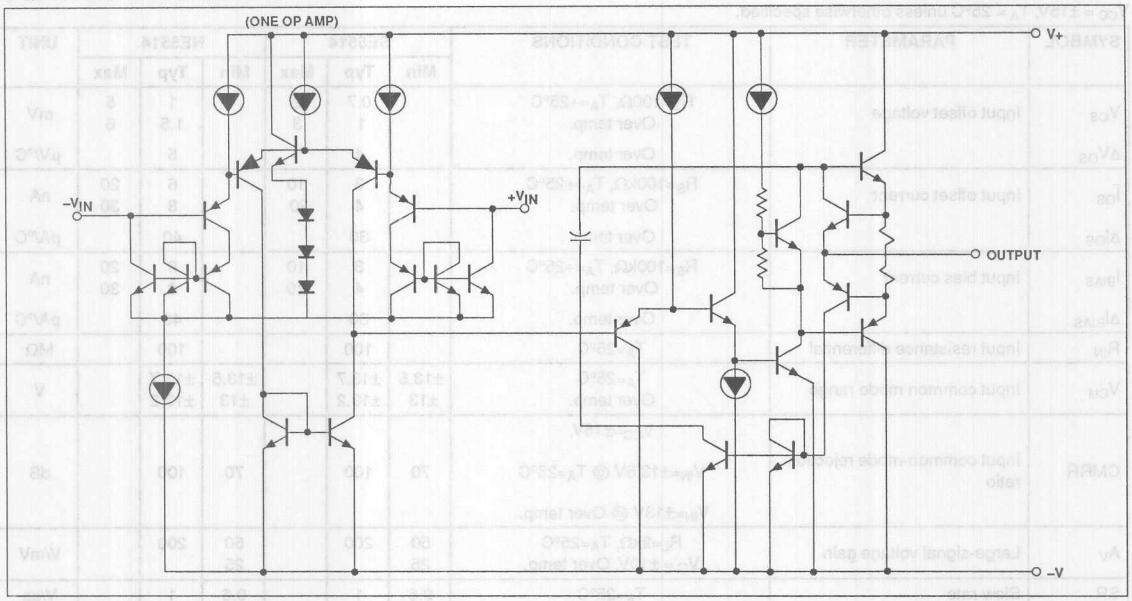


NOTE:
1. SOL - Released in 16-lead large SO package only. Pinout is different than N package.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SOL package	0 to +70°C	NE5514D
14-Pin Plastic DIP	0 to +70°C	NE5514N
14-Pin Plastic DIP	-55 to +125°C	SE5514N

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±16	V
V_{DIFF}	Differential input voltage	32	V
V_{IN}	Input voltage	0 to 32	V
	Output short to ground	Continuous	
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
T_A	Operating ambient temperature range		
	NE5514	0 to 70	°C
	SE5514	-55 to +125	°C
P_{MAX}	Maximum power disspation		
	T_A=25°C (still-air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1250	mW

NOTES:

1. The following derating factors should be applied above 25°C
   N package at 11.4mW/°C
   D package at 10.0mW/°C

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_A = 25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5514			NE5514			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	R_S=100Ω, T_A=+25°C Over temp.		0.7 1	2 3		1 1.5	5 6	mV
ΔV_{OS}		Over temp.		4			5		µV/°C
I_{OS}	Input offset current	R_S=100kΩ, T_A=+25°C Over temp.		3 4	10 20		6 8	20 30	nA
ΔI_{OS}		Over temp.		30			40		pA/°C
I_{BIAS}	Input bias current	R_S=100kΩ, T_A=+25°C Over temp.		3 4	10 20		6 8	20 30	nA
ΔI_{BIAS}		Over temp.		30			40		pA/°C
R_{IN}	Input resistance differential	T_A=25°C		100			100		MΩ
V_{CM}	Input common mode range	T_A=25°C Over temp.	±13.5 ±13	±13.7 ±13.2		±13.5 ±13	±13.7 ±13.2		V
CMRR	Input common-mode rejection ratio	V_{CC}=±15V, V_{IN}=±13.5V @ T_A=25°C V_{IN}=±13V @ Over temp.	70	100		70	100		dB
A_V	Large-signal voltage gain	R_L=2kΩ, T_A=25°C V_O = ±10V, Over temp.	50 25	200		50 25	200		V/mV
SR	Slew rate	T_A=25°C	0.6	1		0.6	1		V/µs
GBW	Small-signal unity gain bandwidth	T_A=25°C		3			3		MHz
θ_M	Phase margin	T_A=25°C		45			45		Degr
V_{OUT}	Output voltage swing	R_L=2kΩ, T_A=25°C Over temp.	±13 ±12.5	±13.5 ±13		±13 ±12.5	±13.5 ±13		V
V_{OUT}	Output voltage swing	R_L=600Ω[1], T_A=25°C Over temp.	±10 ±7.5	±11.5 ±9		±10 ±8	±11.5 ±9		V
I_{CC}	Power supply current	R_L=Open, T_A=25°C Over temp.		6 7	10 12		6 7	10 12	mA
PSRR	Power supply rejection ratio	±5V ≤ V_{CC} ≤ ±15V Over temp.	80	110		80	110		dB
AA	Amplifier to amplifier coupling	f=1kHz to 20kHz, T_A=25°C		-120			-120		dB
THD	Total harmonic distortion	f=10kHz, T_A=25°C V_O=7V_{RMS}		0.01			0.01		%
V_{NOISE}	Input noise voltage	f=1kHz, T_A=25°C		30			30		nV/√Hz
I_{SC}	Short-circuit current	T_A=25°C	10	40	60	10	40	60	mA

NOTES:
1. Not to exceed maximum power dissipation.

Internally-compensated dual low noise operational amplifier

NE/SE5532/5532A

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

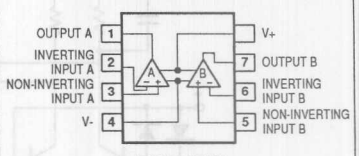
This makes the device especially suitable for application in high-quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used because it has guaranteed noise voltage specifications.

FEATURES

- Small-signal bandwidth: 10MHz
- Output drive capability: 600Ω, 10VRMS
- Input noise voltage: $5nV/\sqrt{Hz}$ (typical)
- DC voltage gain: 50000
- AC voltage gain: 2200 at 10kHz
- Power bandwidth: 140kHz
- Slew rate: 9V/μs
- Large supply voltage range: ±3 to ±20V
- Compensated for unity gain

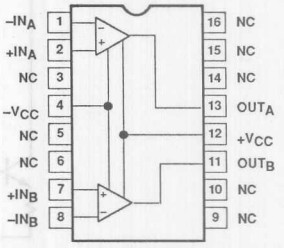
PIN CONFIGURATIONS

FE, N Packages



TOP VIEW

D Package[1]



TOP VIEW

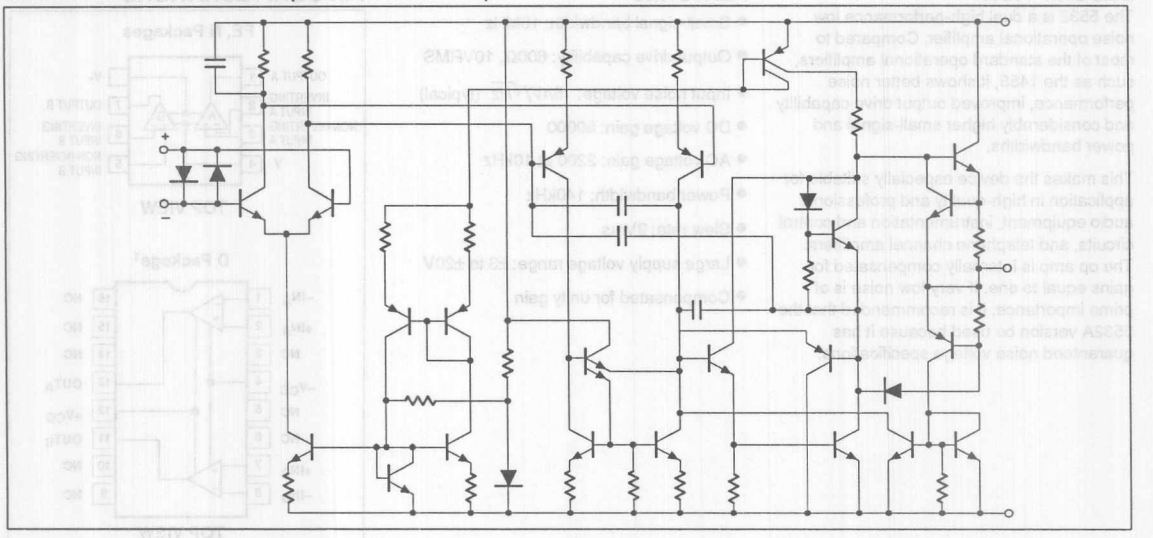
NOTE:
1. SOL and non-standard pinout.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to 70°C	NE5532N
8-Pin Ceramic DIP	0 to 70°C	NE5532FE
8-Pin Plastic DIP	0 to 70°C	NE5532AN
8-Pin Ceramic DIP	0 to 70°C	NE5532AF
8-Pin Ceramic DIP	-55°C to +125°C	SE5532FE
8-Pin Ceramic DIP	-55°C to +125°C	SE5532AF
16-Pin Plastic SOL	0 to 70°C	NE5532D

Internally-compensated dual low noise operational amplifier

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	$\pm V_{SUPPLY}$	V
V_{DIFF}	Differential input voltage[1]	±0.5	V
T_A	Operating temperature range		
	NE5532/A	0 to 70	°C
	SE5532/A	-55 to +125	°C
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Maximum power dissipation, T_A=25°C (still-air)[2]		
	N package	1200	mW
	F package	1000	mW
	D package	1200	mW
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. Thermal resistances of the above packages are as follows:
   N package at 100°C/W
   F package at 135°C/W
   D package at 105°C/W

DC ELECTRICAL CHARACTERISTICS

T_A=25°C V_S=±15V, unless otherwise specified. [1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	SE5532/5532A			NE5532/5532A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			0.5	2		0.5	4	mV
		Over temperature			3			5	mV
$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Offset current				100		10	150	nA
		Over temperature			200			200	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_B	Input current			200	400		200	800	nA
		Over temperature			700			1000	nA
$\Delta I_B/\Delta T$				5			5		nA/°C
I_{CC}	Supply current			8	10.5		8	16	mA
		Over temperature			13				mA
V_{CM}	Common-mode input range		±12	±13		±12	±13		V
CMRR	Common-mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	µV/V
A_{VOL}	Large-signal voltage gain	R_L≥2kΩ, V_O=±10V	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
		R_L≥600Ω, V_O=±10V	40	50		15	50		V/mV
		Over temperature	20			10			V/mV
V_{OUT}	Output swing	R_L≥600Ω	±12	±13		±12	±13		V
		Over temperature	±10	±12		±10	±12		V
		R_L≥600Ω, V_S=±18V	±15	±16		±15	±16		V
		Over temperature	±12	±14		±12	±14		V
		R_L≥2kΩ	±13	±13.5		±13	±13.5		V
		Over temperature	±12	±12.5		±10	±12.5		V
R_{IN}	Input resistance		30	300		30	300		kΩ
I_{SC}	Output short circuit current		10	38	60	10	38	60	mA

NOTES:
1. Diodes protect the inputs against overvoltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature, derate packages based on the package thermal resistance.
3. Output may be shorted to ground at V_S=±15V, T_A=25°C Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

AC ELECTRICAL CHARACTERISTICS

T_A=25°C V_S=±15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5532/5532A			UNIT
			Min	Typ	Max	
R_{OUT}	Output resistance	A_V=30dB Closed-loop f=10kHz, R_L=600Ω		0.3		Ω
	Overshoot	Voltage-follower V_{IN}=100mV_{P-P} C_L=100pF, R_L=600Ω		10		%
A_V	Gain	f=10kHz		2.2		V/mV
GBW	Gain bandwidth product	C_L=100pF, R_L=600Ω		10		MHz
SR	Slew rate			9		V/μs
	Power bandwidth	V_{OUT}=±10V		140		kHz
		V_{OUT}=±14V, R_L=600Ω, V_{CC}=±18V		100		kHz

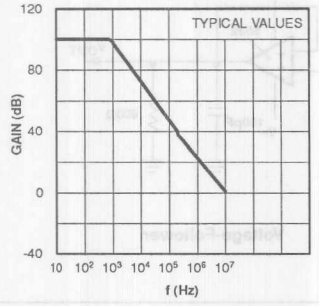
ELECTRICAL CHARACTERISTICS

T_A=25°C V_S=±15V, unless otherwise specified.

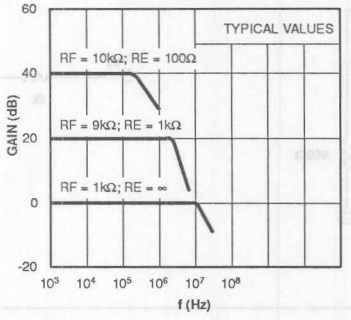
SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5532			NE/SE5532A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{NOISE}	Input noise voltage	f_O=30Hz		8			8	12	nV/√Hz
		f_O=1kHz		5			5	6	nV/√Hz
I_{NOISE}	Input noise current	f_O=30Hz		2.7			2.7		pA/√Hz
		f_O=1kHz		0.7			0.7		pA/√Hz
	Channel separation	f=1kHz, R_S=5kΩ		110			110		dB

TYPICAL PERFORMANCE CHARACTERISTICS

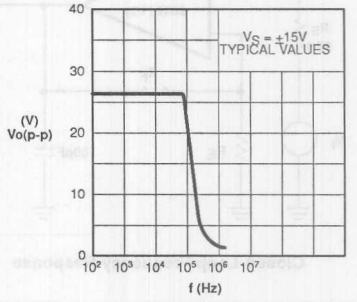
Open-Loop Frequency Response



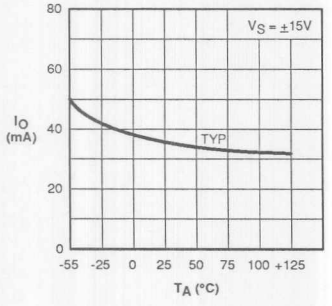
Closed-Loop Frequency Response



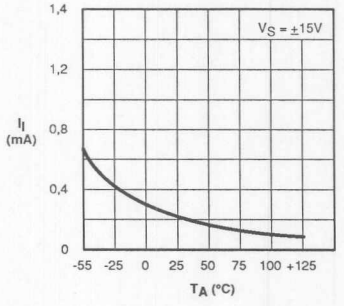
Large-Signal Frequency Response



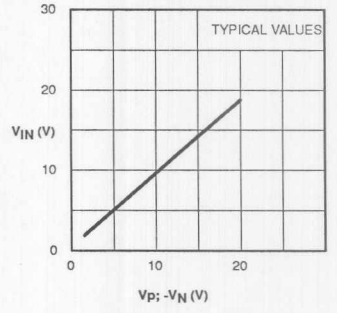
Output Short-Circuit Current



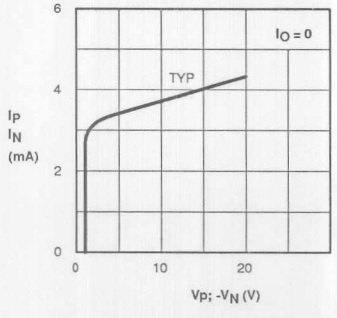
Input Bias Current



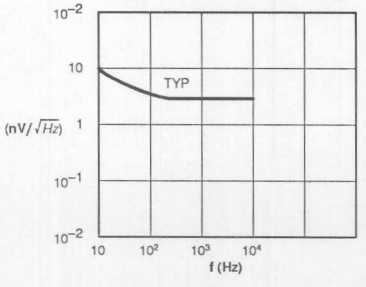
Input Commom-Mode Voltage Range



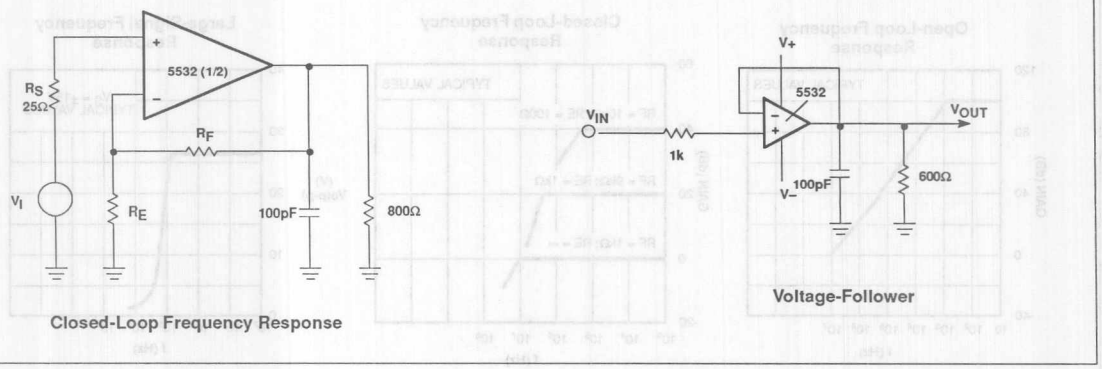
Supply Current



Input Noise Voltage Density



TEST CIRCUITS



Dual and single low noise op amp

NE5533/5533A/ NE/SA/SE5534/5534A

DESCRIPTION

The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

FEATURES

- Small-signal bandwidth: 10MHz
- Output drive capability: 600Ω, 10VRMS at VS=±18V
- Input noise voltage: $4nV/\sqrt{Hz}$
- DC voltage gain: 100000
- AC voltage gain: 6000 at 10kHz
- Power bandwith: 200kHz
- Slew rate: 13V/μs
- Large supply voltage range: ±3 to ±20V
- 5534 MIL-STD processing available

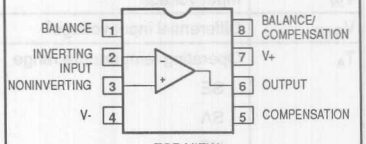
APPLICATIONS

- Audio equipment
- Instrumentation and control circuits
- Telephone channel amplifiers
- Medical equipment

PIN CONFIGURATIONS

NE/SA/SE5534/5534A

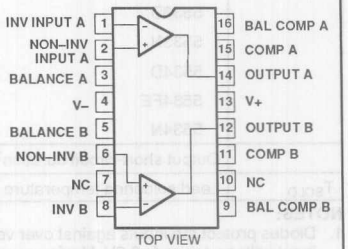
D, FE, N Packages



TOP VIEW

NE5533/5533A

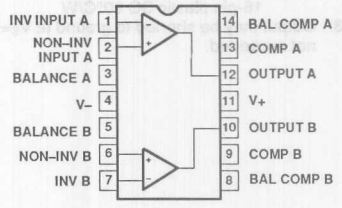
D Package



TOP VIEW

NE5533/5533A

D Package



TOP VIEW

NOTE:
This device may not be symboled in standard format

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5533N
16-Pin Plastic SO package	0 to +70°C	NE5533AD
14-Pin Plastic DIP	0 to +70°C	NE5533AN
16-Pin Plastic SO package	0 to +70°C	NE5533D
8-Pin Plastic SO package	0 to +70°C	NE5534D
8-Pin Hermetic Cerdip	0 to +70°C	NE5534FE
8-Pin Plastic DIP	0 to +70°C	NE5534N
8-Pin Plastic SO package	0 to +70°C	NE5534AD
8-Pin Hermetic Cerdip	0 to +70°C	NE5534AF
8-Pin Plastic DIP	0 to +70°C	NE5534AN
8-Pin Plastic DIP	-40°C to +85°C	SA5534N
8-Pin Plastic SO package	-40°C to +85°C	SA5534AD
8-Pin Hermetic Cerdip	-55°C to +125°C	SE5534AF
8-Pin Plastic DIP	-55°C to +125°C	SE5534N
8-Pin Hermetic Cerdip	-55°C to +125°C	SE5534AF
8-Pin Plastic DIP	-55°C to +125°C	SE5534AN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage[1]	±0.5	V
T_A	Operating temperature range		
	SE	-55 to +125	°C
	SA	-40 to +85	°C
	NE	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation at 25°C[2]		
	5533D	1350	mW
	5533N	1500	mW
	5534D	750	mW
	5534FE	800	mW
	5534N	1150	mW
	Output short-circuit duration[3]	Indefinite	
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Diodes protect the inputs against over voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature, derate packages based on the following junction-to-ambient thermal resistance:
   8-pin ceramic DIP 150°C/W
   8-pin plastic DIP 105°C/W
   8-pin plastic SO 160°C/W
   14-pin plastic DIP 80°C/W
   16-pin plastic SO 90°C/W
3. Output may be shorted to ground at V_S=±15V, T_A=25°C. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_S=±15V, unless otherwise specified. [1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A NE/SA5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			0.5	2		0.5	4	mV
		Over temperature			3			5	mV
$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Offset current			10	200		20	300	nA
		Over temperature			500			400	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_B	Input current			400	800		500	1500	nA
		Over temperature			1500			2000	nA
$\Delta I_B/\Delta T$				5			5		nA/°C
I_{CC}	Supply current			4	6.5		4	8	mA
	per op amp	Over temperature			9			10	mA
V_{CM}	Common mode input range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	µV/V
A_{VOL}	Large-signal voltage gain	R_L≥600Ω, V_O=±10V	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
V_{OUT}	Output swing	R_L≥600Ω	±12	±13		±12	±13		V
		Over temperature	±10	±12		±10	±12		V
		R_L≥600Ω, V_S=±18V	±15	±16		±15	±16		V
		R_L≥2kΩ	±13	±13.5		±13	±13.5		V
		Over temperature	±12	±12.5		±12	±12.5		V
R_{IN}	Input resistance		50	100		30	100		kΩ
I_{SC}	Output short circuit current			38			38		mA

NOTES:
1. For NE5533/5533A/5534/5534A, T_{MIN} = 0°C, T_{MAX} = 70°C
2. For SE5534/5534A, T_{MIN} = -55°C, T_{MAX} = +125°C
3. For SA5534/5534A, T_{MIN} = -40°C, T_{MAX} = +125°C

AC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_S=±15V, unless otherwise specified.

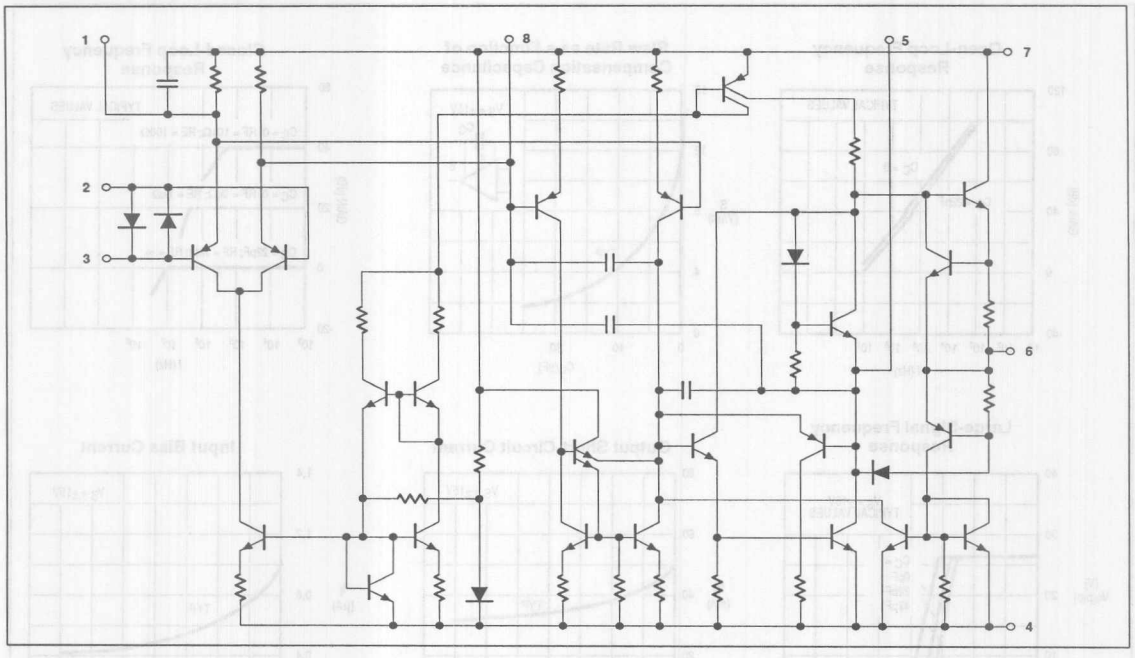
SYMBOL	PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A NESA5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_{OUT}	Output resistance	A_V=30dB closed-loop f=10kHz, R_L=600Ω, C_C=22pF		0.3			0.3		Ω
	Transient response	Voltage-follower, V_{IN}=50mV R_L=600Ω, C_C=22pF, C_L=100pF							
t_R	Rise time			20			20		ns
	Overshoot			20			20		%
	Transient response	V_{IN}=50mV, R_L=600Ω C_C=47pF, C_L=500pF							
t_R	Rise time			50			50		ns
	Overshoot			35			35		%
A_V	Gain	f=10kHz, C_C=0 f=10kHz, C_C=22pF		6 2.2			6 2.2		V/mV V/mV
GBW	Gain bandwidth product	C_C=22pF, C_L=100pF		10			10		MHz
SR	Slew rate	C_C=0 C_C=22pF		13 6			13 6		V/µs V/µs
	Power bandwidth	V_{OUT}=±10V, C_C=0 V_{OUT}=±10V, C_C=22pF V_{OUT}=±14V, R_L=600Ω C_C=22pF, V_{CC}=±18V		200 95 70			200 95 70		kHz kHz kHz

ELECTRICAL CHARACTERISTICS

TA=25°C, V_S = 15V, unless otherwise specified.

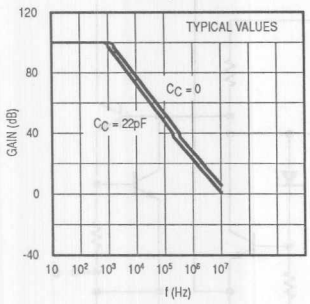
SYMBOL	PARAMETER	TEST CONDITIONS	5533/5534			5533A/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{NOISE}	Input noise voltage	f_O=30Hz f_O=1kHz		7 4			5.5 3.5	7 4.5	nV/√Hz nV/√Hz
I_{NOISE}	Input noise current	f_O=30Hz f_O=1kHz		2.5 0.6			1.5 0.4		pA/√Hz pA/√Hz
	Broadband noise figure	f=10Hz-20kHz, R_S=5kΩ					0.9		dB
	Channel separation	f=1kHz, R_S=5kΩ		110			110		dB

EQUIVALENT SCHEMATIC

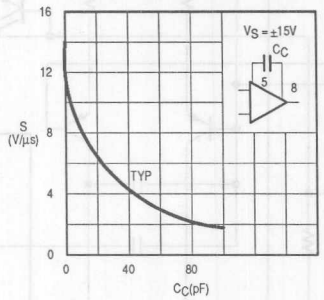


TYPICAL PERFORMANCE CHARACTERISTICS

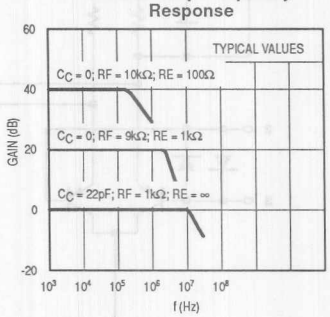
Open-Loop Frequency Response



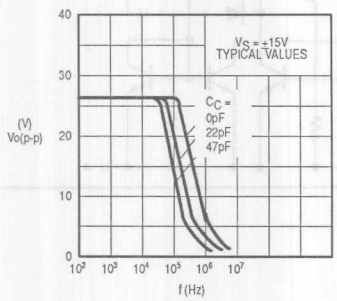
Slew Rate as a Function of Compensation Capacitance



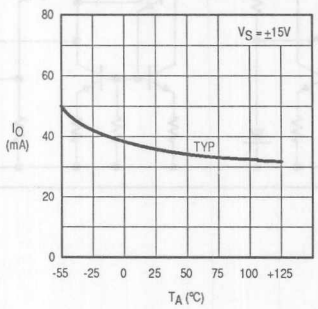
Closed-Loop Frequency Response



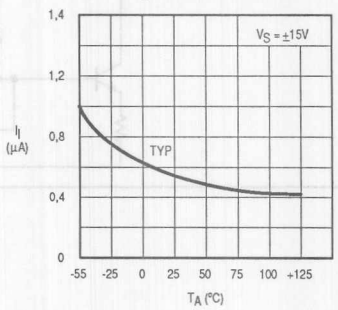
Large-Signal Frequency Response



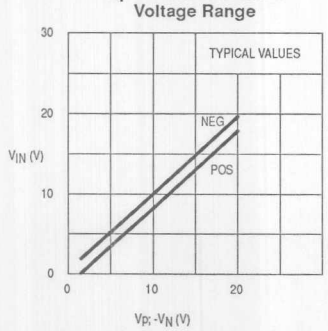
Output Short-Circuit Current



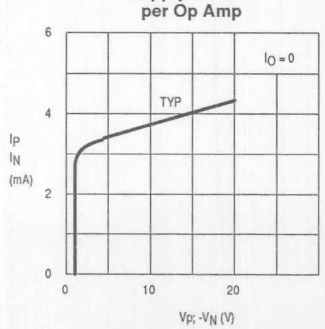
Input Bias Current



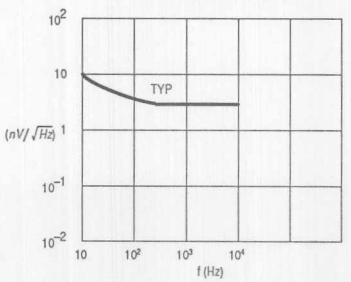
Input Commom-Mode Voltage Range



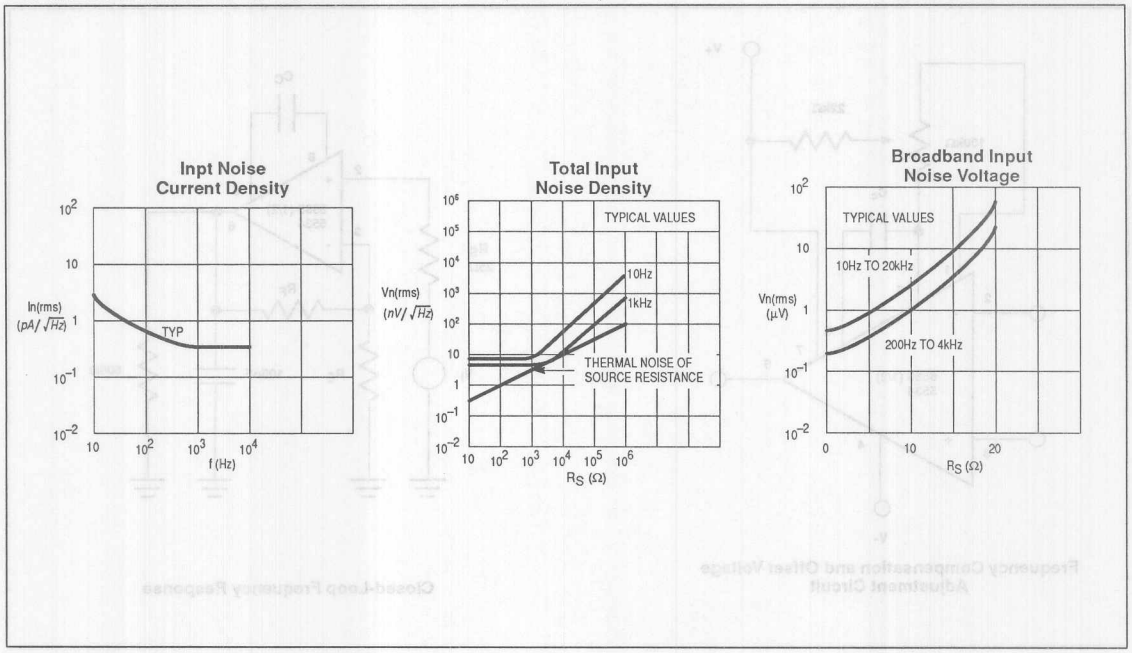
Supply Current per Op Amp



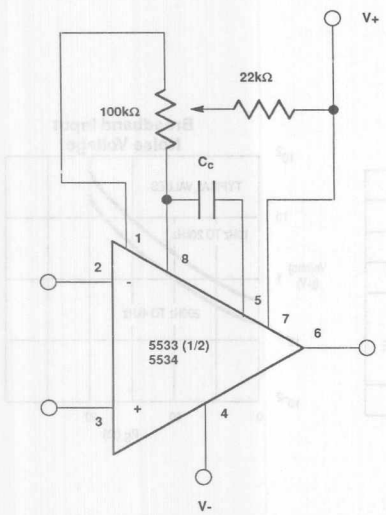
Input Noise Voltage Density



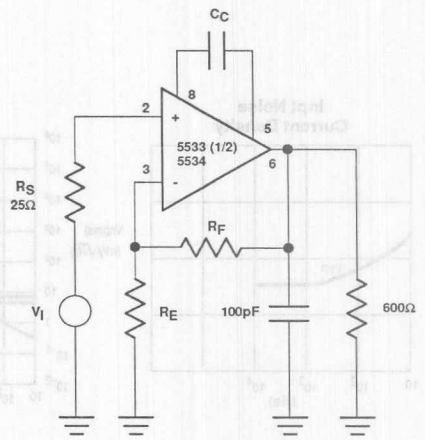
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TEST LOAD CIRCUITS

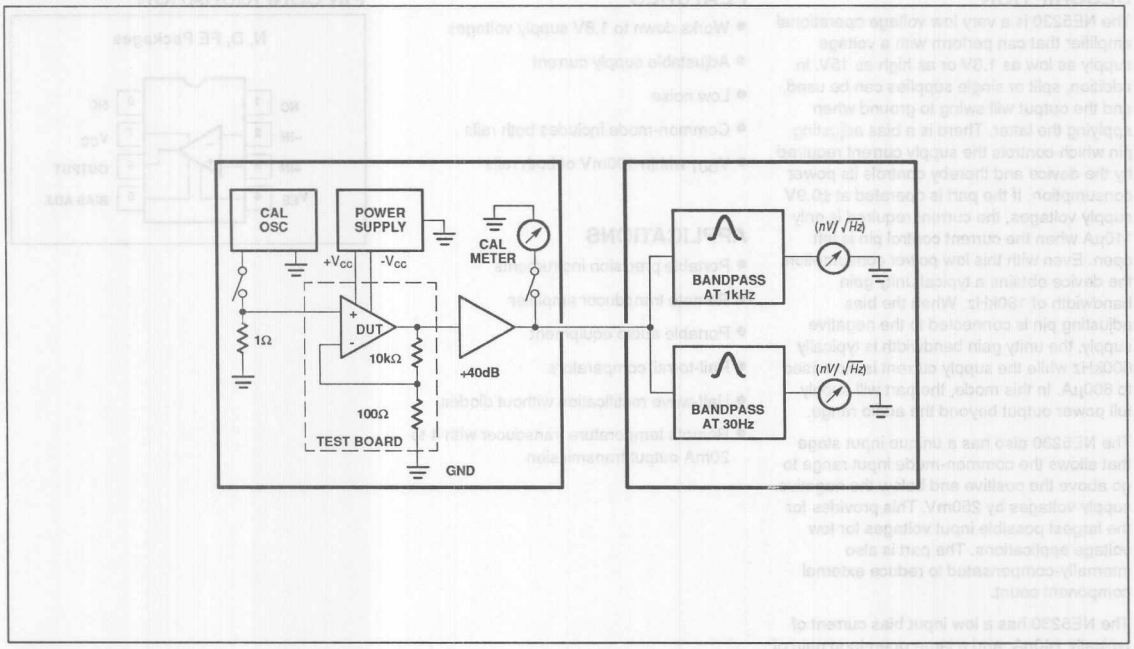


Frequency Compensation and Offset Voltage Adjustment Circuit



Closed-Loop Frequency Response

NOISE TEST BLOCK DIAGRAM



Low voltage operational amplifier NE/SA5230

DESCRIPTION

The NE5230 is a very low voltage operational amplifier that can perform with a voltage supply as low as 1.8V or as high as 15V. In addition, split or single supplies can be used, and the output will swing to ground when applying the latter. There is a bias adjusting pin which controls the supply current required by the device and thereby controls its power consumption. If the part is operated at ±0.9V supply voltages, the current required is only 110μA when the current control pin is left open. Even with this low power consumption, the device obtains a typical unity gain bandwidth of 180kHz. When the bias adjusting pin is connected to the negative supply, the unity gain bandwidth is typically 600kHz while the supply current is increased to 600μA. In this mode, the part will supply full power output beyond the audio range.

The NE5230 also has a unique input stage that allows the common-mode input range to go above the positive and below the negative supply voltages by 250mV. This provides for the largest possible input voltages for low voltage applications. The part is also internally-compensated to reduce external component count.

The NE5230 has a low input bias current of typically ±40nA, and a large open-loop gain of 125dB. These two specifications are beneficial when using the device in transducer applications. The large open-loop gain gives very accurate signal processing because of the large "excess" loop gain in a closed-loop system.

The output stage is a class AB type that can swing to within 100mV of the supply voltages for the largest dynamic range that is needed in many applications. The NE5230 is ideal for portable audio equipment and remote transducers because of its low power consumption, unity gain bandwidth, and 30nV/$\sqrt{Hz}$ noise specification.

FEATURES

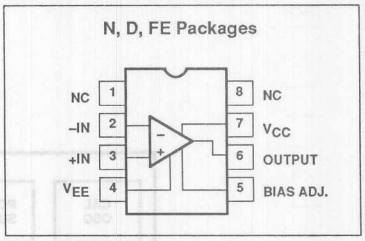
- Works down to 1.8V supply voltages
- Adjustable supply current
- Low noise
- Common-mode includes both rails
- V_{OUT} within 100mV of both rails

APPLICATIONS

- Portable precision instruments
- Remote transducer amplifier
- Portable audio equipment
- Rail-to-rail comparators
- Half-wave rectification without diodes
- Remote temperature transducer with 4 to 20mA output transmission

PIN CONFIGURATION

N, D, FE Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5230D
8-Pin Plastic DIP	0 to +70°C	NE5230N
8-Pin Plastic SO	-40°C to +85°C	SA5230D
8-Pin Ceramic DIP	-40°C to +85°C	SA5230FE
8-Pin Plastic DIP	-40°C to +85°C	SA5230N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Single supply voltage	18	V
V_S	Dual supply voltage	±9	V
V_{IN}	Input voltage[1]	±9 (18)	V
	Differential input voltage[1]	$\pm V_S$	V
V_{CM}	Common-mode voltage (positive)	V_{CC}+0.5	V
V_{CM}	Common-mode voltage (negative)	V_{EE}-0.5	V
P_D	Power dissipation[2]	500	mW
T_J	Operating junction temperature[2]	150	°C
	80Output short-circuit duration to either power supply pin[2, 3]	Indefinite	s
T_{STG}	Storage temperature	-65 to 150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Can exceed the supply voltages when $V_S \leq \pm 7.5V$ (15V).
2. The maximum operating junction temperature is 150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions. Derate above 25°C at the following rates:
   FE package at 6.7mW/°C
   N package at 9.5mW/°C
   D package at 6.25mW/°C
3. Momentary shorts to either supply are permitted in accordance to transient thermal impedance limitations determined by the package and device mounting conditions.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNIT
Single supply voltage	1.8 to 15	V
Dual supply voltage	±0.9 to ±7.5	V
Common-mode voltage (positive)	V_{CC}+0.25	V
Common-mode voltage (negative)	V_{EE}-0.25	V
Temperature		
NE grade	0 to 70	°C
SA grade	-40 to 85	°C

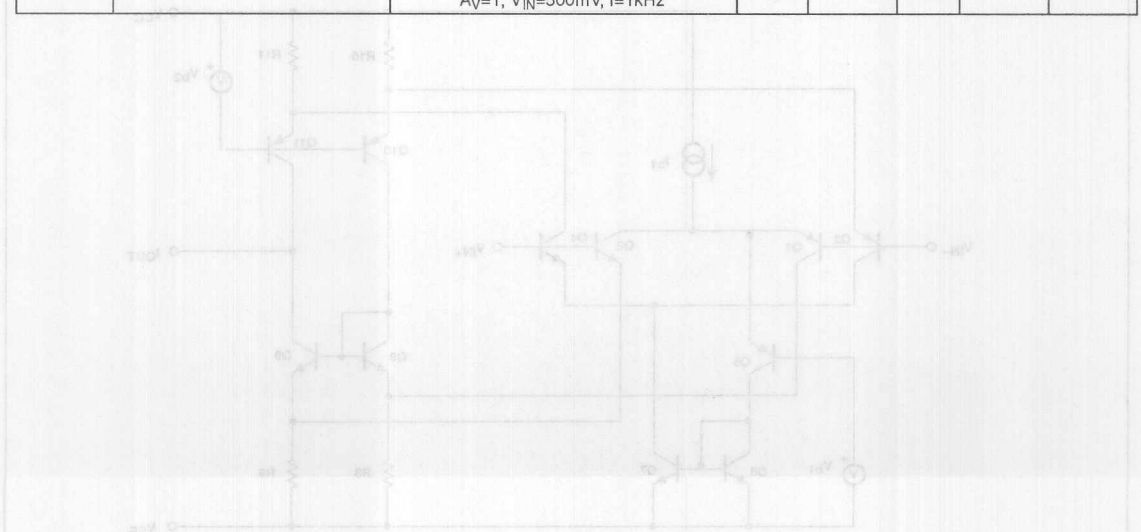
DC AND AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $\pm 0.9V \leq V_S \leq +7.5V$ or equivalent single supply, R_L=10kΩ, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER		TEST CONDITIONS		BIAS	NE/SA5230			UNIT
						Min	Typ	Max	
V_{OS}	Offset voltage		T_A=25°C		Any		0.4	3	mV
					Any		3	4	mV
V_{OS}	Drift				Any		2	5	µV/°C
I_{OS}	Offset current		T_A=25°C		High		3	50	nA
			T_A=25°C		Low		3	30	nA
					High			100	nA
					Low			60	nA
I_{OS}	Drift				High		0.5	1.4	nA/°C
					Low		0.3	1.4	nA/°C
I_B	Bias current		T_A=25°C		High		40	150	nA
			T_A=25°C		Low		20	60	nA
					High			200	nA
					Low			150	nA
I_B	Drift				High		2	4	nA/°C
					Low		2	4	nA/°C
I_S	Supply current		V_S=±0.9V	T_A=25°C	Low		110	160	µA
				T_A=25°C	High		600	750	µA
					Low			250	µA
					High			800	µA
			V_S=±7.5V	T_A=25°C	Low		320	550	µA
				T_A=25°C	High		1.1	1.6	µA
					Low			600	µA
					High			1.7	µA
V_{CM}	Common-mode input range		V_{OS}≤6mV, T_A=25°C		Any	V^- -0.25		V^+ +0.25	V
					Any	V^-		V^+	V
CMRR	Common-mode rejection ratio		V_S=±7.5V	R_S=10kΩ, V_{CM}=±7.5V, T_A=25°C	Any	85	95		dB
				R_S=10kΩ, V_{CM}=±7.5V	Any	80			dB
PSRR	Power supply rejection ratio		T_A=25°C		High	90	105		dB
			T_A=25°C		Low	85	95		dB
					High	75			dB
					Low	80			dB
I_L	Load current	source	V_S=±7.5V		Any	4	10		mA
		sink	V_S=±7.5V		Any	5	15		mA
		source	V_S=±7.5V		Any	1	5		mA
		sink	V_S=±7.5V		Any	2	6		mA
		source	V_S=±0.9V, T_A=25°C		High	4	6		mA
		sink	V_S=±0.9V, T_A=25°C		High	5	7		mA
		source	V_S=±7.5V, T_A=25°C		High		16		mA
		sink	V_S=±7.5V, T_A=25°C		High		32		mA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS		BIAS	NE/SA5230			UNIT
					Min	Typ	Max	
A_{VOL}	Large-signal open-loop gain	V_S=±7.5V	R_L=10kΩ, T_A=25°C	High	120	2000		V/mV
			R_L=10kΩ, T_A=25°C	Low	60	750		V/mV
				High	100	800		V/mV
				Low	50	800		V/mV
V_{OUT}	Output voltage swing	V_S=±0.9V	T_A=25°C +SW	Any	750	800		mV
			T_A=25°C -SW	Any	750	800		mV
			+SW	Any	700			mV
			-SW	Any	700			mV
		V_S=±7.5V	T_A=25°C +SW	Any	7.30	7.35		V
			T_A=25°C -SW	Any	-7.32	-7.35		V
			+SW	Any	7.25	7.30		V
			-SW	Any	-7.30	-7.35		V
SR	Slew rate	T_A=25°C		High		0.25		V/µs
		T_A=25°C		Low		0.09		V/µs
BW	Inverting unity gain bandwidth	C_L=100pF, T_A=25°C		High		0.6		MHz
		C_L=100pF, T_A=25°C		Low		0.25		MHz
θ_M	Phase margin	C_L=100pF, T_A=25°C		Any		70		Deg.
t_S	Settling time	C_L=100pF, 0.1%		High		2		µs
		C_L=100pF, 0.1%		Low		5		µs
V_{INN}	Input noise	R_S=0Ω, f=1kHz		High		30		nV/√Hz
		R_S=0Ω, f=1kHz		Low		60		nV/√Hz
THD	Total Harmonic Distortion	V_S=±7.5V A_V=1, V_{IN}=500mV, f=1kHz		High		0.003		%
		V_S=±0.9V A_V=1, V_{IN}=500mV, f=1kHz		High		0.002		%



THEORY OF OPERATION

Input Stage

Operational amplifiers which are able to function at minimum supply voltages should have input and output stage swings capable of reaching both supply voltages within a few millivolts in order to achieve ease of quiescent biasing and to have maximum input/output signal handling capability. The input stage of the NE5230 has a common-mode voltage range that not only includes the entire supply voltage range, but also allows either supply to be exceeded by 250mV without increasing the input offset voltage by more than 6mV. This is unequalled by any other operational amplifier today.

In order to accomplish the feat of rail-to-rail input common-mode range, two emitter-coupled differential pairs are placed in parallel so that the common-mode voltage of one can reach the positive supply rail and the other can reach the negative supply rail. The simplified schematic of Figure 1 shows how the complementary emitter-coupler transistors are configured to form the basic input stage cell. Common-mode input signal voltages in the range from 0.8V above V_{EE} to V_{CC} are handled completely by the NPN pair, Q3 and Q4, while common-mode input signal voltages in the range of V_{EE} to 0.8V above V_{EE} are processed only by the PNP pair, Q1 and Q2. The intermediate range of input voltages requires that both the NPN and PNP pairs are operating. The collector currents of the input transistors are summed by the current combiner circuit composed of transistors Q8 through Q11 into one output current. Transistor Q8 is connected as a diode to ensure that the outputs of Q2 and Q4 are properly subtracted from those of Q1 and Q3.

The input stage was designed to overcome two important problems for rail-to-rail capability. As the common-mode voltage moves from the range where only the NPN pair was operating to where both of the input pairs were operating, the effective transconductance would change by a factor of two. Frequency compensation for the ranges where one input pair was operating would, of course, not be optimal for the range where both pairs were operating. Secondly, fast changes in the common-mode voltage would abruptly saturate and restore the emitter current sources, causing transient distortion. These problems were overcome by assuring that only the input transistor pair which is able to function properly is active. The NPN pair is normally activated by the current source I_{B1} through Q5 and the current mirror Q6 and Q7, assuming the PNP pair is non-conducting. When the common-mode input voltage passes below the reference voltage, V_{B1}=0.8V at the base of Q5, the emitter current is gradually steered toward the PNP pair, away from the NPN pair. The transfer of the emitter currents between the complementary input pairs occurs in a voltage range of about 120mV around the reference voltage V_{B1}. In this way the sum of the emitter currents for each of the NPN and PNP transistor pairs is kept constant; this ensures that the transconductance of the parallel combination will be constant, since the transconductance of bipolar transistors is proportional to their emitter currents.

An essential requirement of this kind of input stage is to minimize the changes in input offset voltage between that of the NPN and PNP transistor pair which occurs when the input common-mode voltage crosses the internal reference voltage, V_{B1}. Careful circuit layout with a cross-coupled quad for each input pair has yielded a typical input offset voltage of less than 0.3mV and a change in the input offset voltage of less than 0.1mV.

Output Stage

Processing output voltage swings that nominally reach to less than 100mV of either supply voltage can only be achieved by a pair of complementary common-emitter connected transistors. Normally, such a configuration causes complex feed-forward signal paths that develop by combining biasing and driving which can be found in previous low supply voltage designs. The unique output stage of the NE5230 separates the functions of driving and biasing, as shown in the simplified schematic of Figure 2, and has the advantage of a shorter signal path which leads to increasing the effective bandwidth.

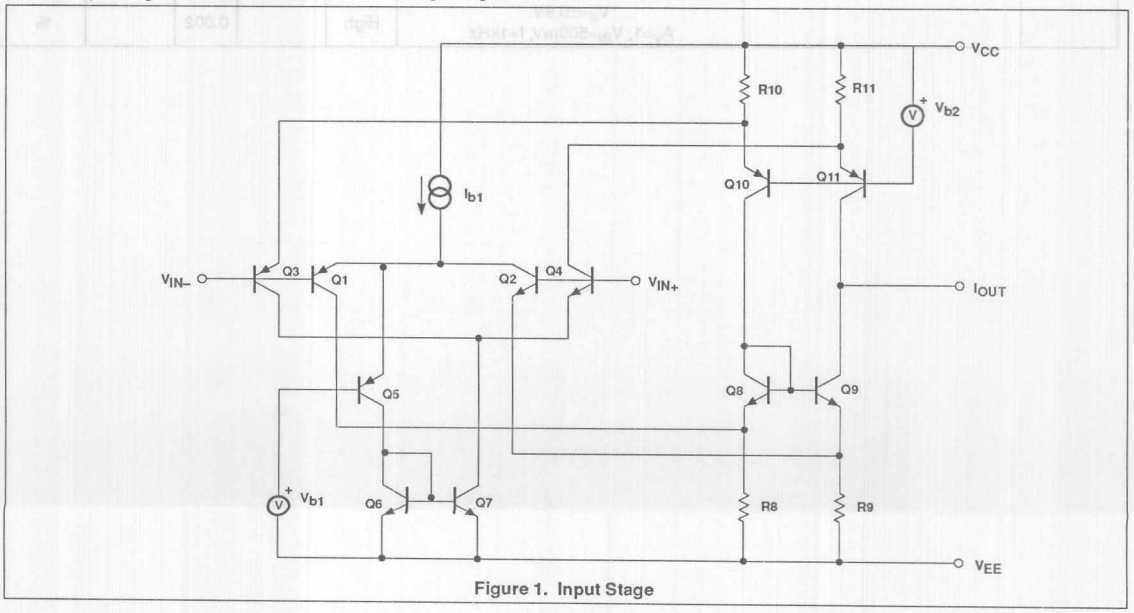


Figure 1. Input Stage

This output stage consists of two parts: the Darlington output transistors and the class AB control regulator. The output transistor Q3 connected with the Darlington transistors Q4 and Q5 can source up to 10mA to an output load. The output of NPN Darlington connected transistors Q1 and Q2 together are able to sink an output current of 10mA. Accurate and efficient class AB control is necessary to insure that none of the output transistors are ever completely cut off. This is accomplished by the differential amplifier (formed by Q8 and Q9) which controls the biasing of the output transistors. The differential amplifier compares the summed voltages across two diodes, D1 and D2, at the base of Q8 with the summed voltages across the base-emitter diodes of the output transistors Q1 and Q3. The base-emitter voltage of Q3 is converted into a current by Q6 and R6 and reconverted into a voltage across the base-emitter diode of Q7 and R7. The summed voltage across the base-emitter diodes of the output transistors Q3 and Q1 is proportional to the logarithm of the product of the push and pull currents I_{OP} and I_{ON}, respectively. The combined voltages across diodes D1 and D2 are proportional to the logarithm of the square of the reference current I_{B1}. When the diode characteristics and temperatures of the pairs Q1, D1 and Q3, Q2 are equal, the relation $I_{OP} \times I_{ON} = I_{B1} \times I_{B1}$ is satisfied.

Separating the functions of biasing and driving prevents the driving signals from becoming delayed by the biasing circuit. The output Darlington transistors are directly accessible for in-phase driving signals on the bases of Q5 and Q2. This is very important for simple high-frequency compensation. The output transistors can be high-frequency compensated by Miller capacitors CM1A and CM1B connected from the collectors to the bases of the output Darlington transistors.

A general-purpose op amp of this type must have enough open-loop gain for applications when the output is driving a low resistance load. The NE5230 accomplishes this by inserting an intermediate common-emitter stage between the input and output stages. The three stages provide a very large gain, but the op amp now has three natural dominant poles — one at the output of each common-emitter stage. Frequency compensation is implemented with a simple scheme of nested, pole-splitting Miller integrators. The Miller capacitors CM1A and CM1B are the first part of the nested structure, and provide compensation for the output and intermediate stages. A second pair of Miller integrators provide pole-splitting compensation for the pole from the input stage and the pole resulting from the compensated combination of poles from the intermediate and output stages. The result is a stable, internally-compensated op amp with a phase margin of 70 degrees.

THERMAL CONSIDERATIONS

When using the NE5230, the internal power dissipation capabilities of each package should be considered. Signetics does not recommend operation at die temperatures above 110°C in the SO package because of its inherently smaller package mass. Die temperatures of 150°C can be tolerated in all the other packages. With this in mind, the following equation can be used to estimate the die temperature:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

Where

$T_A \equiv Ambient Temperature$
$T_J = Die\ Temperature$
$P_D \equiv Power\ Dissipation = (I_{CC} \times V_{CC})$
$\theta_{JA} \equiv Package thermal resistance = 270°C/W$ for $SO-8$ *in PC board mounting*

See the packaging section for information regarding other methods of mounting.

θ_{JA}=100°C/W for the plastic DIP;
θ_{JA}=110°C/W for the ceramic DIP.

The maximum supply voltage for the part is 15V and the typical supply current is 1.1mA (1.6mA max). For operation at supply

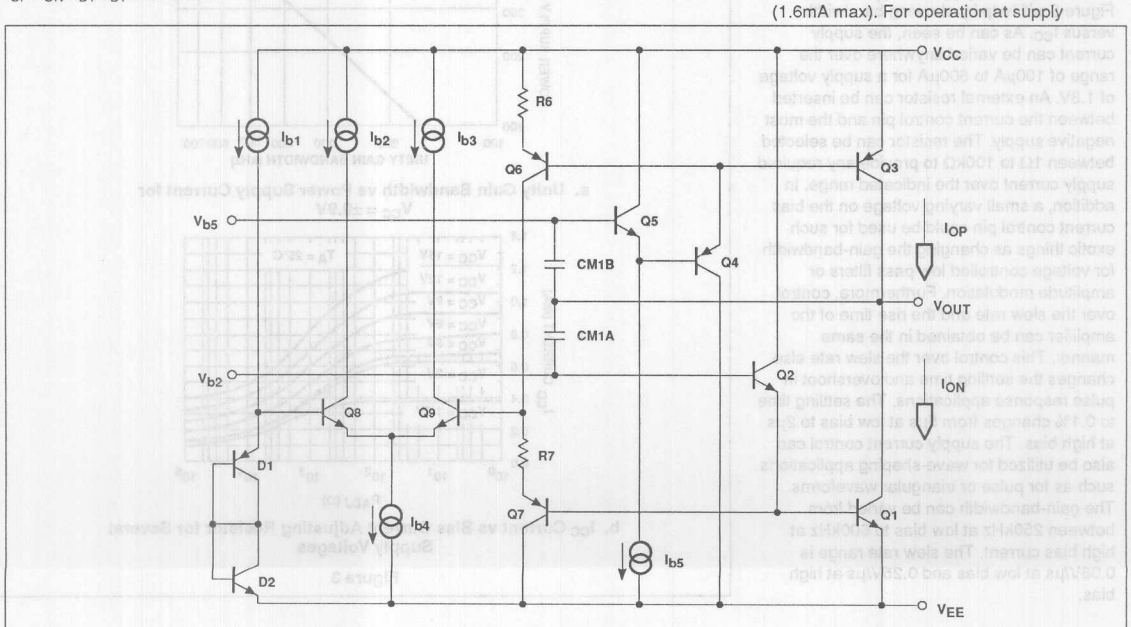


Figure 2. Output Stage

voltages other than the maximum, see the data sheet for I_{CC} versus V_{CC} curves. The supply current is somewhat proportional to temperature and varies no more than 100μA between 25°C and either temperature extreme.

Operation at higher junction temperatures than that recommended is possible but will result in lower MTBF (Mean Time Between Failures). This should be considered before operating beyond recommended die temperature because of the overall reliability degradation.

DESIGN TECHNIQUES AND APPLICATIONS

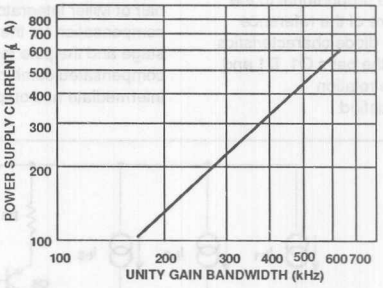
The NE5230 is a very user-friendly amplifier for an engineer to design into any type of system. The supply current adjust pin (Pin 5) can be left open or tied through a pot or fixed resistor to the most negative supply (i.e., ground for single supply or to the negative supply for split supplies). The minimum supply current is achieved by leaving this pin open. In this state it will also decrease the bandwidth and slew rate. When tied directly to the most negative supply, the device has full bandwidth, slew rate and I_{CC}. The programming of the current-control pin depends on the trade-offs which can be made in the designer's application. The graph in Figure 3 will help by showing bandwidth versus I_{CC}. As can be seen, the supply current can be varied anywhere over the range of 100μA to 600μA for a supply voltage of 1.8V. An external resistor can be inserted between the current control pin and the most negative supply. The resistor can be selected between 1Ω to 100kΩ to provide any required supply current over the indicated range. In addition, a small varying voltage on the bias current control pin could be used for such exotic things as changing the gain-bandwidth for voltage controlled low pass filters or amplitude modulation. Furthermore, control over the slew rate and the rise time of the amplifier can be obtained in the same manner. This control over the slew rate also changes the settling time and overshoot in pulse response applications. The settling time to 0.1% changes from 5μs at low bias to 2μs at high bias. The supply current control can also be utilized for wave-shaping applications such as for pulse or triangular waveforms. The gain-bandwidth can be varied from between 250kHz at low bias to 600kHz at high bias current. The slew rate range is *0.08V/μs at low bias and 0.25V/μs at high bias.*

The full output power bandwidth range for V_{CC} equals 2V, is above 40kHz for the maximum bias current setting and greater than 10kHz at the minimum bias current setting.

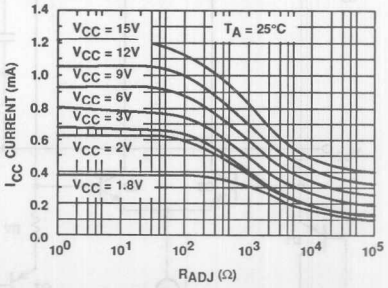
If extremely low signal distortion (<0.05%) is required at low supply voltages, exclude the common-mode crossover point (V_{B1}) from the common-mode signal range. This can be accomplished by proper bias selection or by using an inverting amplifier configuration.

Most single supply designs necessitate that the inputs to the op amp be biased between V_{CC} and ground. This is to assure that the input signal swing is within the working common-mode range of the amplifier. This leads to another helpful and unique property of the NE5230 that other CMOS and bipolar low voltage parts cannot achieve. It is the simple fact that the input common-mode voltage can go beyond either the positive or negative supply voltages. This benefit is made very clear in a non-inverting voltage-follower configuration. This is shown in Figure 4 where the input sine wave allows an undistorted output sine wave which will swing less than 100mV of either supply voltage. Many competitive parts will show severe clipping caused by input common-mode limitations. The NE5230 in this configuration offers more freedom for quiescent biasing of the inputs close to the positive supply rail where similar op amps would not allow signal processing.

There are not as many considerations when designing with the NE5230 as with other devices. Since the NE5230 is internally-compensated and has a unity gain-bandwidth of 600kHz, board layout is not so stringent as for very high frequency devices such as the NE5205. The output capability of the NE5230 allows it to drive relatively high capacitive loads and small resistive loads. The power supply pins should be decoupled with a low-pass RC network as close to the supply pins as possible to eliminate 60Hz and other external power line noise, although the power supply rejection ratio (PSRR) for the part is very high. The pinout for the NE5230 is the same as the



a. Unity Gain Bandwidth vs Power Supply Current for V_{CC} = ±0.9V



b. I_{CC} Current vs Bias Current Adjusting Resistor for Several Supply Voltages

Figure 3

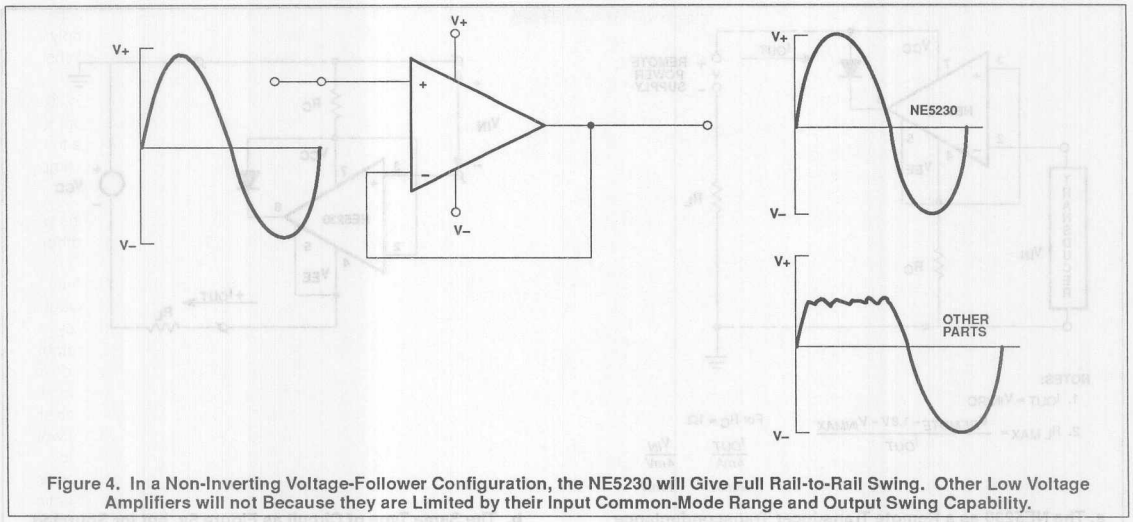


Figure 4. In a Non-Inverting Voltage-Follower Configuration, the NE5230 will Give Full Rail-to-Rail Swing. Other Low Voltage Amplifiers will not Because they are Limited by their Input Common-Mode Range and Output Swing Capability.

standard single op amp pinout with the exception of the bias current adjusting pin.

REMOTE TRANSDUCER WITH CURRENT TRANSMISSION

There are many ways to transmit information along two wires, but current transmission is the most beneficial when the sensing of remote singals is the aim. It is further enhanced in the form of 4 to 20mA information which is used in many control-type systems. This method of transmission provides immunity from line voltage drops, large load resistance variations, and voltage noise pickup. The zero reference of 4mA not only can show if there is a break in the line when no current is flowing, but also can power the transducer at the remote location. Usually the transducer itself is not equipped to provide for the current transmission. The unique features of the NE5230 can provide high output current capability coupled with low power consumption. It can be recotely connected to the transducer to create a current loop with minimal external components. The circuit for this is shown in Figure 5. Here, the part is configured as a voltage-to-current, or transconductance amplifier. This is a novel circuit that takes advantage of the NE5230's large open-loop gain. In AC applications, the load current will decrease as the open-loop gain rolls off in magnitude. The low offset voltage and current sinking capabilities of the NE5230 must also be considered in this application.

The NE5230 circuit shown in Figure 5 is a pseudo transistor configuration. The inverting input is equivalent to the "base," the point where V_{EE} and the non-inverting input meet is the "emitter," and the connection after the output diode meets the V_{CC} pin is the collector. The output diode is essential to keep the output from saturating in this configuration. From here it can be seen that the base and emitter form a voltage-follower and the voltage present at R_C must equal the input voltage present at the inverting input. Also, the emitter and collector form a current-follower and the current flowing through R_C is equivalent to the current through R_L and the amplifier. This sets up the current loop. Therefore, the following equation can be formulated for the working current transmission line. The load current is:

$$I_L = V_{IN}/R_C \quad (2)$$

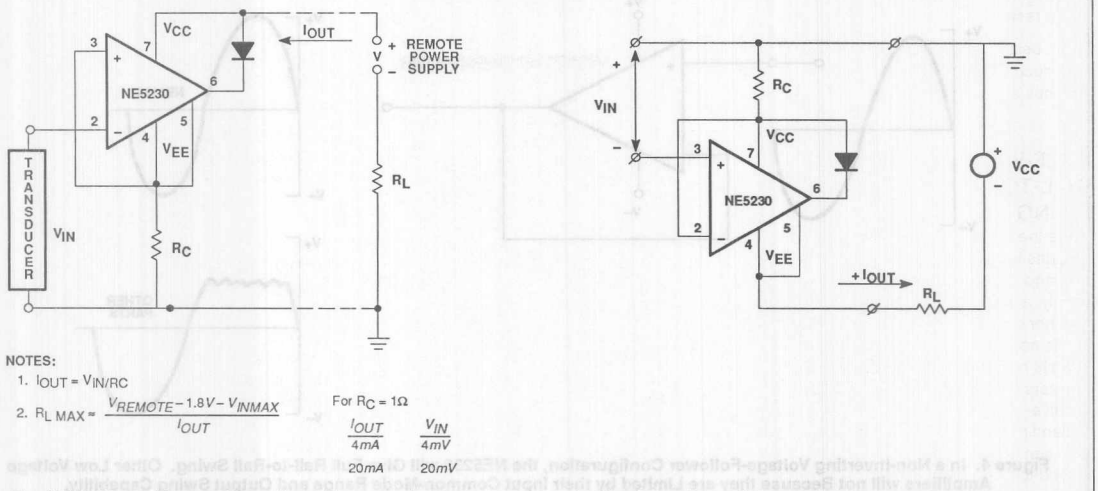
and proportional to the input voltage for a set R_C. Also, the current is constant no matter what load resistance is used while within the operating bandwidth range of the op amp. When the NE5230's supply voltage falls past a certain point, the current cannot remain constant. This is the "voltage compliance" and is very good for this application because of the near rail output voltage. The equation that determines the voltage compliance as well as the largest possible load resistor for the NE5230 is as follows:

$$R_{L\,max} = [V_{remote\ supply}) - V_{CC\,min} - V_{IN\,max}]/I_L \quad (3)$$

Where $V_{CC\,min}$ is the worst-case power supply voltage (approximately 1.8V) that will still keep the part operational. As an example, when using a 15V remote power supply, a current sensing resistor of 1Ω, and an input voltage (V_{IN}) of 20mV, the output current (I_L) is 20mA. Furthermore, a load resistance of zero to approximately 650Ω can be inserted in the loop without any change in current when the bias current-control pin is tied to the negative supply pin. The voltage drop across the load and line resistance will not affect the NE5230 because it will operate down to 1.8V. With a 15V remote supply, the voltage available at the amplifier is still enough to power it with the maximum 20mA output into the 650Ω load.

What this means is that several instruments, such as a chart recorder, a meter, or a controller, as well as a long cable, can be connected in series on the loop and still obtain accurate readings if the total resistance does not exceed 650Ω. Furthermore, any variation of resistance in this range will not change the output current.

Any voltage output type transducer can be used, but one that does not need external DC voltage or current excitation to limit the maximum possible load resistance is preferable. Even this problem can be surmounted if the supply power needed by the transducer is compatible with the NE5230. The power goes up the line to the transducer and amplifier while the transducer signal is sent back via the current output of



a. The NE5230 as a Remote Transducer Transconductance Amp With 4-20mA Current Transmission Output Capability

b. The Same Type of Circuit as Figure 5a, but for Sourcing Current to the Load

Figure 5

the NE5230 transconductance configuration. The voltage range on the input can be changed for transducers that produce a large output by simply increasing the current sense resistor to get the corresponding 4 to 20mA output current. If a very long line is used which causes high line resistance, a current repeater could be inserted into the line. The same configuration of Figure 5 can be used with exception of a resistor across the input and line ground to convert the current back to voltage. Again, the current sensing resistor will set up the transconductance and the part will receive power from the line.

TEMPERATURE TRANSDUCER

A variation on the previous circuit makes use of the supply current control pin. The voltage present at this pin is proportional to absolute temperature (PTAT) because it is produced by the amplifier bias current through an internal resistor divider in a PTAT cell. If the control pin is connected to the input pin, the NE5230 itself can be used as a temperature transducer. If the center tap of a resistive pot is connected to the control pin with one side to ground and the other to the inverting input, the voltage can be changed to give different temperature versus output current conditions (see Figure 6). For additional control, the output current is still proportional to the input

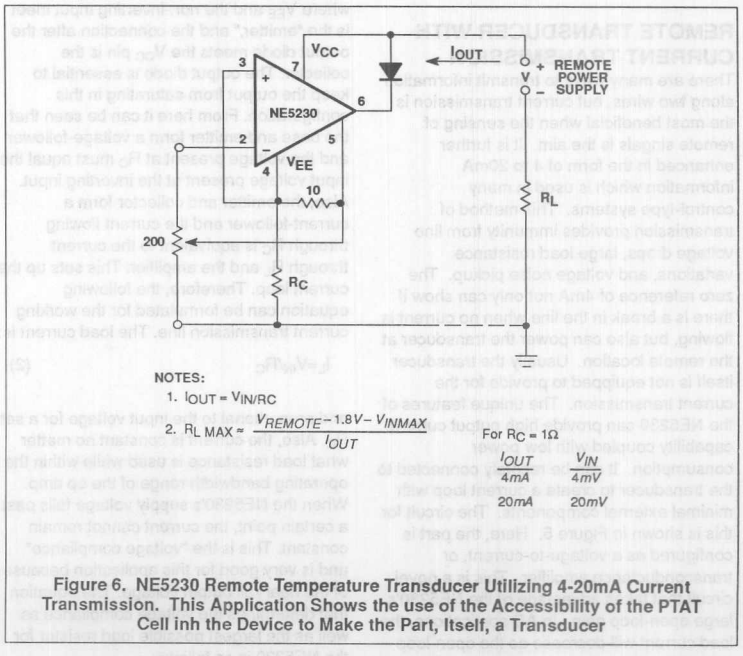


Figure 6. NE5230 Remote Temperature Transducer Utilizing 4-20mA Current Transmission. This Application Shows the use of the Accessibility of the PTAT Cell inh the Device to Make the Part, Itself, a Transducer

voltage differential divided by the current sense resistor.

When using the NE5230 as a temperature transducer, the thermal considerations in the previous section must be kept in mind.

HALF-WAVE RECTIFIER WITH RAIL-TO-GROUND OUTPUT SWING

Since the NE5230 input common-mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction becomes a simple task. All that is needed are two external resistors; there is no need for diodes or matched resistors. Moreover, it can have either positive- or negative-going outputs, depending on the way the bias is arranged. This can be seen in Figure 7. Circuit (a) is biased to ground, while circuit (b) is biased to the positive supply. This rather unusual biasing does not cause any problems with the NE5230 because of the unique internal saturation detectors incorporated into the part to keep the PNP and NPN output transistors out of "hard" saturation. It is therefore relatively quick to recover from a saturated output condition. Furthermore, the device does not have parasitic current draw when the output is biased to either rail. This makes it possible to bias the NE5230 into "saturation" and obtain half-wave rectification with good recovery. The simplicity of biasing and the rail-to-ground half-sine wave swing are unique to this device. The circuit gain can be changed by the standard op amp gain equations for an inverting configuration.

It can be seen in these configurations that the op amp cannot respond to one-half of the incoming waveform. It cannot respond because the waveform forces the amplifier to swing the output beyond either ground or the positive supply rail, depending on the biasing, and, also, the output cannot disengage during this half cycle. During the other half cycle, however, the amplifier achieves a half-wave that can have a peak equal to the total supply voltage. The photographs in Figure 8 show the effect of the different biasing schemes, as well as the wide bandwidth (it works over the full audio range), that the NE5230 can achieve in this configuration.

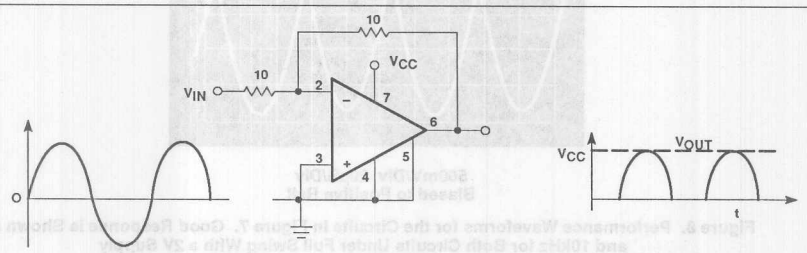
By adding another NE5230 in an inverting summer configuration at the output of the half-wave rectifier, a full-wave can be realized. The values for the input and feedback resistors must be chosen so that each peak will have equal amplitudes. A table for calculating values is included in Figure 9. The summing network combines the input signal at the half-wave and adds it to double the half-wave's output, resulting in the full-wave. The output waveform can be referenced to the supply or ground, depending on the half-wave configuration. Again, no diodes are needed to achieve the rectification.

This circuit could be used in conjunction with the remote transducer to convert a received AC output signal into a DC level at the full-wave output for meters or chart recorders that need DC levels.

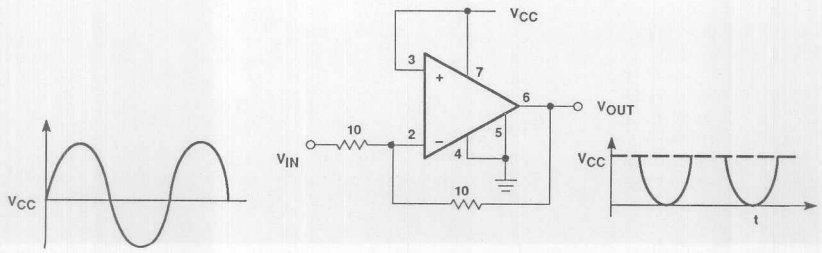
CONCLUSION

The NE5230 is a versatile op amp in its own right. The part was designed to give low voltage and low power operation without the limitations of previously available amplifiers that had a multitude of problems. The previous application examples are unique to this amplifier and save the user money by excluding various passive components that would have been needed if not for the NE5230's special input and output stages.

The NE5230 has a combination of novel specifications which allows the designer to implement it easily into existing low-supply voltage designs and to enhance their performance. It also offers the engineer the freedom to achieve greater amplifier system design goals. The low input referenced noise voltage eases the restrictions on designs where S/N ratios are important. The wide



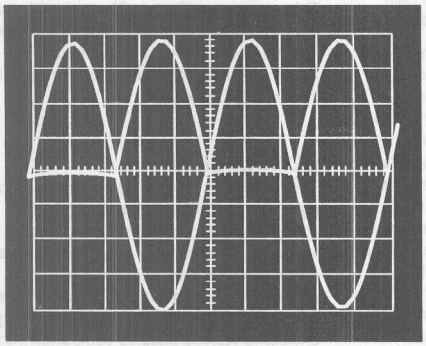
a. Rail-to-Ground Output Swing Referenced to Ground



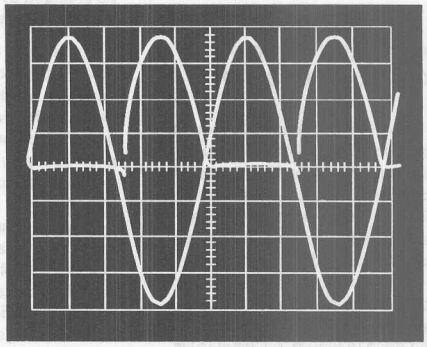
b. Negative-Going Output Referenced to V_{CC}

Figure 7. Half-Way Rectifier With Positive-Going Output Swings

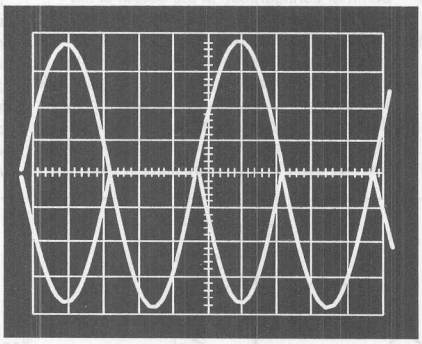
full-power bandwidth and output load handling capability allow it to fit into portable audio applications. The truly ample open-loop gain and low power consumption easily lend themselves to the requirements of remote transducer applications. The low, untrimmed typical offset voltage and low offset currents help to reduce errors in signal processing designs. The amplifier is well isolated from changes on the supply lines by its typical power supply rejection ratio of 105dB.



500mV/Div 200μS/Div
Biased to Ground

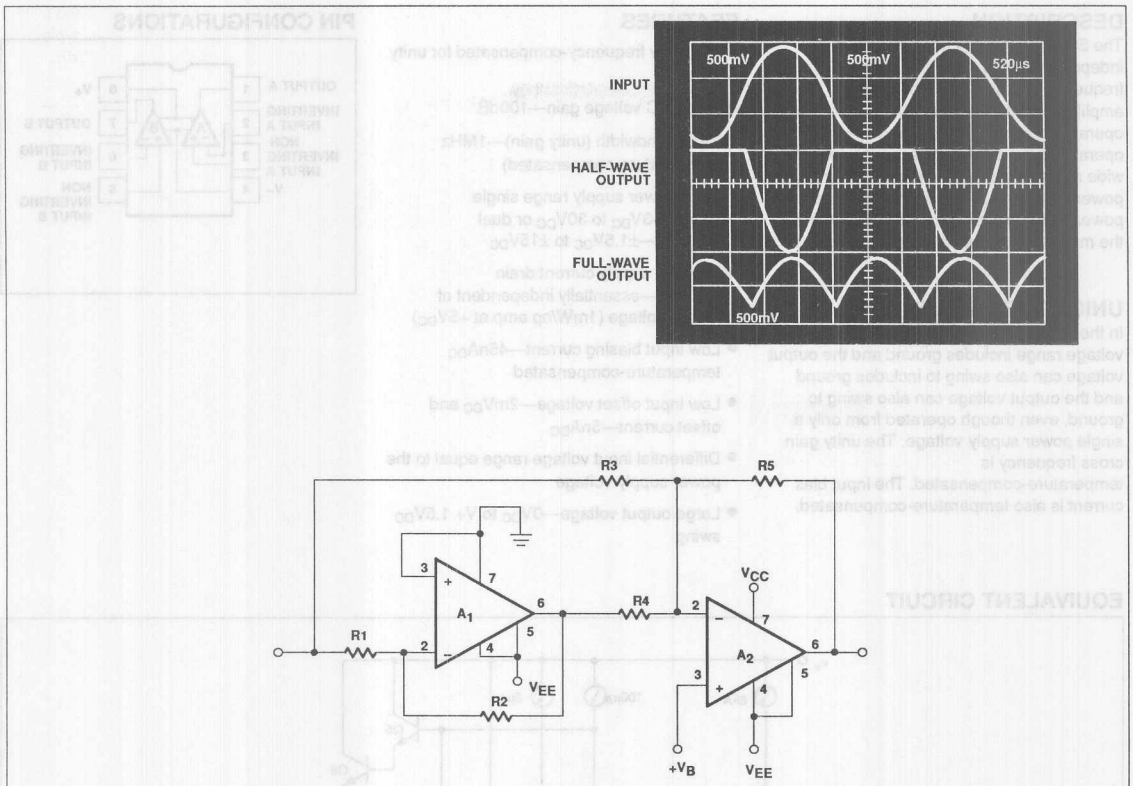


500mV/Div 20μS/Div
Biased to Ground



500mV/Div 20μS/Div
Biased to Positive Rail

Figure 8. Performance Waveforms for the Circuits in Figure 7. Good Response is Shown at 1 and 10kHz for Both Circuits Under Full Swing With a 2V Supply



NOTES:
R2 = 2 R1
R4 = R5 = R3
$+V_B$ will vary output reference.
For single supply operation V_{EE} can be grounded on A2.

Figure 9. Adding an Inverting Summer to the Input and Output of the Half-Wave will Result in Full-Wave

REFERENCES

Johan H. Huijsing, "Multi-stage Amplifier with Capacitive Nesting for Frequency Compensation," U.S. Patent Application Serial No. 602.234, filed April 19, 1984.

Bob Blauschild, "Differential Amplifier with Rail-to-Rail Capability," U.S. Patent Application Serial No. 525.181, filed August 23, 1983.

Operational Amplifiers - Characteristics and Applications, Robert G. Irvine, Prentice-Hall, Inc., Englewood Cliffs, NJ 07632, 1981.

Transducer Interface Handbook - A Guide to Analog Signal Conditioning, Edited by Daniel H. Sheingold, Analog Devices, Inc., Norwood, MA 02062, 1981.

Low power dual operational amplifiers

NE/SA/SE532/ LM158/258/358/A/2904

DESCRIPTION

The 532/358/LM2904 consists of two independent, high gain, internally frequency-compensated operational amplifiers internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible, and the low power supply current drain is independent of the magnitude of the power supply voltage.

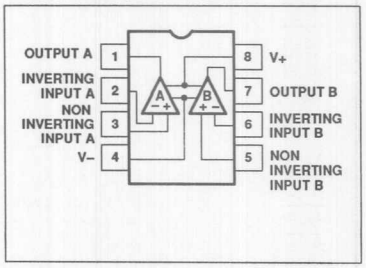
UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature-compensated. The input bias current is also temperature-compensated.

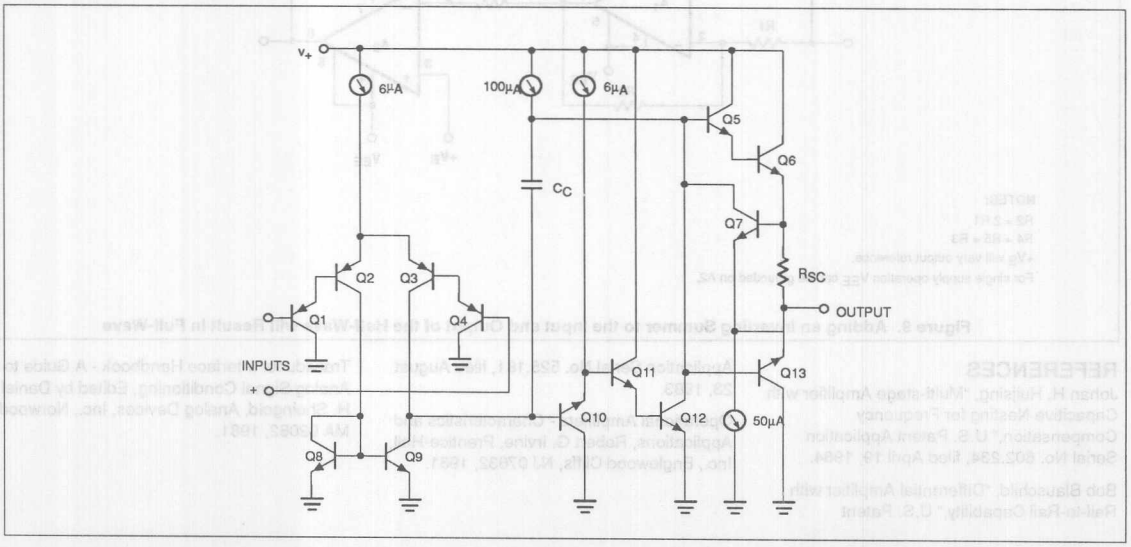
FEATURES

- Internally frequency-compensated for unity gain
- Large DC voltage gain—100dB
- Wide bandwidth (unity gain)—1MHz (temperature-compensated)
- Wide power supply range single supply—$3V_{DC}$ to $30V_{DC}$ or dual supplies—$\pm1.5V_{DC}$ to $\pm15V_{DC}$
- Very low supply current drain (400μA)—essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)
- Low input biasing current—$45nA_{DC}$ temperature-compensated
- Low input offset voltage—$2mV_{DC}$ and offset current—$5nA_{DC}$
- Differential input voltage range equal to the power supply voltage
- Large output voltage—$0V_{DC}$ to V+ $1.5V_{DC}$ swing

PIN CONFIGURATIONS



EQUIVALENT CIRCUIT



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE532D
8-Pin Plastic DIP	0 to +70°C	NE532N
8-Pin Ceramic DIP	0 to +70°C	NE532FE
8-Pin Plastic SO	-40°C to +85°C	SA532D
8-Pin Plastic DIP	-40°C to +85°C	SA532N
8-Pin Ceramic DIP	-40°C to +85°C	SA532FE
8-Pin Plastic SO	-40°C to +85°C	LM2904D
8-Pin Plastic DIP	-40°C to +85°C	LM2904N
8-Pin Ceramic DIP	-55°C to +125°C	LM158FE
8-Pin Plastic DIP	-25°C to +125°C	LM258N
8-Pin Plastic SO	-25°C to +125°C	LM258D
8-Pin Plastic SO	0 to +70°C	LM358D
8-Pin Plastic DIP	0 to +70°C	LM358N
8-Pin Plastic DIP	0 to +70°C	LM358AN
8-Pin Plastic SO	0 to +70°C	LM358AD
8-Pin Plastic DIP	-55°C to +125°C	SE532N
8-Pin Ceramic DIP	-55°C to +125°C	SE532FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage, V+	32 or ±16	V_{DC}
	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	-0.3 to +32	V_{DC}
P_D	Maximum power dissipation T_A=25°C (Still air)[1] FE package N package D package	 780 1160 780	 mW mW mW
	Output short-circuit to GND[5] V+<15 V_{DC} and T_A=25°C	 Continuous	
T_A	Operating ambient temperature range NE532/LM358/LM358A LM258 SA532/LM2904 SE532/LM158	 0 to +70 -25 to +85 -40 to +85 -55 to +125	 °C °C °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V+=+5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE532, LM158/258			NE/SA532/ LM358/LM2904			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω R_S=0Ω, over temp.		±2	±5 ±7		±2	±7 ±9	mV mV
V_{OS}	Drift	R_S=0Ω, over temp.		7			7		µV/°C
I_{OS}	Offset current	I_{IN} (+)-I_{IN} (-) Over temp.		±3	±30 ±100		±5	±50 ±150	nA nA
I_{OS}	Drift	Over temp.		10			10		pA/°C
I_{BIAS}	Input current[2]	I_{IN} (+) or I_{IN} (-) Over temp., I_{IN} (+) or I_{IN} (-)		45 40	150 300		45 40	250 500	nA nA
I_B	Drift	Over temp.		50			50		pA/°C
V_{CM}	Common-mode voltage range[3]	V+=30V Over temp., V+=30V	0 0		V+-1.5 V+-2.0	0 0		V+-1.5 V+-2.0	V V
CMRR	Common-mode rejection ratio	V+=30V	70	85		65	70		dB
V_{OH}	Output voltage swing	R_L≥2kΩ, V+=30V, over temp. R_L≥10kΩ, V+=30V, over temp.	26 27	28		26 27	28		V V
V_{OL}	Output voltage swing	R_L≥10kΩ, over temp.		5	20		5	20	mV
I_{CC}	Supply current	R_L=∞, V+=30V R_L=∞ on all amplifiers, over temp., V+ =30V		0.5 0.6	1.0 1.2		0.5 0.6	1.0 1.2	mA mA
A_{VOL}	Large-signal voltage gain	R_L≥2kΩ, V_{OUT} ±10V, V+=15V (for large V_O swing) over temp.	50 25	100		25 15	100		V/mV V/mV
PSRR	Supply voltage rejection ratio	R_S=0Ω	65	100		65	100		dB
	Amplifier-to-amplifier coupling[4]	f=1kHz to 20kHz (input referred)		-120			-120		dB
I_{OUT}	Output current Source	V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}	20	40		20	40		mA
		V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}, over temp.	10	20		10	20		mA
	Sink	V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}	10	20		10	20		mA
		V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}, over temp.	5	8		5	8		mA
		V_{IN+}=0V, V_{IN-}=+1V_{DC}, V_O=200mV	12	50		12	50		µA
I_{SC}	Short circuit current[5]			40	60		40	60	mA
	Differential input voltage[6]				V+			V+	V
GBW	Unity gain bandwidth	T_A=25°C		1			1		MHz
SR	Slew rate	T_A=25°C		0.3			0.3		V/µs
V_{NOISE}	Input noise voltage	T_A=25°C, f=1kHz		40			40		nV/√Hz

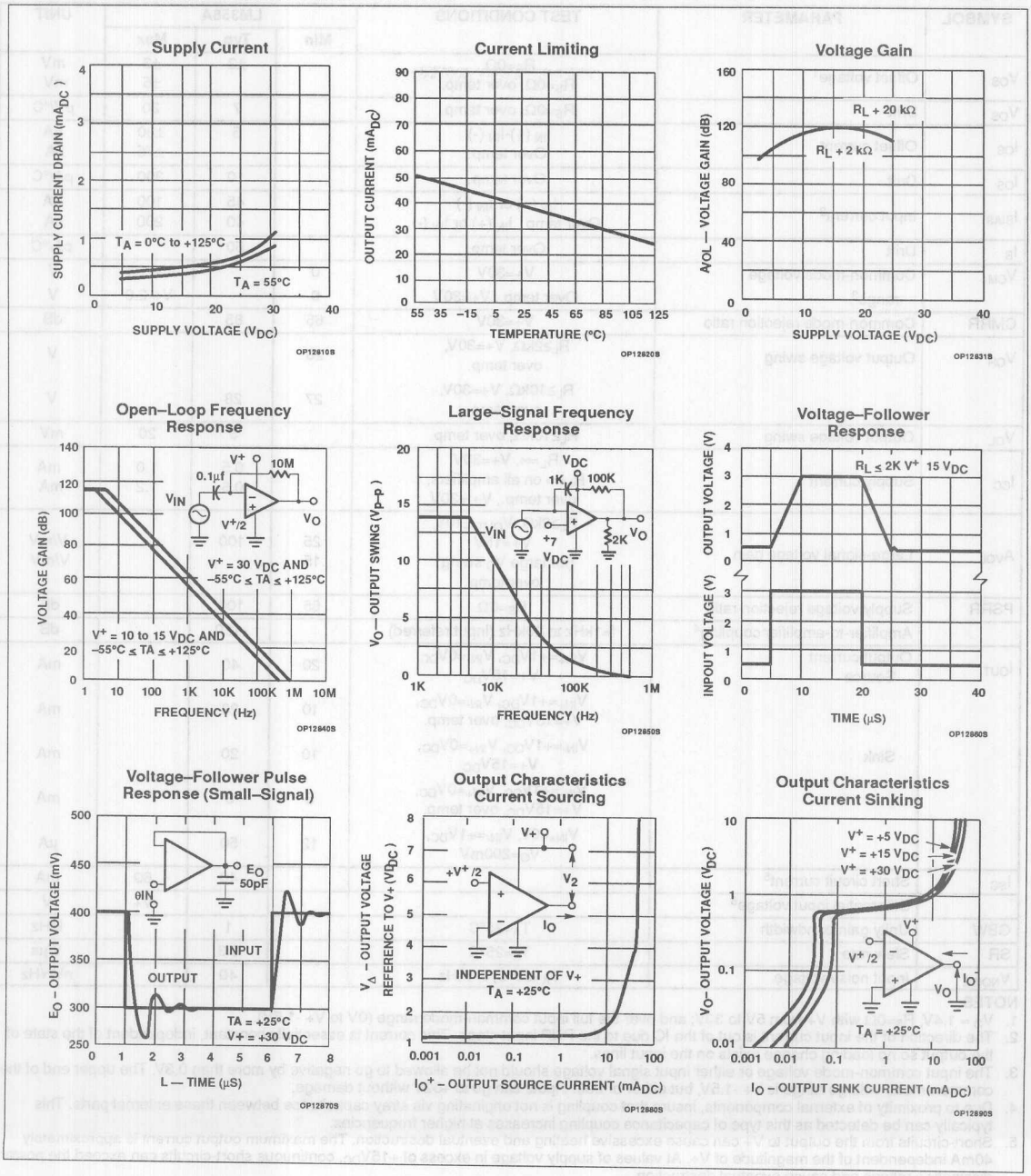
DC ELECTRICAL CHARACTERISTICS T_A=25°C, V+=+5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM358A			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω R_S=0Ω, over temp.		±2	±3 ±5	mV mV
V_{OS}	Drift	R_S=0Ω, over temp.		7	20	µV/°C
I_{OS}	Offset current	I_{IN} (+)-I_{IN} (-) Over temp.		5	±30 ±75	nA nA
I_{OS}	Drift	Over temp.		10	300	pA/°C
I_{BIAS}	Input current[2]	I_{IN} (+) or I_{IN} (-) Over temp., I_{IN} (+) or I_{IN} (-)		45 40	100 200	nA nA
I_B	Drift	Over temp.		50		pA/°C
V_{CM}	Common-mode voltage range[3]	V+=30V Over temp., V+=30V	0 0		V+-1.5 V+-2.0	V V
CMRR	Common-mode rejection ratio	V+=30V	65	85		dB
V_{OH}	Output voltage swing	R_L≥2kΩ, V+=30V, over temp. R_L≥10kΩ, V+=30V, over temp.	26 27	 28		V V
V_{OL}	Output voltage swing	R_L≥10kΩ, over temp.		5	20	mV
I_{CC}	Supply current	R_L=∞, V+=30V R_L=∞ on all amplifiers, over temp., V+ =30V		0.5 0.6	1.0 1.2	mA mA
A_{VOL}	Large-signal voltage gain	R_L≥2kΩ, V_{OUT} ±10V, V+=15V (for large V_O swing) over temp.	25 15	100		V/mV V/mV
PSRR	Supply voltage rejection ratio	R_S=0Ω	65	100		dB
	Amplifier-to-amplifier coupling[4]	f=1kHz to 20kHz (input referred)		-120		dB
I_{OUT}	Output current Source	V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}	20	40		mA
		V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}, over temp.	10	20		mA
	Sink	V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}	10	20		mA
		V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}, over temp.	5	8		mA
		V_{IN+}=0V, V_{IN-}=+1V_{DC}, V_O=200mV	12	50		µA
I_{SC}	Short circuit current[5]			40	60	mA
	Differential input voltage[6]				V+	V
GBW	Unity gain bandwidth	T_A=25°C		1		MHz
SR	Slew rate	T_A=25°C		0.3		V/µs
V_{NOISE}	Input noise voltage	T_A=25°C, f=1kHz		40		nV/√Hz

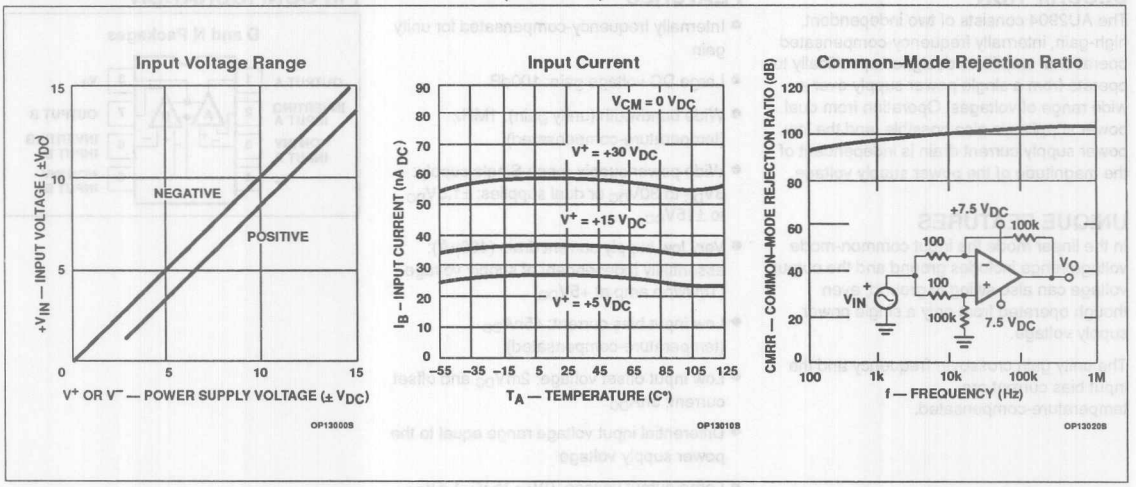
NOTES:

1. V_O ≈ 1.4V, R_S=0Ω with V+ from 5V to 30V; and over the full input common-mode range (0V to V+ -1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance coupling increases at higher frequencies.
5. Short-circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to +32V_{DC} without damage.

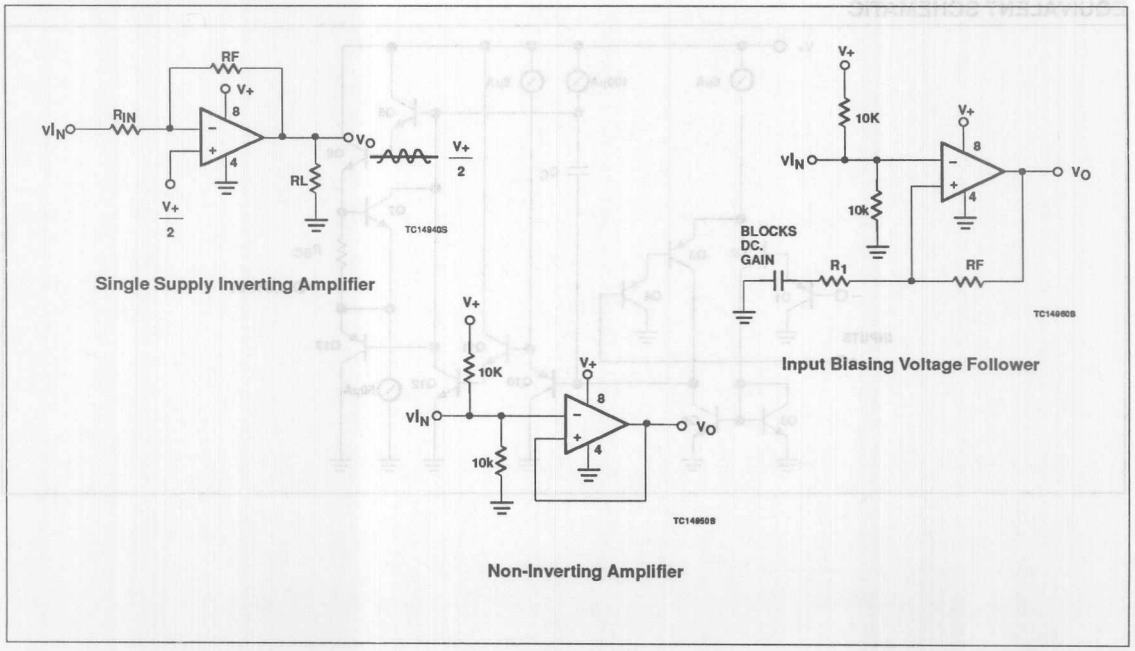
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TYPICAL APPLICATIONS



Low power dual operational amplifier

AU2904

DESCRIPTION

The AU2904 consists of two independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible, and the low power supply current drain is independent of the magnitude of the power supply voltage.

UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

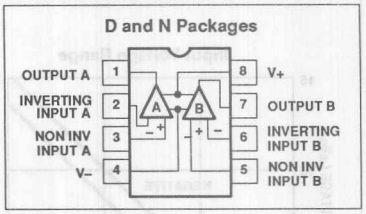
The unity gain crossover frequency and the input bias current are temperature-compensated.

FEATURES

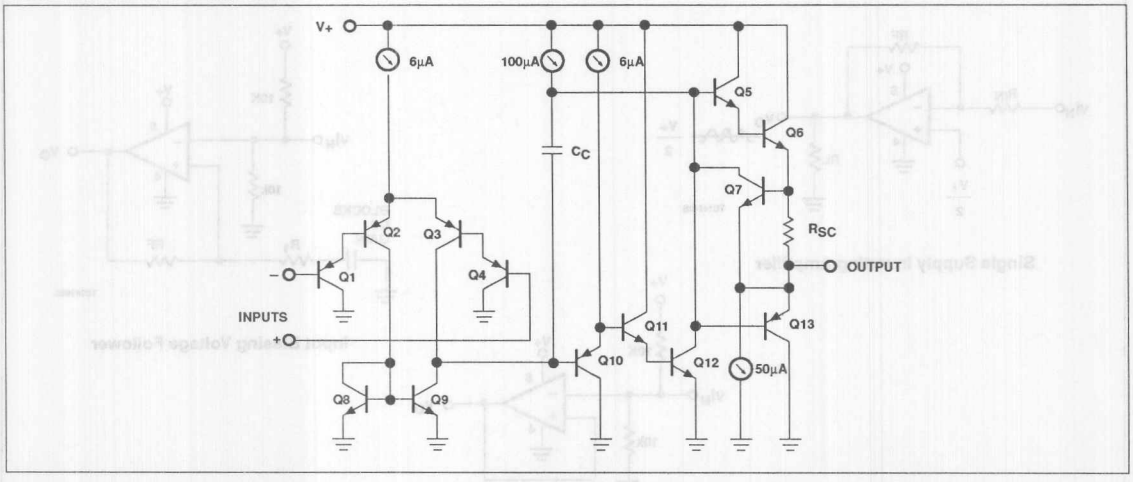
- Internally frequency-compensated for unity gain
- Large DC voltage gain: 100dB
- Wide bandwidth (unity gain): 1MHz (temperature-compensated)
- Wide power supply range Single supply: $3V_{DC}$ to $30V_{DC}$ or dual supplies: $\pm1.5V_{DC}$ to $\pm15V_{DC}$
- Very low supply current drain (400μA): essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)
- Low input bias current: $45nA_{DC}$ (temperature-compensated)
- Low input offset voltage: $2mV_{DC}$ and offset current: $5nA_{DC}$
- Differential input voltage range equal to the power supply voltage
- Large output voltage: $0V_{DC}$ to V+-$1.5V_{DC}$ swing

PIN CONFIGURATION

D and N Packages



EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	-40 to +125°C	AU2904N
8-Pin Plastic SO	-40 to +125°C	AU2904D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage V+	32 or ±16	V_{DC}
	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	-0.3 to +32	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A=25°C(still-air)[1]		
	N package	1160	mW
	D package	780	mW
	Output short-circuit to GND[5] $V+<15V_{DC}$ and T_A=25°C	Continuous	
T_A	Operating ambient temperature range AU2904	-40 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=25°C V+ =+5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	AU2904			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω		±2	±7	mV
		R_S=0Ω, over temp.			±9	mV
V_{OS}	Drift	R_S=0Ω, over temp.		7		µV/°C
I_{OS}	Offset current	$I_{IN}(+)-I_{IN}(-)$		±5	±50	nA
		Over temp.			±150	nA
I_{OS}	Drift	Over temp.		10		pA/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	250	nA
		Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		40	500	nA
I_{BIAS}	Drift	Over temp.		50		pA/°C
V_{CM}	Common-mode voltage range[3]	V+=30V	0		V+-1.5	V
		Over temp., V+=30V	0		V+-2.0	V
CMRR	Common-mode rejection ratio	V+=30V	65	70		dB
V_{OH}	Output voltage swing	R_L≥2kΩ, V+=30V, over temp.	26			V
		R_L≥10kΩ, V+=30V, over temp.	27	26		V
V_{OL}	Output voltage swing	R_L≥10kΩ, Over temp.		5	20	mV
I_{CC}	Supply current	R_L=∞, V+=30V		0.5	1.0	mA
		R_L=∞ on all amplifiers, Over temp., V+=30V		0.6	1.2	mA
A_{VOL}	Large-signal voltage gain	R_L≥2kΩ, V_{OUT} ±10V, V+=15V	25	100		V/mV
		Over temp.	15			V/mV
PSRR	Supply voltage rejection ratio	R_S=0Ω	65	100		dB
	Amplifier-to-amplifier coupling[4]	f=1kHz to 20kHz (input referred)		-120		dB
I_{OUT}	Output current source	V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}	20	40		mA

DC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	AU2904			UNIT
			Min	Typ	Max	
	Sink	V_{IN+}=+1V_{DC}, V_{IN-}=0V_{DC}, V+=15V_{DC}, over temp.	10	20		mA
		V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}	10	20		mA
		V_{IN-}=+1V_{DC}, V_{IN+}=0V_{DC}, V+=15V_{DC}, over temp.	5	8		mA
		V_{IN+}=0V, V_{IN-}=+1V_{DC}, V_O=200mV	12	50		µA
I_{SC}	Short circuit current[5]			40	60	mA

DC ELECTRICAL CHARACTERISTICS

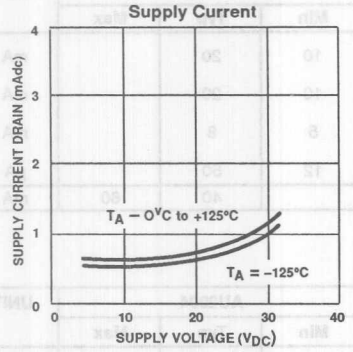
SYMBOL	PARAMETER	TEST CONDITIONS	AU2904			UNIT
			Min	Typ	Max	
	Differential input voltage[3]				V+	V
GBW	Unity gain bandwidth	T_A=25°C		1		MHz
SR	Slew rate	T_A=25°C		0.3		V/µs
V_{NOISE}	Input noise voltage	T_A=25°C f=1kHz		40		nV/√Hz

NOTES:

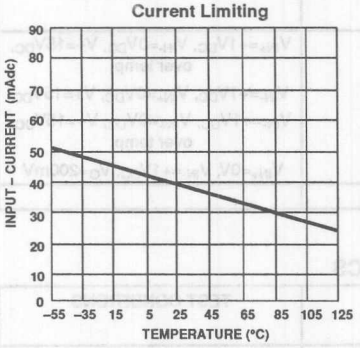
1. V_O ≈ 1.4V, R_S=0Ω with V_{CC} from 5V to 30V and over full input common-mode range (0V_{DC}+ to V_{CC}-1.5V).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+-1.5, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of coupling increases at higher frequencies.
5. Short-circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.

TYPICAL PERFORMANCE CHARACTERISTICS

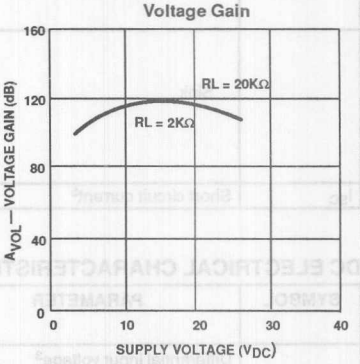
Supply Current



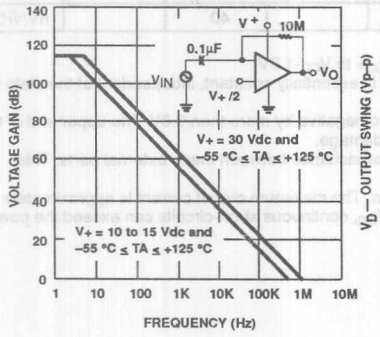
Current Limiting



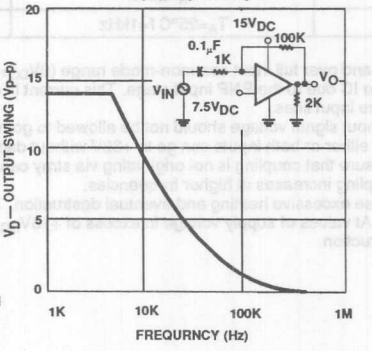
Voltage Gain



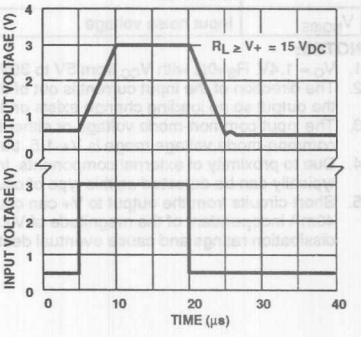
Oper–Loop Frequency Response



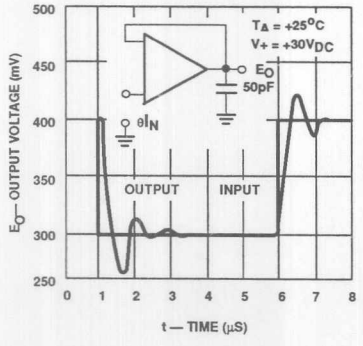
Large–Signal Frequency Resopnse



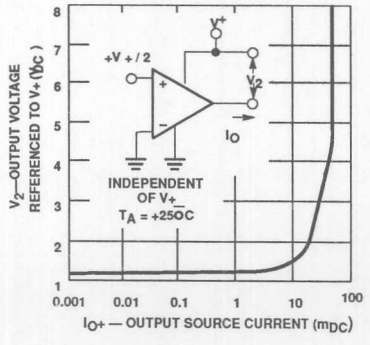
Voltage–Follower Pulse Response



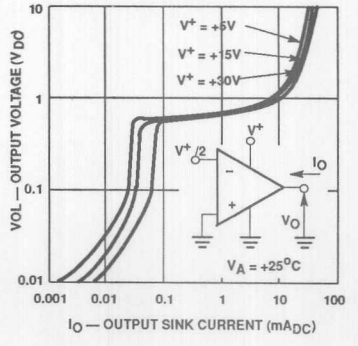
Voltage–Follower Pulse Response (Small–Signal)



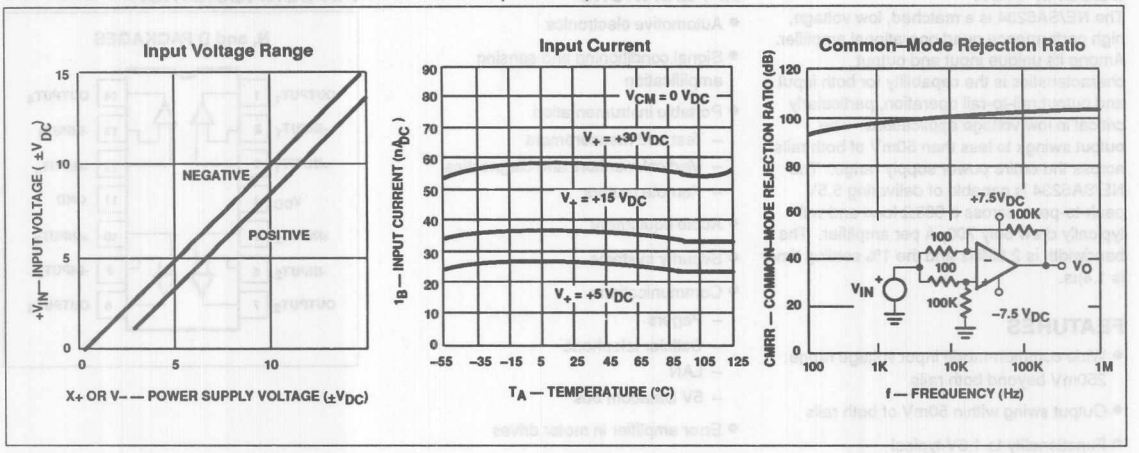
Output Characteristics Current Sourcing



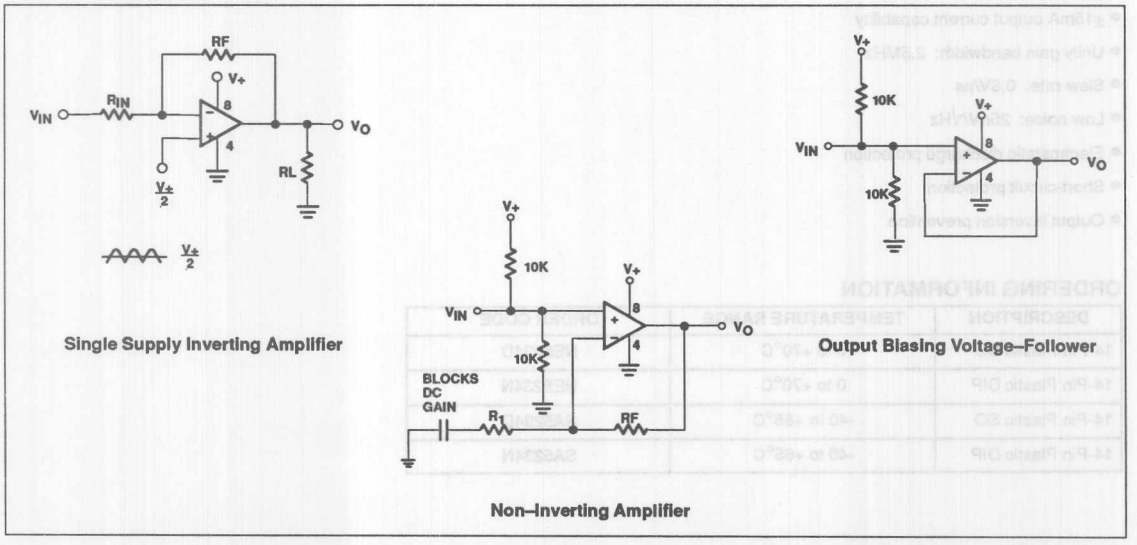
Output Characteristics Current Sinking



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TYPICAL APPLICATIONS



Matched quad high-performance low-voltage operational amplifier

NE/SA5234

DESCRIPTION

The NE/SA5234 is a matched, low voltage, high performance quad operational amplifier. Among its unique input and output characteristics is the capability for both input and output rail-to-rail operation, particularly critical in low voltage applications. The output swings to less than 50mV of both rails across the entire power supply range. The NE/SA5234 is capable of delivering 5.5V peak-to-peak across a 600Ω load and will typically draw only 700μA per amplifier. The bandwidth is 2.5MHz and the 1% settling time is 1.4μs.

FEATURES

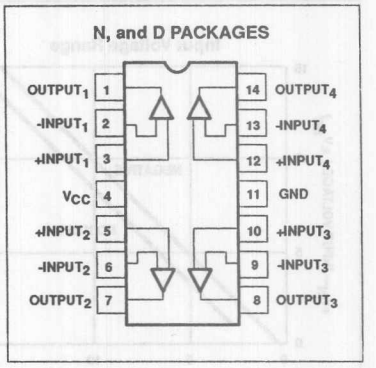
- Wide common-mode input voltage range: 250mV beyond both rails
- Output swing within 50mV of both rails
- Functionality to 1.8V typical
- Low current consumption: 700μA per amplifier
- ±15mA output current capability
- Unity gain bandwidth: 2.5MHz
- Slew rate: 0.8V/μs
- Low noise: 25nV/√Hz
- Electrostatic discharge protection
- Short-circuit protection
- Output inversion prevention

APPLICATIONS

- Automotive electronics
- Signal conditioning and sensing amplification
- Portable instrumentation
  - Test and measurement
  - Medical monitors and diagnostics
  - Remote meters
- Audio equipment
- Security systems
- Communications
  - Pagers
  - Cellular telephone
  - LAN
  - 5V Datacom bus
- Error amplifier in motor drives
- Transducer buffer amplifier

PIN CONFIGURATION

N, and D PACKAGES



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE5234D
14-Pin Plastic DIP	0 to +70°C	NE5234N
14-Pin Plastic SO	-40 to +85°C	SA5234D
14-Pin Plastic DIP	-40 to +85°C	SA5234N

Matched quad high-performance low-voltage operational amplifier

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
V_{ESD}	ESD protection voltage at any pin[5] human body model robot model	 2000 200	 V V
V_S	Dual supply voltage	±3.5	V
V_{DP}	Voltage at any device pin[1]	V_S ± 0.5	V
I_{DP}	Current into any device pin[1]	± 50	mA
V_{IN}	Differential input voltage[2]	0.5	V
V_{CM}	Common-mode input voltage (positive)	V_{CC} + 0.5	V
V_{CM}	Common-mode input voltage (negative)	V_{EE} - 0.5	V
P_D	Power dissipation[3]	500	mW
T_J	Operating junction temperature[3]	+150	°C
V_{SC}	Supply voltage allowing indefinite output short circuit to either rail[3,4]	7	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C
θ_{JA}	Thermal impedance		
	14 pin Plastic DIP	80	°C/W
	14 pin Plastic SO	115	°C/W

NOTES:

1. Each pin is protected by ESD diodes. The voltage at any pin is limited by the ESD diodes.
2. The differential input of each amplifier is limited by two internal diodes, connected in parallel and opposite to each other. For more differential input range, use differential resistors in series with the input pins.
3. The maximum operating junction temperature is +150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions. Derates above +25°C: F package at 6.7mW/°C; N package at 9.5mW/°C; D package at 6.25mW/°C.
4. Simultaneous short circuits of two or more amplifiers to the positive or negative rail can exceed the power dissipation ratings and cause eventual destruction of the device.
5. Guaranteed by design.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	+2 to +5.5	V
V_S	Dual supply voltage	±1 to ±2.75	V
V_{CM}	Common-mode input voltage (positive)	V_{CC} + 0.25	V
V_{CM}	Common-mode input voltage (negative)	V_{EE} - 0.25	V
T_A	Temperature		
	NE	0 to +70	°C
	SA	-40 to +85	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2 to 5.5V, V_{EE} = 0V, T_A = 25°C; $V_{EE} < V_{CM} < V_{CC}$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current	V_{CC} = 5.5V		2.8	3.5		2.8	3.5	mA
		V_{CC} = 5.5V over full temperature range		3.0	4.2		3.2	4.3	mA
V_{OS}	Offset voltage			±0.2	±4		±0.2	±4	mV
		Over full temperature range		±0.4	±5		±0.6	±5	mV
$\Delta V_{OS}/\Delta T$	Offset voltage drift with temperature			4			4		µV/°C
ΔV_{OS}	Offset voltage difference between any amplifiers in the same package at the same common mode level[1]			0.4	3		0.4	3	mV
		Over full temperature range		0.8	4		1.2	4	mV
I_{OS}	Offset current			±3	±20		±3	±30	nA
		Over full temperature range		±4	±30		±6	±60	nA
$\Delta I_{OS}/\Delta T$	Offset current drift with temperature			0.02	±.3		0.03	±.3	nA/°C
I_B	Input bias current[1]	$V_{EE} < V_{CM} < V_{EE}$ +0.5V	-150	-90		-150	-90		nA
		Over full temperature range	-175	-100		-200	-150		nA
		V_{EE} +1V < V_{CM} < V_{CC}		25	70		25	75	nA
		Over full temperature range		35	100		35	120	nA
$\Delta I_B/\Delta T$	Input bias current drift with temperature			0.5			0.5		nA/°C
ΔI_B	Input bias current difference between any amplifier in the same package at the same common mode level.	$V_{EE} < V_{CM} < V_{EE}$ +0.5V		10	30		10	30	nA
		Over full temperature range		25	50		50	70	nA
		V_{EE} +1V < V_{CM} < V_{CC}		5	20		5	20	nA
		Over full temperature range		15	30		25	50	nA
V_{CM}	Common-mode input range	$V_{OS} \leq$ 6mV	V_{EE}-0.25		V_{CC}+0.25	V_{EE}-0.25		V_{CC}+0.25	V
		$V_{OS} \leq$ 6mV over full temperature range	V_{EE}-0.1		V_{CC}+0.1	V_{EE}-0.1		V_{CC}+0.1	V
CMRR	Common-mode rejection ratio, small signal	$V_{EE} < V_{CM} < V_{EE}$+0.5V, V_{EE}+1V < V_{CM} < V_{CC}		100		90	100		dB
		Over full temperature range		100		80	90		dB
	Common-mode rejection ratio, large signal	$V_{EE} < V_{CM} < V_{CC}$		90			100		dB
		Over full temperature range		80			90		dB
PSRR	Power supply rejection ratio	$V_{EE} < V_{CM} < V_{CC}$	80	100		80	100		dB
		Over full temperature range	80	90		80	90		dB

DC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
I_L	Peak load current, sink and source		10	12		10	12		mA
		Over full temperature range	5	8		5	8		mA
A_{VOL}	Open-loop voltage gain		90	110		90	110		dB
		Over full temperature range		90			90		dB
V_{OUT}	Output voltage swing	I_{PEAK} = 0.1mA	V_{EE}+0.05		V_{CC}-0.05	V_{EE}+0.1		V_{CC}-0.1	V
		I_{PEAK} = 10mA	V_{EE}+0.25		V_{CC}-0.25	V_{EE}+0.25		V_{CC}-0.25	V
		I_{PEAK} = 5mA over full temp range	V_{EE}+0.22		V_{CC}-0.2	V_{EE}+0.2		V_{CC}-0.2	V
	Output voltage swing for V_{CC} = 2.75V, V_{EE} = -2.75V	R_L = 2kΩ	V_{EE}+0.2		V_{CC}-0.2	V_{EE}+0.2		V_{CC}-0.2	V
		R_L = 600Ω,	V_{EE}+0.25		V_{CC}-0.25	V_{EE}+0.25		V_{CC}-0.25	V

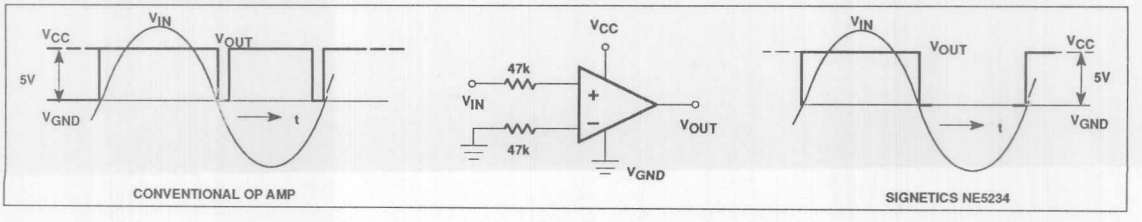
NOTES:
1. These parameters are measured for $V_{EE} < V_{CM} < V_{EE}$+.5V and for V_{EE}+1V < $V_{CM} < V_{CC}$. By design these parameters are intermediate for common mode ranges between the measured regions.

AC ELECTRICAL CHARACTERISTICS

T_A = +25°C; V_{CC} = 2 to 5.5V; R_L = 10k; C_L = 100pF; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA/SE5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	Over full temperature range	.5	0.8		.5	0.8		V/μs
BW	Unity gain bandwidth: -3dB	Over full temperature range	2	2.5	4.0	2	2.5	4.0	MHz
θ_M	Phase Margin	C_L = 50pF		55			55		deg
t_S	1% settling time	A_V = 1, 1V step		1.4			1.4		μs
V_N	Input referred voltage noise	A_V = 1, R_S = 0Ω, at 1kHz		25			25		nV/$Hz^{1/2}$
THD	Total harmonic distortion	10kHz, $1V_{P-P}$, A_V = 1		0.1			0.1		%

OUTPUT INVERSION PREVENTION



Matched quad high-performance low-voltage operational amplifier

NE/SA5234

DC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
I_O	Peak load current; sink and source		10	12		10	12		mA
		Over full temperature range	6	8		8	8		mA
A_{VOL}	Open-loop voltage gain		50	110		80	110		dB
		Over full temperature range	80				80		dB
V_{OUT}	Output voltage swing	I_{PEAK} = 0.1mA	V_{EE}+0.05		V_{CC}−0.05	V_{EE}+0.1		V_{CC}−0.1	V
		I_{PEAK} = 10mA	V_{EE}+0.5		V_{CC}−0.25	V_{EE}+0.25		V_{CC}−0.25	V
		I_{PEAK} = 5mA over full temp range	V_{EE}+0.2		V_{CC}−0.2	V_{EE}+0.2		V_{CC}−0.2	V
	Output voltage swing for V_{CC} = +2.75V; V_{EE} = −2.75V	R_L = 2kΩ	V_{EE}+0.2		V_{CC}−0.2	V_{EE}+0.2		V_{CC}−0.2	V
		R_L = 600Ω	V_{EE}+0.25		V_{CC}−0.25	V_{EE}+0.25		V_{CC}−0.25	V

NOTES:
1. These parameters are measured for $V_{EE} < V_{CM} < V_{EE}$+8V and for V_{EE}+1V < $V_{CM} < V_{CC}$. By design, these parameters are intermediate for common mode ranges between the measured regions.

AC ELECTRICAL CHARACTERISTICS

T_A = +25°C; V_{CC} = 2 to 8.5V; R_L = 10k; C_L = 100pF; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE5234			SA/SE5234			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	Over full temperature range	.5	0.8		.5	0.8		V/µs
BW	Unity gain bandwidth: -3dB	Over full temperature range	2	2.5	4.0	2	2.5	4.0	MHz
Θ_ϕ	Phase Margin	C_L = 60pF		55			55		deg
t_S	1% settling time	A_V = 1, 1V step		1.4			1.4		µs
V_N	Input referred voltage noise	A_V = 1, R_S = 0Ω, at 1kHz		25			25		$\frac{nV}{Hz^{1/2}}$
THD	Total Harmonic distortion	10kHz, $1V_{p-p}$, A_V = 1		0.1			0.1		%

OUTPUT INVERSION PREVENTION

CONVENTIONAL OP AMP

NONINVERTING DESIGN

Section 2
High Frequency/Video Amplifiers

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NE/SA5204A	Wide-band high-frequency amplifier	99
NE/SA/ SE5205A	Wide-band high-frequency amplifier	108
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NE/SA5219	Wideband variable gain amplifier	133
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Philips Semiconductors-Signetics

Section 2
High Frequency/Video Amplifiers

General Purpose/Linear ICs

INDEX

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NE/SA5230 Wideband variable gain amplifier 119

NE/SA5219 Wideband variable gain amplifier 139

NE/SE5230 High frequency operational amplifier 145

NE5502 Video amplifier 154

NE592 Video amplifier 159

μA733/733C Differential video amplifier 167

Wide-band high-frequency amplifier NE/SA5204A

DESCRIPTION

The NE/SA5204A family of wideband amplifiers replaces the NE/SA5204 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nomically identical to the original parts.

The NE/SA5204A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 200MHz. The -3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204A operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204A is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204A solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC-coupling capacitors because the NE/SA5204A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

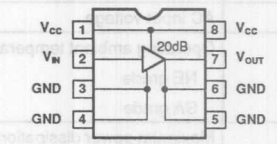
The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204As in series as required, without any degradation in amplifier stability.

FEATURES

- Bandwidth (min.)
  200 MHz, ±0.5dB
  350 MHz, -3dB
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface-mount package available
- Cascadable
- 2000V ESD protection

PIN CONFIGURATION

N, D Packages



TOP VIEW

APPLICATIONS

- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broadband LANs
- Networks
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

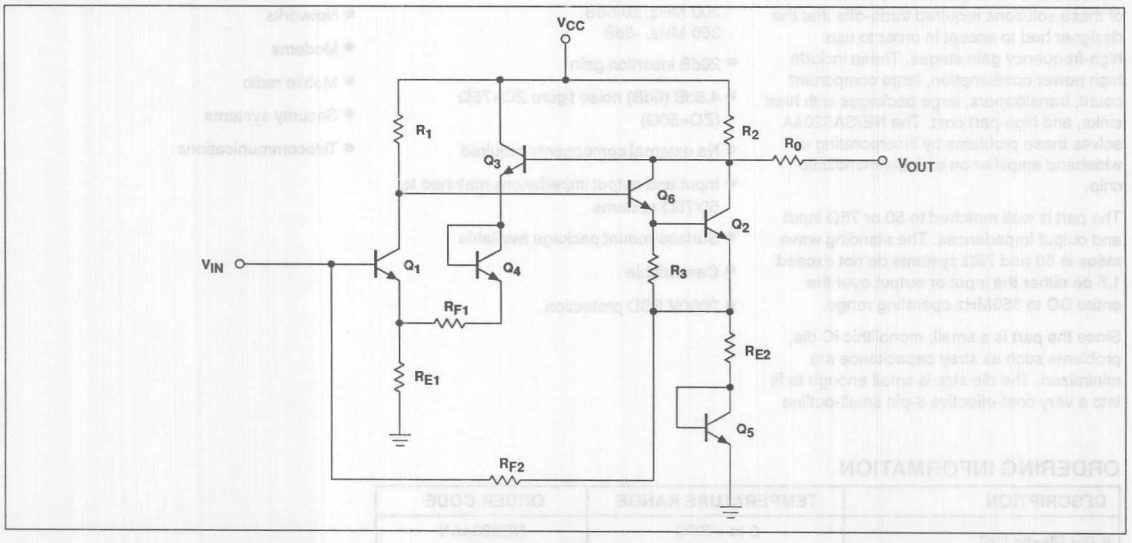
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C –40 to +85°C	NE5204AN SA5204AN
8-Pin Plastic SO package	0 to +70°C –40 to +85°C	NE5204AD SA5204AD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{IN}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	–40 to +85	°C
P_{DMAX}	Maximum power dissipation[1, 2] T_A=25°C(still–air)		
	N package	1160	mW
	D package	780	mW
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	–55 to +150	°C
T_{SOLD}	Lead temperature (soldering 60s)	300	°C

NOTES:
1. Derate above 25°C, at the following rates
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See "Power Dissipation Considerations" section.

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5		8	V
I_{CC}	Supply current	Over temperature	19	25	33	mA
S21	Insertion gain	f=100MHz, over temperature	16	19	22	dB
S11	Input return loss	f=100MHz		25		dB
		DC –550MHz		12		dB
S22	Output return loss	f=100MHz		27		dB
		DC –550MHz		12		dB
S12	Isolation	f=100MHz		–25		dB
		DC –550MHz		–18		dB
BW	Bandwidth	±0.5dB	200	350		MHz
BW	Bandwidth	–3dB	350	550		MHz
	Noise figure (75Ω)	f=100MHz		4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0		dB
	Saturated output power	f=100MHz		+7.0		dBm
	1dB gain compression	f=100MHz		+4.0		dBm
	Third–order intermodulation intercept (output)	f=100MHz		+17		dBm
	Second–order intermodulation intercept (output)	f=100MHz		+24		dBm
t_R	Rise time			500		ps
t_P	Propagation delay			500		ps

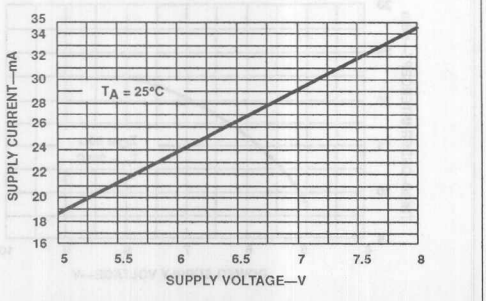


Figure 1. Supply Current vs Supply Voltage

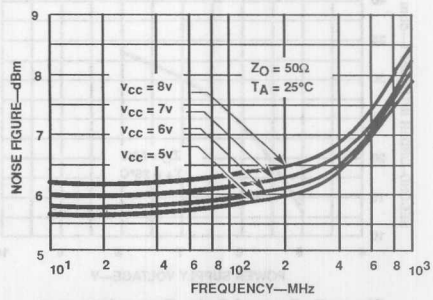


Figure 2. Noise Figure vs Frequency

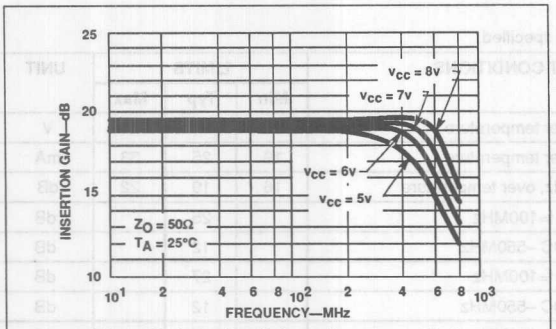


Figure 3. Insertion Gain vs Frequency (S_{21})

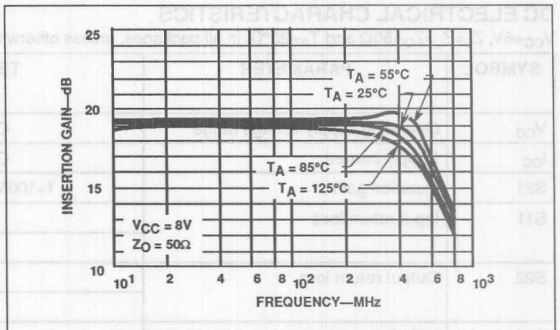


Figure 4. Insertion Gain vs Frequency (S_{21})

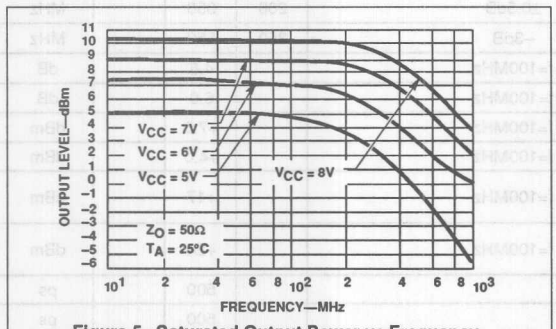


Figure 5. Saturated Output Power vs Frequency

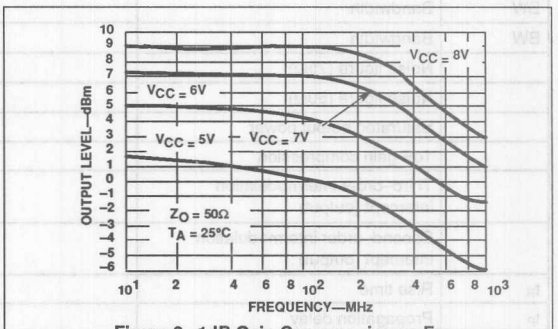


Figure 6. 1dB Gain Compression vs Frequency

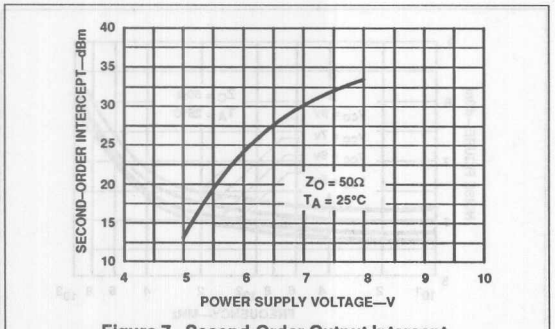


Figure 7. Second-Order Output Intercept vs Supply Voltage

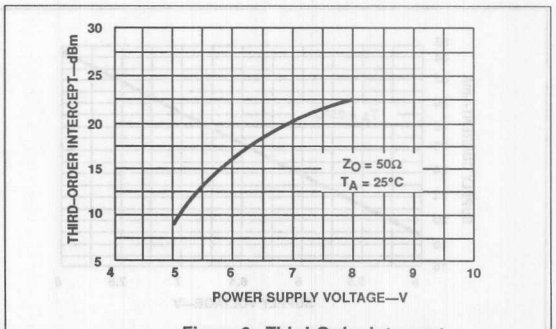


Figure 8. Third-Order Intercept vs Supply Voltage

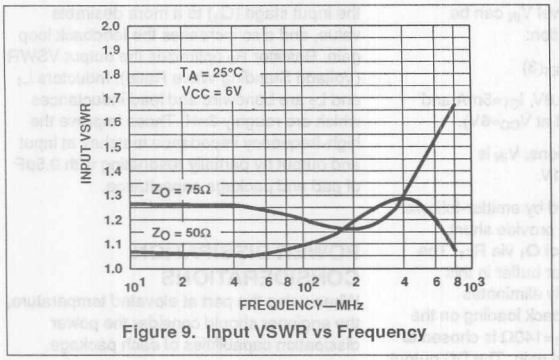


Figure 9. Input VSWR vs Frequency

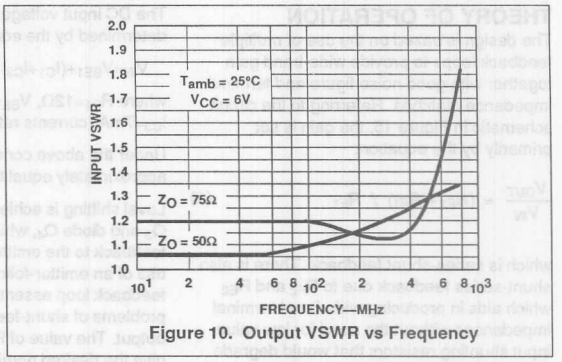


Figure 10. Output VSWR vs Frequency

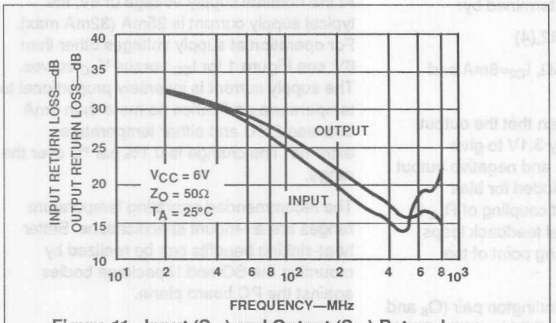


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

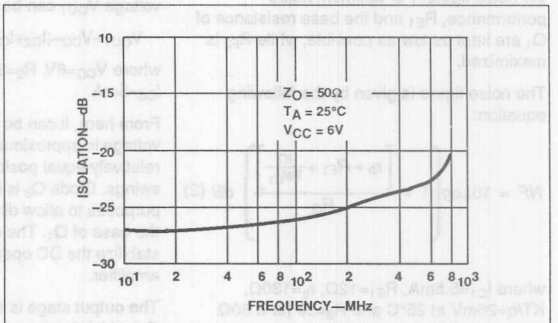


Figure 12. Isolation vs Frequency (S_{12})

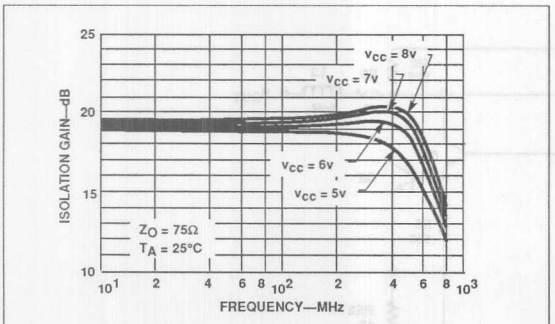


Figure 13. Insertion Gain vs Frequency (S_{21})

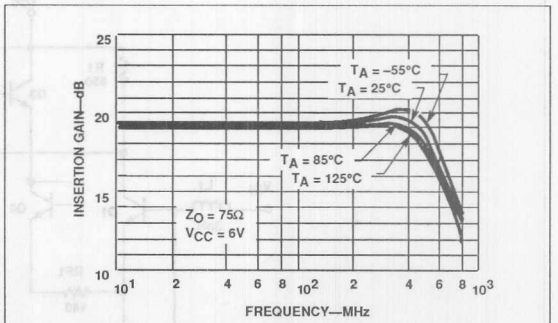


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1}) \; / \; R_{E1} \qquad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wide-band terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible, while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10Log\left(1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}}\right]}{R_O}\right) dB \quad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\,R_{E1} \quad (3)$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4, which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt-feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2, \quad (4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=8mA and I_{C6}=5mA.

From here, it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat-sinking benefits can be realized by mounting the SO and N package bodies against the PC board plane.

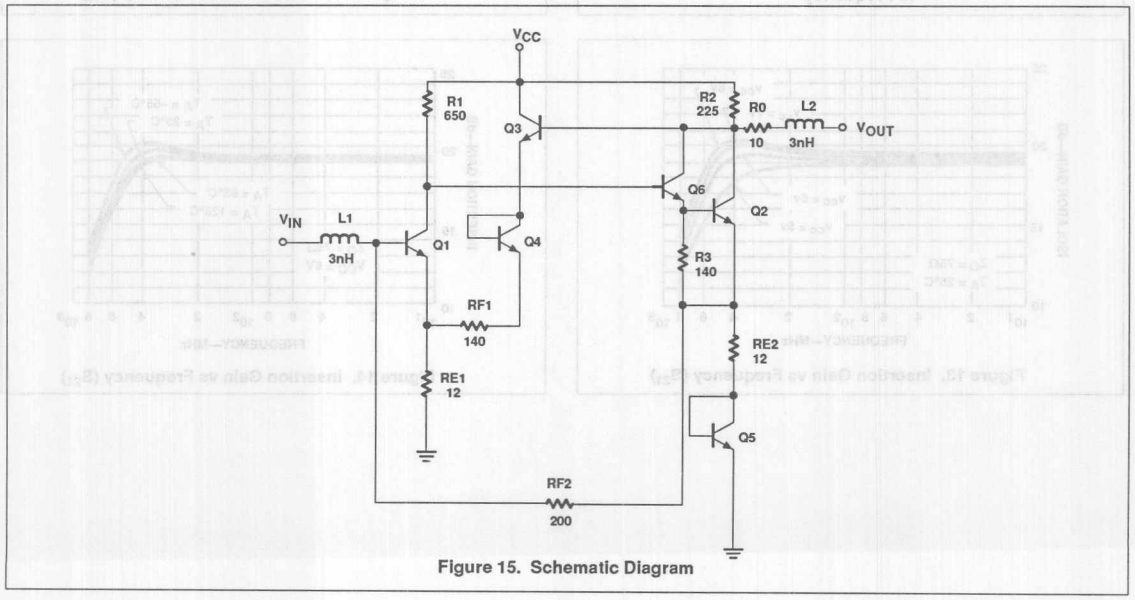


Figure 15. Schematic Diagram

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5204A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible, and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC-coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low-impedance system, or the DC bias on the output of the amplifier will be loaded down, causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high-frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

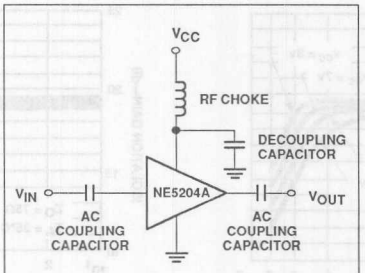


Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling

SCATTERING PARAMETERS

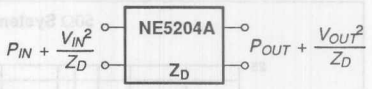
The primary specifications for the NE5204A are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier, and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5204A to other high-frequency amplifiers.

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D=Z_{IN}=Z_{OUT}$ for the NE/SA/SE5204A



$P_{IN} + \frac{V_{IN}^2}{Z_D}$ $\quad P_{OUT} + \frac{V_{OUT}^2}{Z_D}$

$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I=V_I{}^2$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the NE/SA/SE5204A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

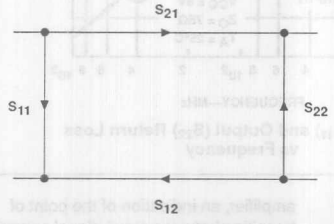
$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:



a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} = \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OSOLATION

$$S_{12} = \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} = \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} = \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

b.

Figure 17.

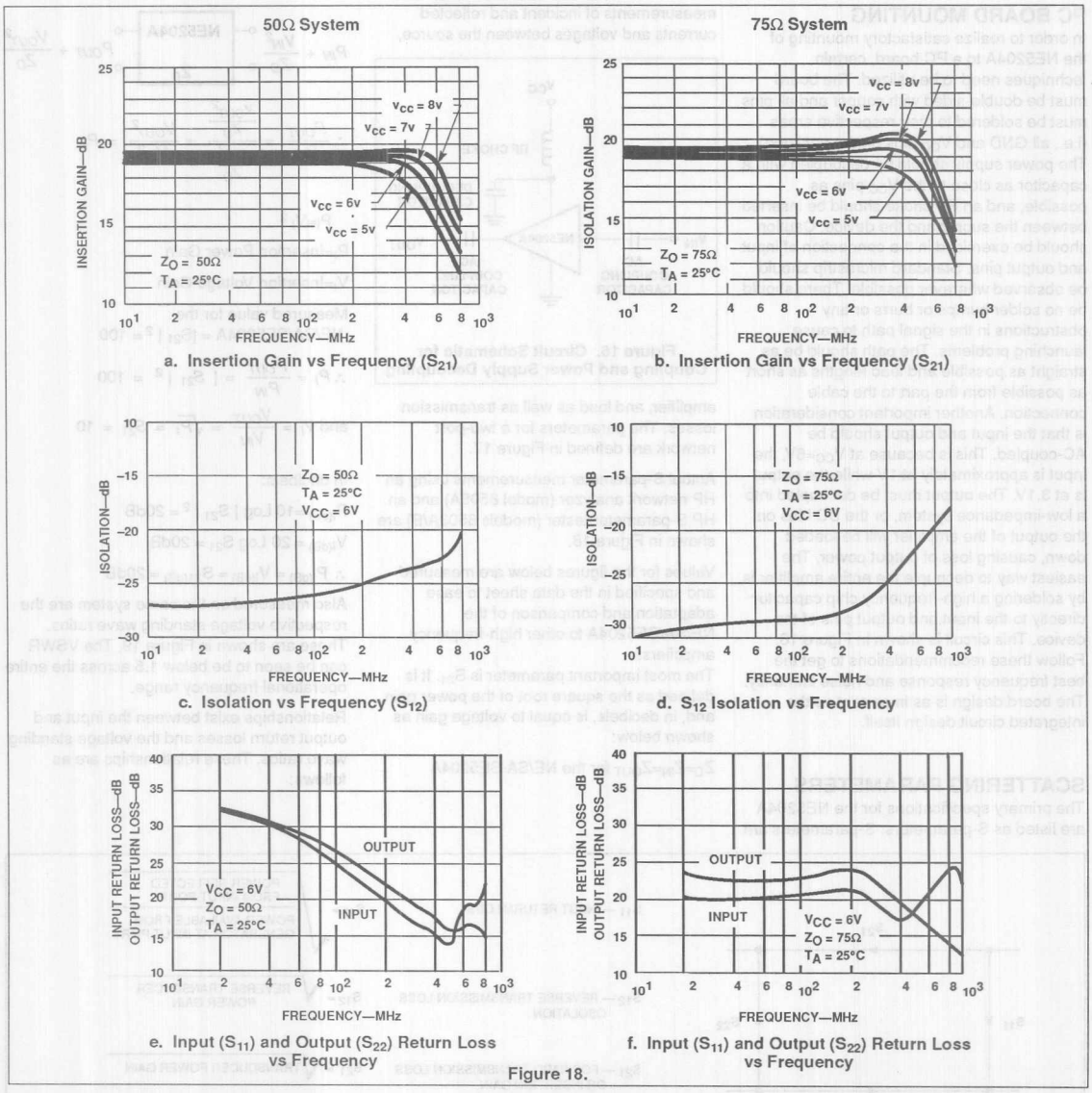


Figure 18.

INPUT RETURN LOSS=S_{11}dB
S_{11}dB=20 Log | S_{11} |

OUTPUT RETURN LOSS=S_{22}dB
S_{22}dB=20 Log | S_{22} |

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

1DB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily

overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

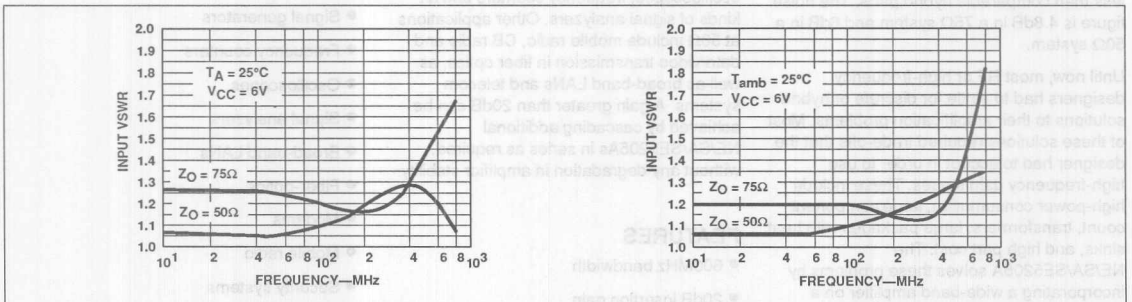
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$$IP_2 = P_{OUT} + IMR_2$$

$$IP_3 = P_{OUT} + IMR_3/2$$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One



a. Input VSWR vs Frequency

b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA5204A we have chosen an output level of –10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

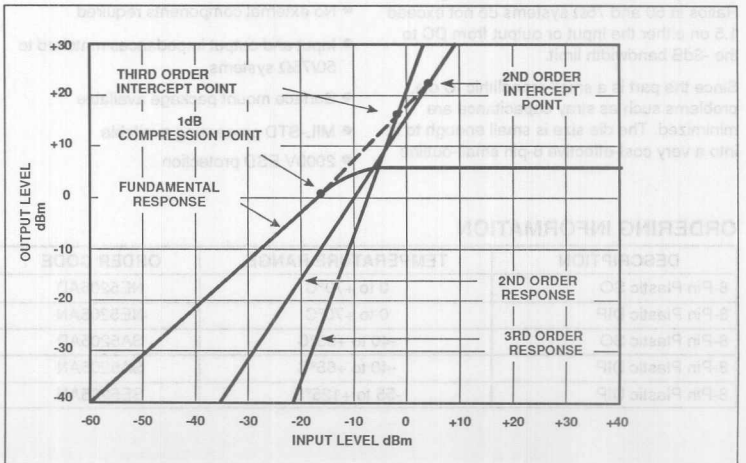


Figure 20.

Wide-band high-frequency amplifier NE/SA/SE5205A

DESCRIPTION

The NE/SA/SE5205A family of wideband amplifiers replace the NE/SA/SE5205 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nominally identical to the original parts.

The NE/SA/SE5205A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the -3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205A operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205A solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the -3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC coupling capacitors because the NE/SA/SE5205A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

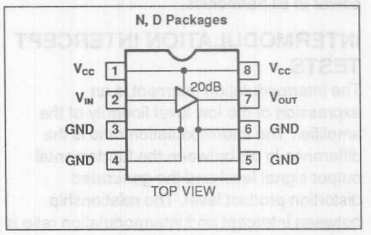
The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205As in series as required, without any degradation in amplifier stability.

FEATURES

- 600MHz bandwidth
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface mount package available
- MIL-STD processing available
- 2000V ESD protection

PIN CONFIGURATIONS



APPLICATIONS

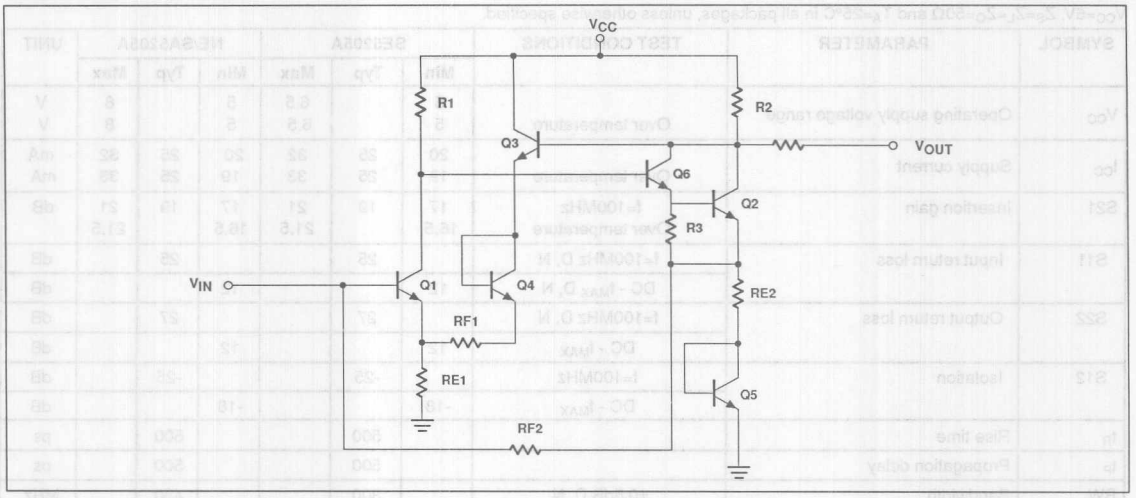
- 75Ω cable TV decoder boxes
- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broad-band LANs
- Fiber-optics
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5205AD
8-Pin Plastic DIP	0 to +70°C	NE5205AN
8-Pin Plastic SO	-40 to +85°C	SA5205AD
8-Pin Plastic DIP	-40 to +85°C	SA5205AN
8-Pin Plastic DIP	-55 to +125°C	SE5205AN

Wide-band high-frequency amplifier NE/SA/SE5205A

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range		
	NE grade	0 to +70	°C
	SA grade	-40 to +85	°C
	SE grade	-55 to +125	°C
P_{DMAX}	Maximum power dissipation, T_A=25°C (still-air)[1, 2]		
	N package	1160	mW
	D package	780	mW

NOTES:
1. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. See "Power Dissipation Considerations" section.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=6V, Z_S=Z_L=Z_O=50Ω and T_A=25°C in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205A			NE/SA5205A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Operating supply voltage range	Over temperature	5 5		6.5 6.5	5 5		8 8	V V
I_{CC}	Supply current	Over temperature	20 19	25 25	32 33	20 19	25 25	32 33	mA mA
S21	Insertion gain	f=100MHz Over temperature	17 16.5	19	21 21.5	17 16.5	19	21 21.5	dB
S11	Input return loss	f=100MHz D, N		25			25		dB
		DC - f_{MAX} D, N	12			12			dB
S22	Output return loss	f=100MHz D, N		27			27		dB
		DC - f_{MAX}	12			12			dB
S12	Isolation	f=100MHz		-25			-25		dB
		DC - f_{MAX}	-18			-18			dB
t_R	Rise time			500			500		ps
t_P	Propagation delay			500			500		ps
BW	Bandwidth	±0.5dB D, N		300			450		MHz
f_{MAX}	Bandwidth	-3dB D, N				550			MHz
	Noise figure (75Ω)	f=100MHz		4.8			4.8		dB
	Noise figure (50Ω)	f=100MHz		6.0			6.0		dB
	Saturated output power	f=100MHz		+7.0			+7.0		dBm
	1dB gain compression	f=100MHz		+4.0			+4.0		dBm
	Third-order intermodulation intercept (output)	f=100MHz		+17			+17		dBm
	Second-order intermodulation intercept (output)	f=100MHz		+24			+24		dBm

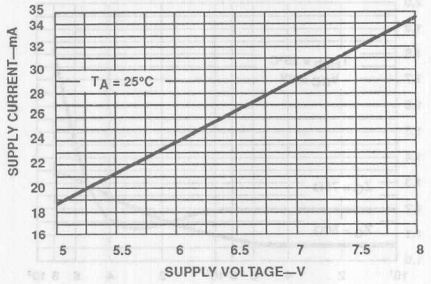


Figure 1. Supply Current vs Supply Voltage

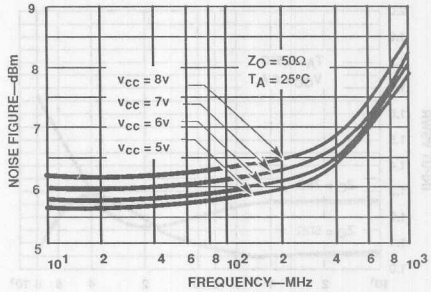


Figure 2. Noise Figure vs Frequency

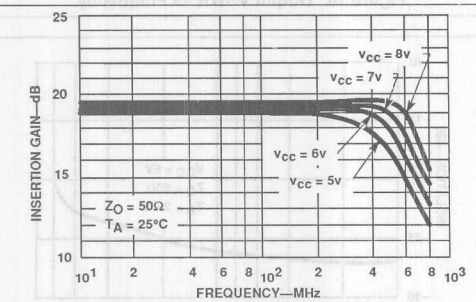


Figure 3. Insertion Gain vs Frequency (S_{21})

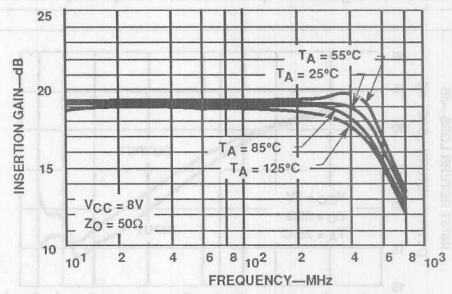


Figure 4. Insertion Gain vs Frequency (S_{21})

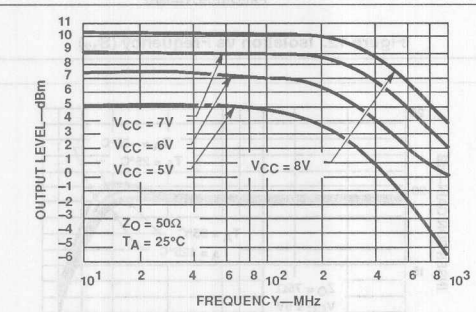


Figure 5. Saturated Output Power vs Frequency

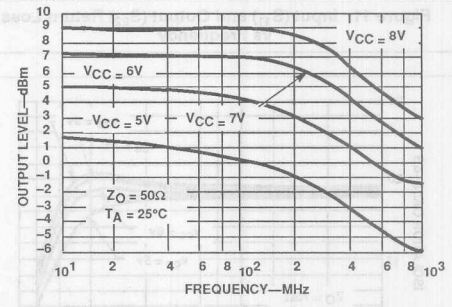


Figure 6. 1dB Gain Compression vs Frequency

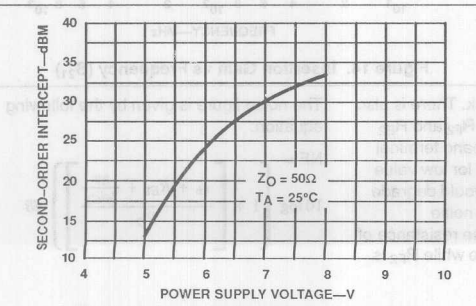


Figure 7. Second-Order Output Intercept vs Supply Voltage

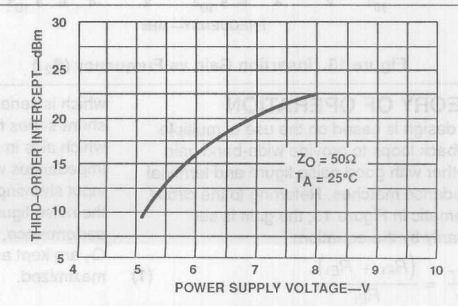


Figure 8. Third-Order Intercept vs Supply Voltage

Wide-band high-frequency amplifier NE/SA/SE5205A

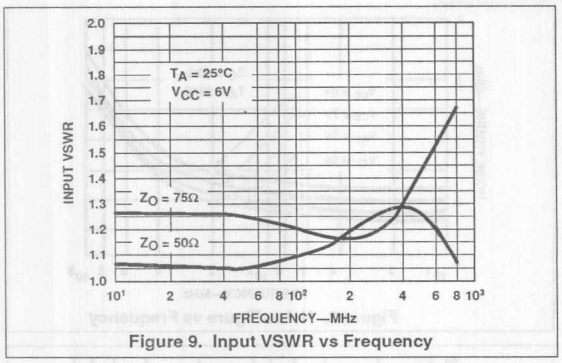


Figure 9. Input VSWR vs Frequency

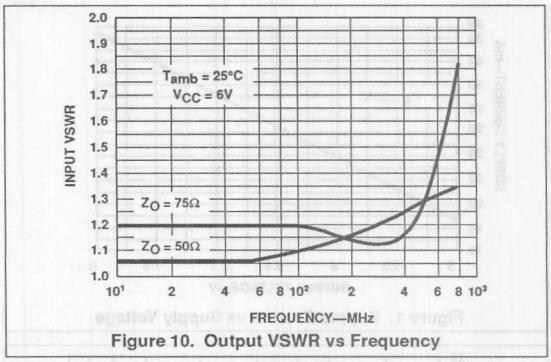


Figure 10. Output VSWR vs Frequency

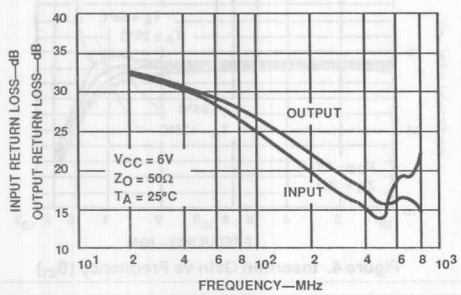


Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

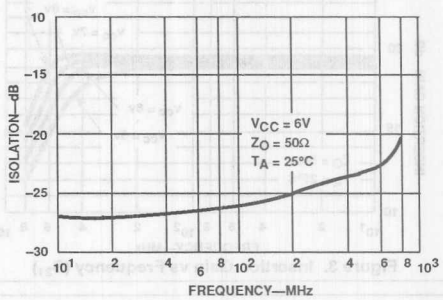


Figure 12. Isolation vs Frequency (S_{12})

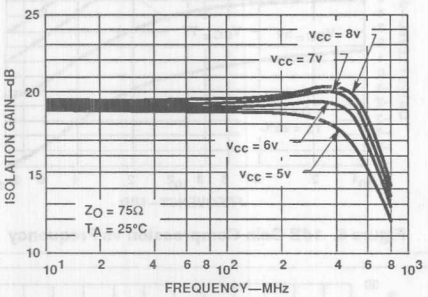


Figure 13. Insertion Gain vs Frequency (S_{21})

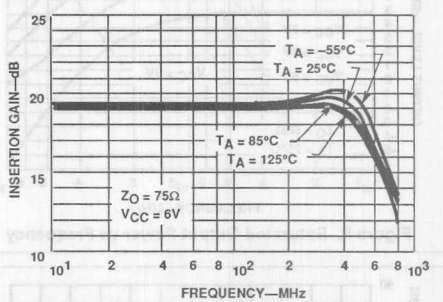


Figure 14. Insertion Gain vs Frequency (S_{21})

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{(R_{F1} + R_{E1})}{R_{E1}} \quad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF = 10\log\left\{1 + \left[\frac{r_b + R_{E1} + \frac{KT}{2qI_{C1}}}{R_O}\right]\right\} dB \quad (2)$$

where I_{C1}=5.5mA, R_{E1}=12Ω, r_b=130Ω, KT/q=26mV at 25°C and R_0=50 for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN}=V_{BE1}+(I_{C1}+I_{C3})\ R_{E1}$$

where R_{E1}=12Ω, V_{BE}=0.8V, I_{C1}=5mA and I_{C3}=7mA (currents rated at V_{CC}=6V).

Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of R_{F1}=140Ω is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT}=V_{CC}-(I_{C2}+I_{C6})R2,(4)$$

where V_{CC}=6V, R_2=225Ω, I_{C2}=8mA and I_{C6}=5mA.

From here it can be seen that the output voltage is approximately 3.1V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

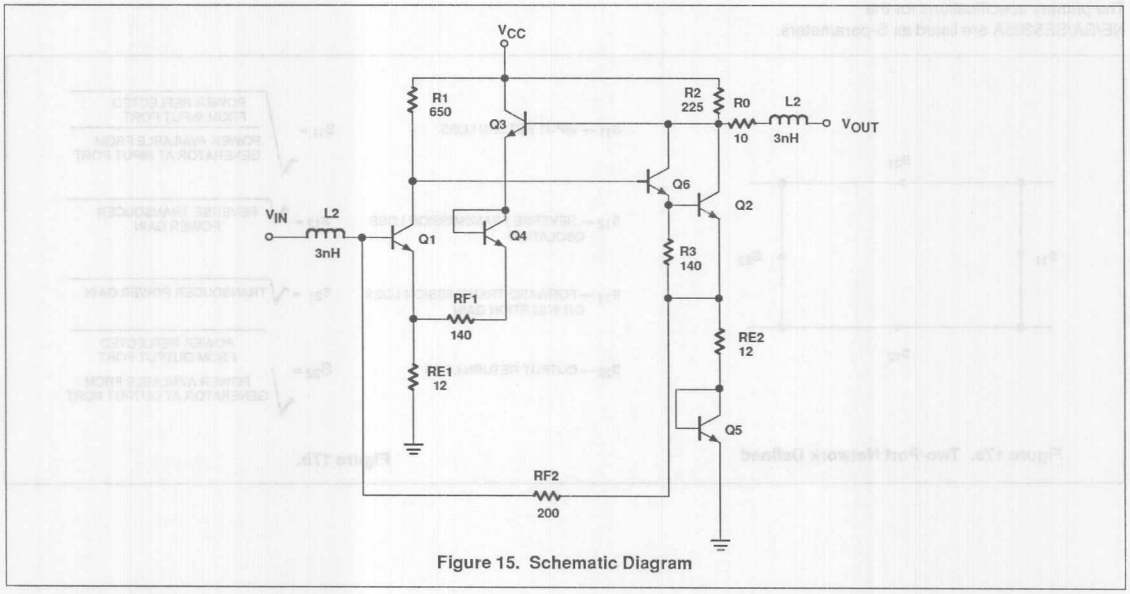


Figure 15. Schematic Diagram

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (32mA Max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D package body against the PC board plane.

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205A to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and

output should be AC coupled. This is because at V_{CC}=6V, the input is approximately at 1V while the output is at 3.1V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205A to other high-frequency amplifiers.

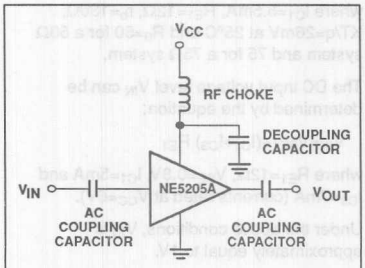


Figure 1. Circuit Schematic for Coupling and Power Supply Decoupling

SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205A are listed as S-parameters.

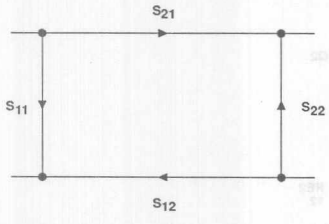


Figure 17a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} = \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS
OSOLATION

$$S_{12} = \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

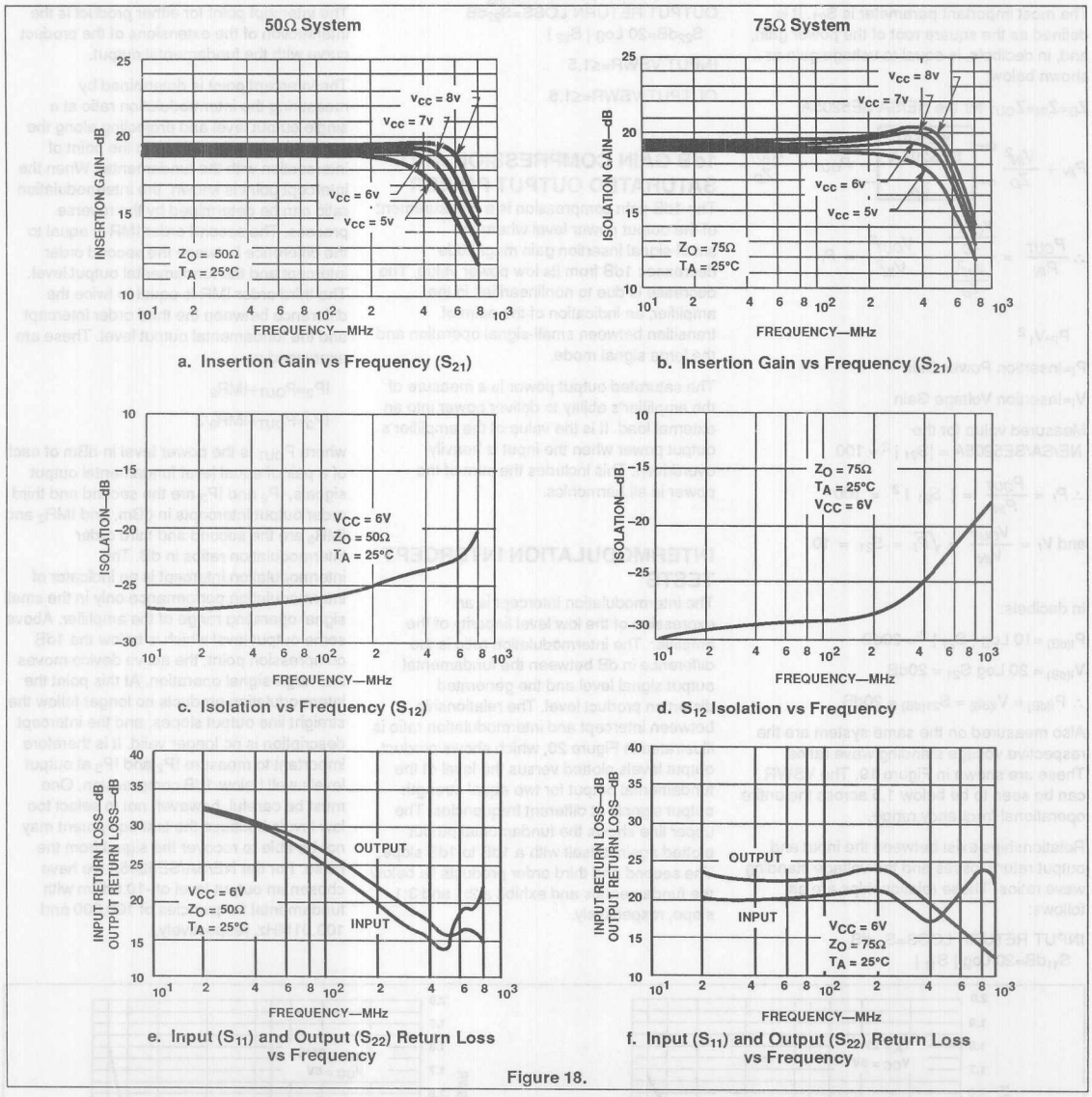
S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} = \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} = \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

Figure 17b.



a. Insertion Gain vs Frequency (S_{21})

b. Insertion Gain vs Frequency (S_{21})

c. Isolation vs Frequency (S_{12})

d. S_{12} Isolation vs Frequency

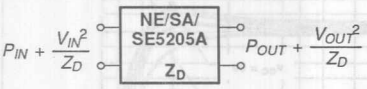
e. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

f. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 18.

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D=Z_{IN}=Z_{OUT}$ for the NE/SA/SE5205A



$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{OUT}^2}{Z_D}}{\frac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$P_I=V_I{}^2$

P_I=Insertion Power Gain

V_I=Insertion Voltage Gain

Measured value for the NE/SA/SE5205A = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

$$\text{and } V_I = \frac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20\text{dB}$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20\text{dB}$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20\text{dB}$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS=S_{11}dB

$S_{11}\text{dB}=20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS=S_{22}dB

$S_{22}\text{dB}=20 \text{ Log } |S_{22}|$

INPUT VSWR=≤1.5

OUTPUT VSWR=≤1.5

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

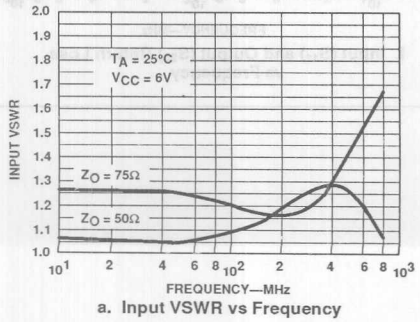
The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

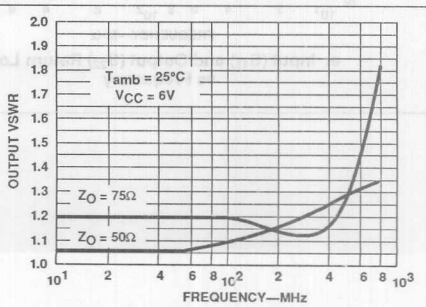
$IP_2=P_{OUT}+IMR_2$

$IP_3=P_{OUT}+IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is nc longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205A we have chosen an output level of -10.5dBm with fundamental frequencies of 100.000 and 100.01MHz, respectively.



a. Input VSWR vs Frequency



b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to High-Frequency Amplifiers by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

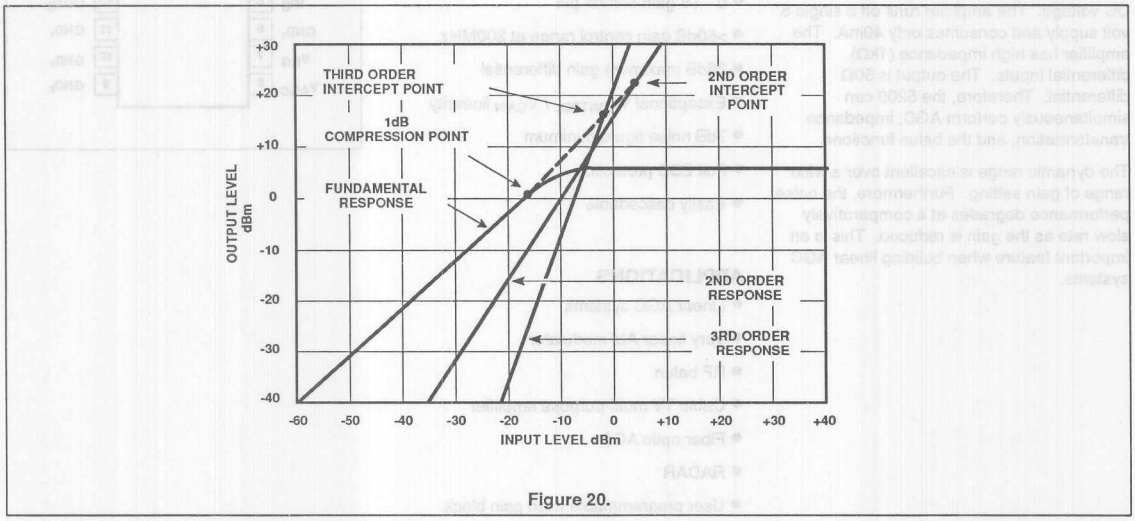


Figure 20.

Wideband variable gain amplifier NE/SA5209

DESCRIPTION

The NE5209 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5209 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5209 can simultaneously perform AGC, impedance transformation, and the balun functions.

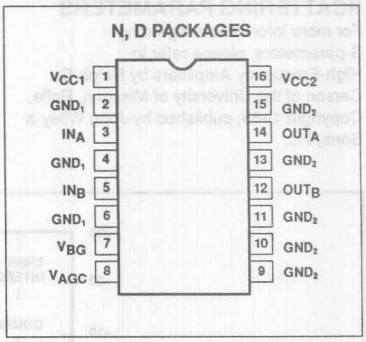
The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

FEATURES

- Gain to 1.5GHz
- 850MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

PIN CONFIGURATION

N, D PACKAGES



APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE5209D
16-Pin Plastic DIP	0 to +70°C	NE5209N
16-Pin Plastic SO	-40 to +85°C	SA5209D
16-Pin Plastic DIP	-40 to +85°C	SA5209N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   16-Pin DIP: θ_{JA} = 85°C/W
   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	V_{CC1} = V_{CC2} = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	38	43	48	mA
		Over temperature[1]	30		55	mA
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	17	19	21	dB
		Over temperature[1]	16		22	dB
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	23	25	27	dB
		Over temperature[1]	22		28	dB
R_{IN}	Input resistance (single-ended)	DC tested at ±50μA	0.9	1.2	1.5	kΩ
		Over temperature[1]	0.8		1.7	kΩ
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	40	60	75	Ω
		Over temperature[1]	35		90	Ω
V_{OS}	Output offset voltage (output referred)			±20	±100	mV
		Over temperature[1]			±250	mV
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
		Over temperature[1]	1.4		2.6	V
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
		Over temperature[1]	1.7		3.1	V
PSRR	Output offset supply rejection ratio		20	45		dB
	(output referred)	Over temperature[1]	15			dB
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
		Over temperature[1]	1.1		1.55	V

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
R_{BG}	Bandgap loading	Over temperature[1]	2	10		kΩ
V_{AGC}	AGC DC control voltage range	Over temperature[1]		0-1.3		V
I_{BAGC}	AGC pin DC bias current	0V<V_{AGC}<1.3V		-0.7	-6	µA
		Over temperature[1]			-10	µA

NOTES:

1. "Over Temperature Range" testing is as follows:
   NE is 0 to +70°C
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth		600	850		MHz
		Over temperature[1]	500			MHz
GF	Gain flatness	DC - 500MHz		±0.4		dB
		Over temperature[1]		±0.6		dB
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[2]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended) for linear operation[2]	R_L = 50Ω		400		mV_{P-P}
		R_L = 1kΩ		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	R_S = 50Ω, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		$nV/\sqrt{Hz}$
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	R_L = 50Ω		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:

1. "Over Temperature Range" testing is as follows:
   NE is 0 to +70°C
   SA is -40 to +85°C
   At the time of this data sheet release, the D package over-temperature data sheet limits are guaranteed via guardbanded room temperature testing only.
2. With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R_L = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

NE5209 APPLICATIONS

The NE5209 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 1. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5209 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output is used and properly matched, nearly 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5209 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5209 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5209 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5209. A maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5209 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path, and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5209 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5209 is shown in Figure 2. Three NE5209s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5209s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5209s will give a dynamic range in excess of 60dB.

The NE5209 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

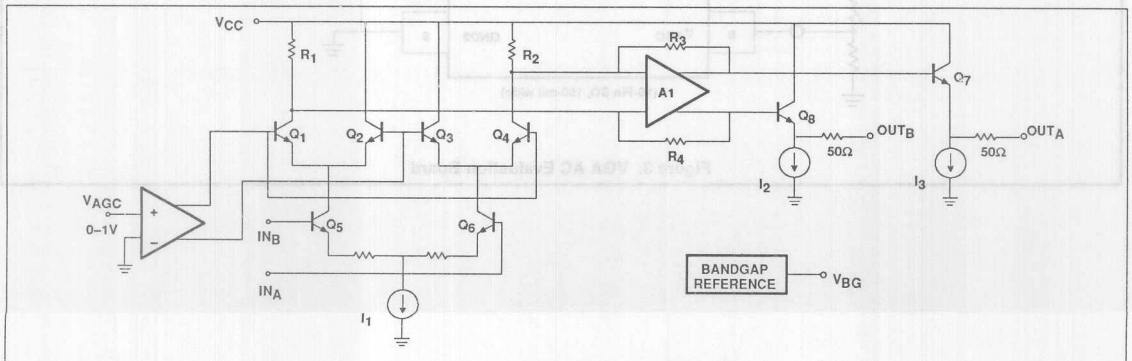


Figure 1. Equivalent Schematic of the VGA

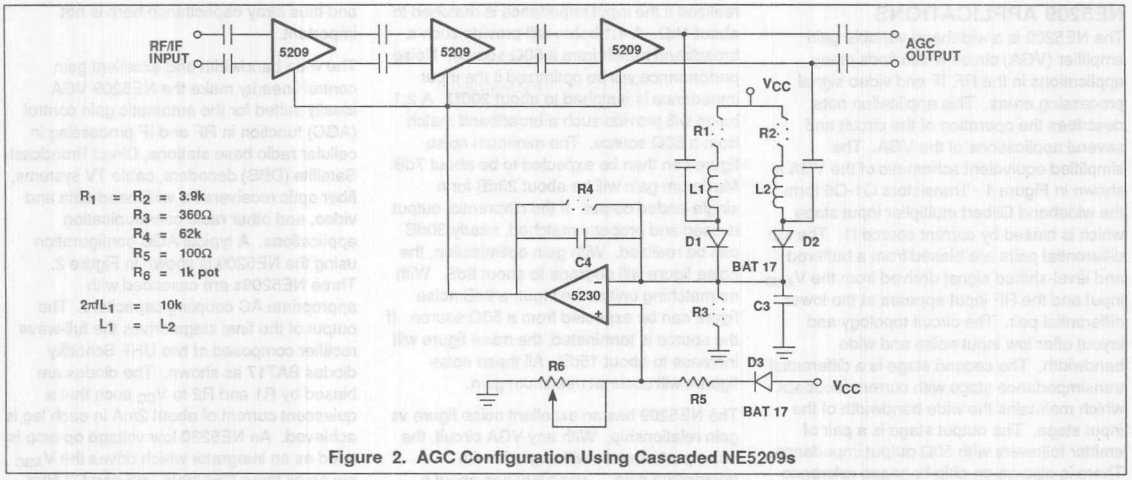


Figure 2. AGC Configuration Using Cascaded NE5209s

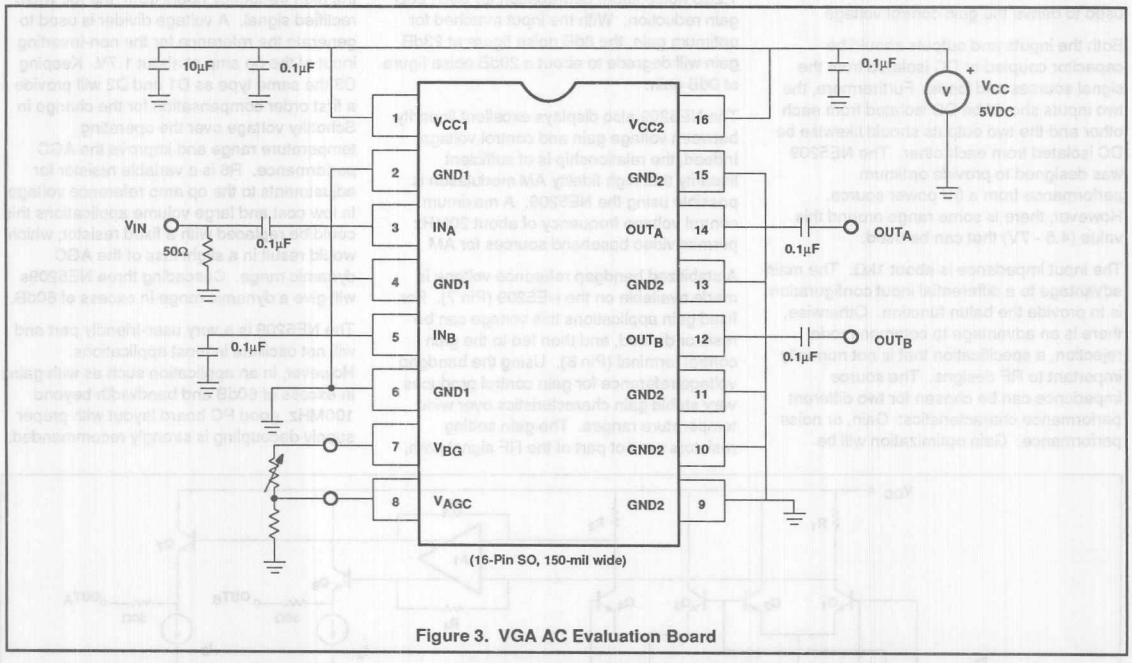
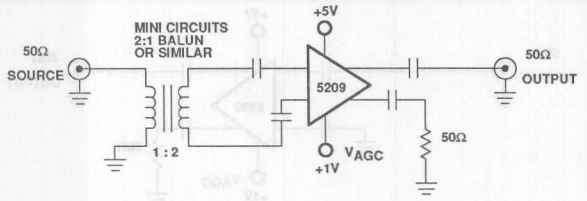
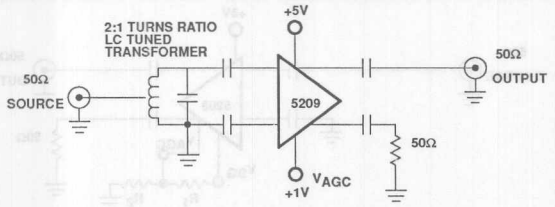


Figure 3. VGA AC Evaluation Board



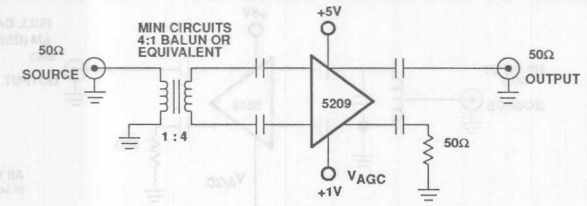
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain.

Figure 4. Broadband Noise Optimization



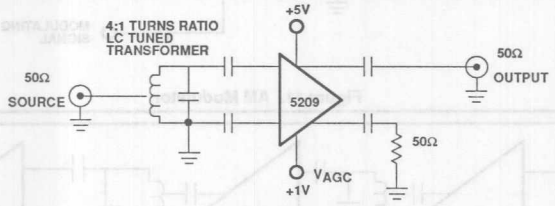
This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 5. Narrowband Noise Optimization



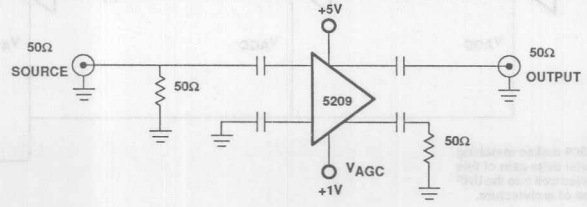
This circuit will exhibit about an 8dB noise figure with 24dB gain.

Figure 6. Broadband Gain Optimization



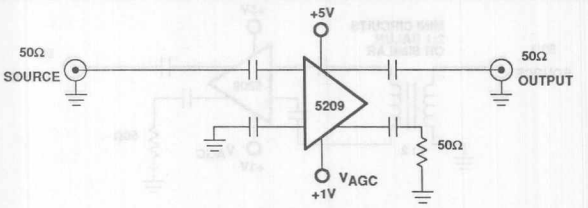
This circuit will exhibit approximately an 8dB noise figure and 25dB gain.

Figure 7. Narrowband Gain Optimization



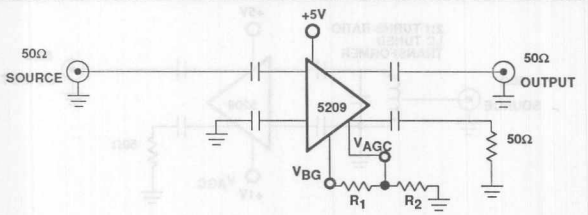
The noise figure of this configuration will be approximately 15dB.

Figure 8. Simple Amplifier Configuration



With the 50Ω source left unterminated, the noise figure is 9dB.

Figure 9 Unterminated Configuration

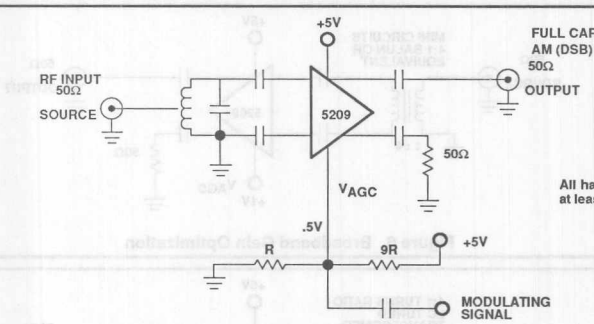


Gain = 19dB + 20log$_{10}$ V_{AGC}

where $V_{AGC} = \left[\frac{R_2}{R_1 + R_2} V_{BG}\right]$

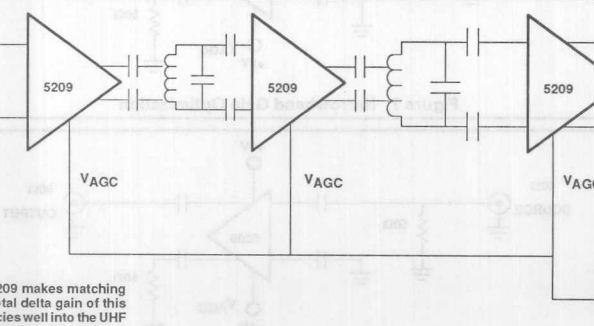
and is in units of Volts, for $V_{AGC} \leq 1V$

Figure 10. User-Programmable Fixed Gain Block



All harmonic distortion products will be at least -50dBc over the audio spectrum.

Figure 11. AM Modulator



The high input impedance to the NE5209 makes matching to crystal filters relatively easy. The total delta gain of this system will approach 80dB. IF frequencies well into the UHF region can be configured with this type of architecture.

Figure 12. Receiver AGC IF Chain

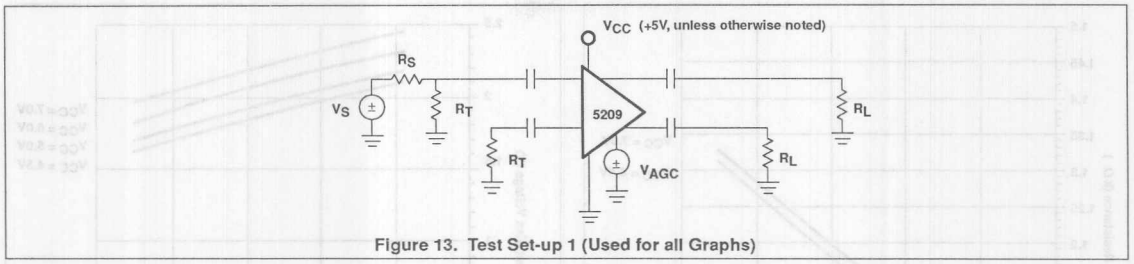


Figure 13. Test Set-up 1 (Used for all Graphs)

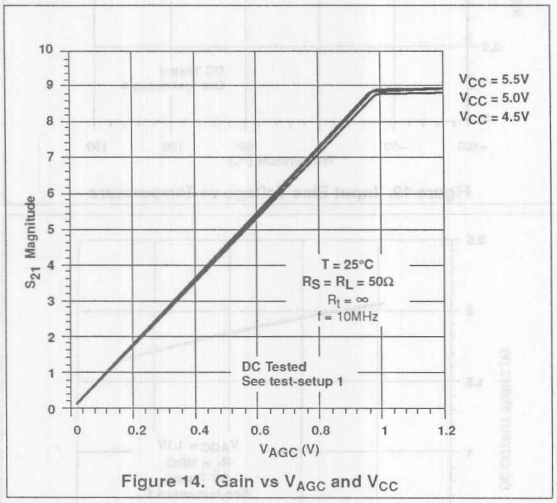


Figure 14. Gain vs V_{AGC} and V_{CC}

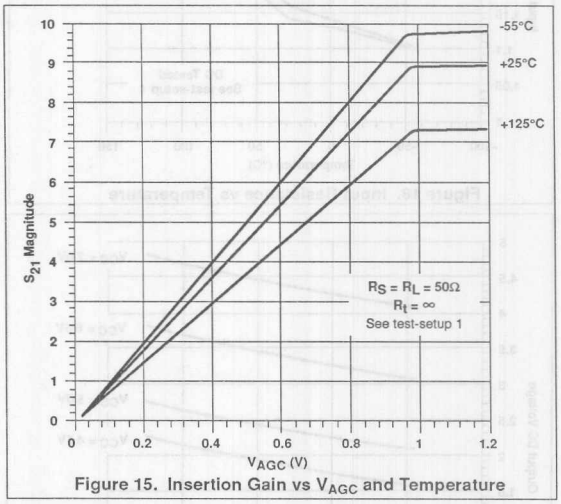


Figure 15. Insertion Gain vs V_{AGC} and Temperature

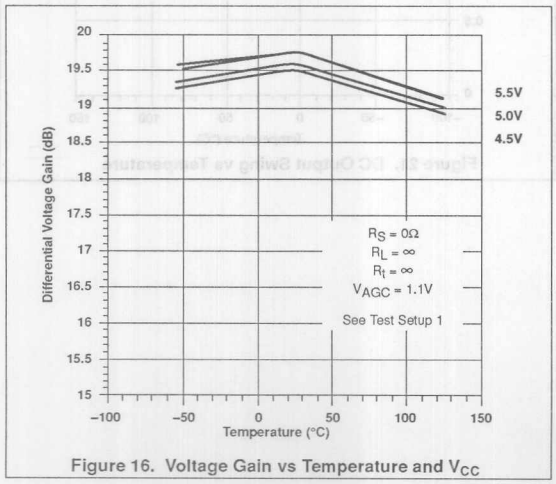


Figure 16. Voltage Gain vs Temperature and V_{CC}

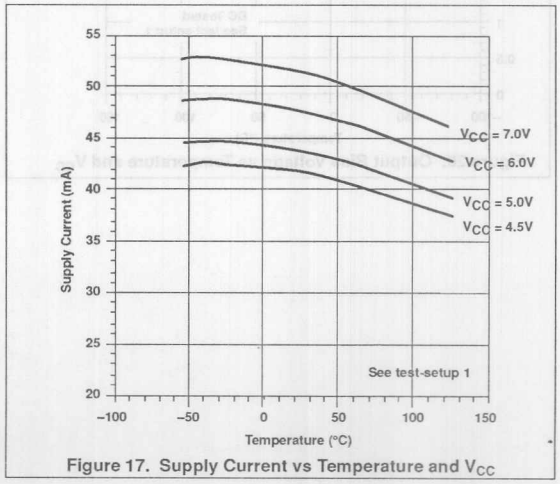


Figure 17. Supply Current vs Temperature and V_{CC}

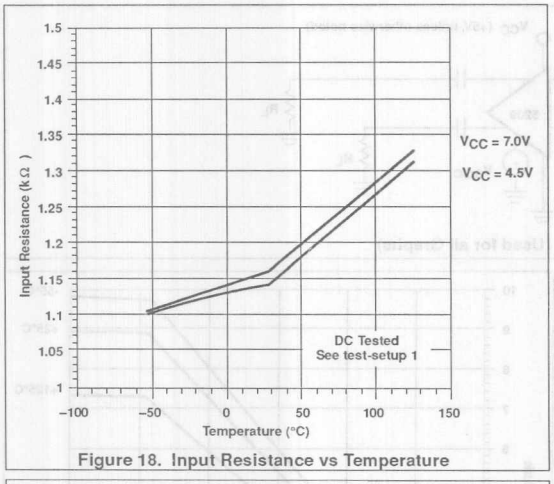


Figure 18. Input Resistance vs Temperature

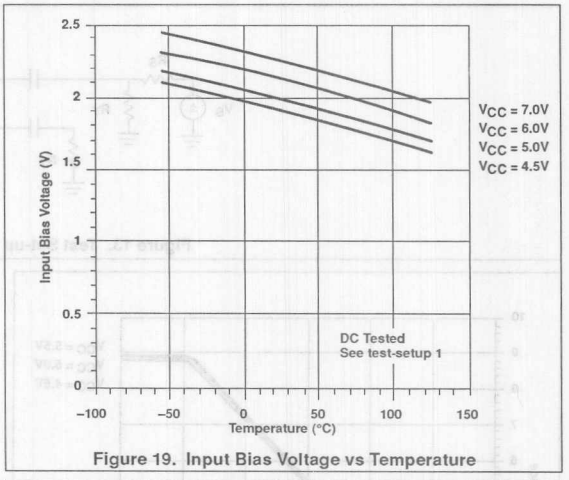


Figure 19. Input Bias Voltage vs Temperature

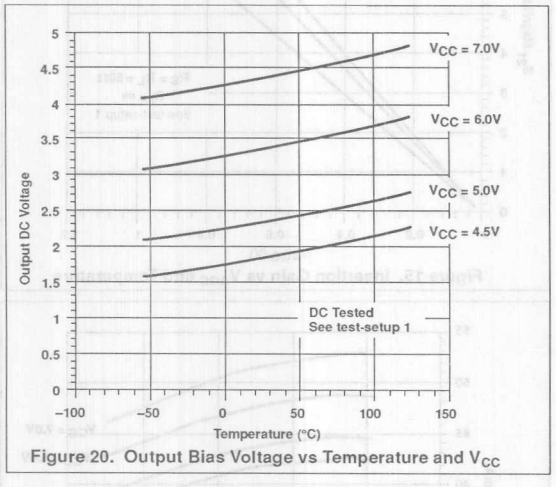


Figure 20. Output Bias Voltage vs Temperature and V_{CC}

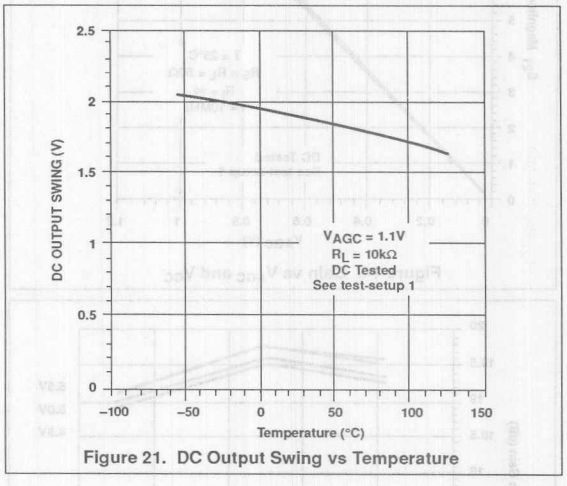


Figure 21. DC Output Swing vs Temperature

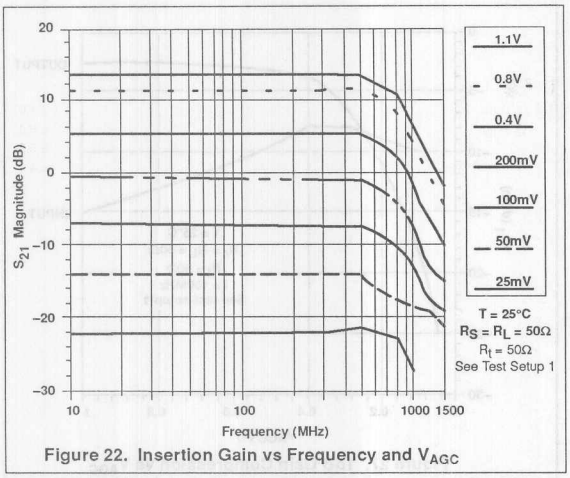


Figure 22. Insertion Gain vs Frequency and V_{AGC}

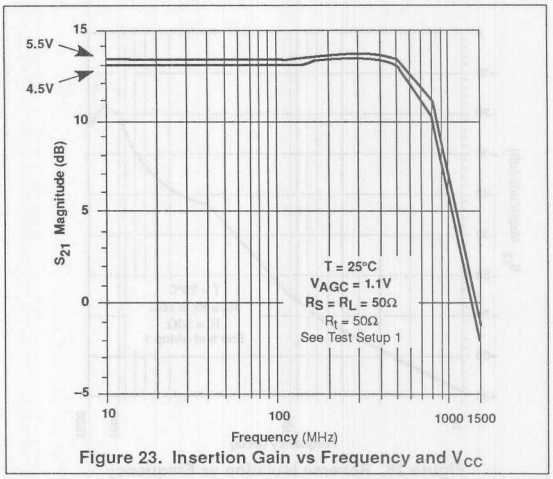


Figure 23. Insertion Gain vs Frequency and V_{CC}

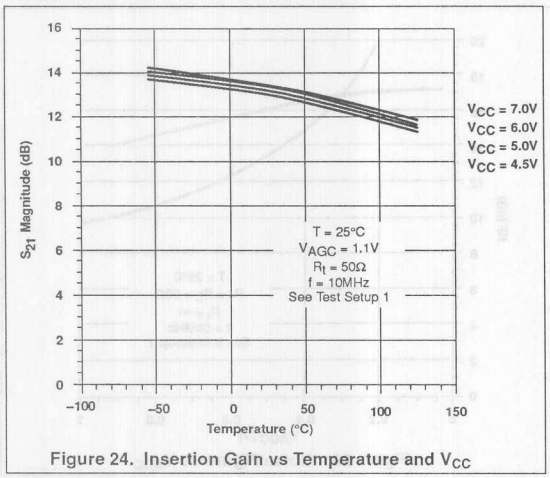


Figure 24. Insertion Gain vs Temperature and V_{CC}

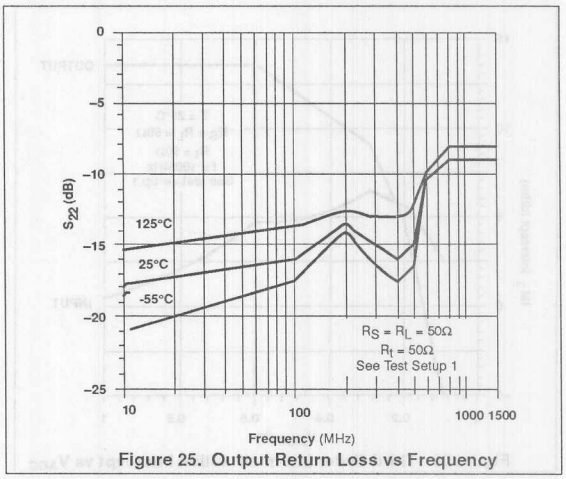


Figure 25. Output Return Loss vs Frequency

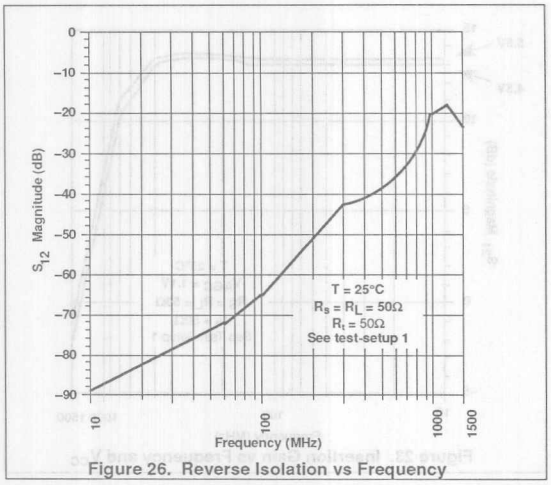


Figure 26. Reverse Isolation vs Frequency

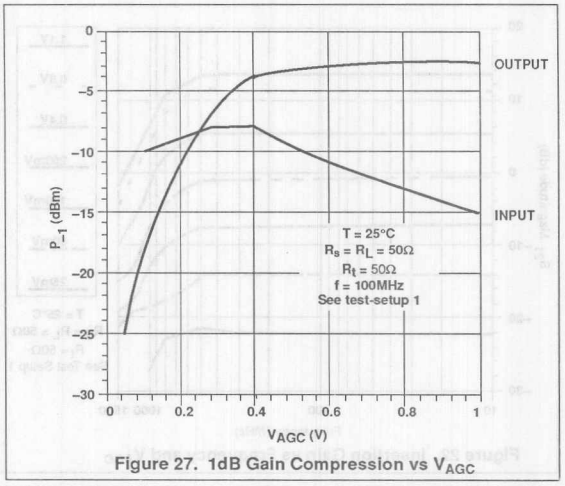


Figure 27. 1dB Gain Compression vs V_{AGC}

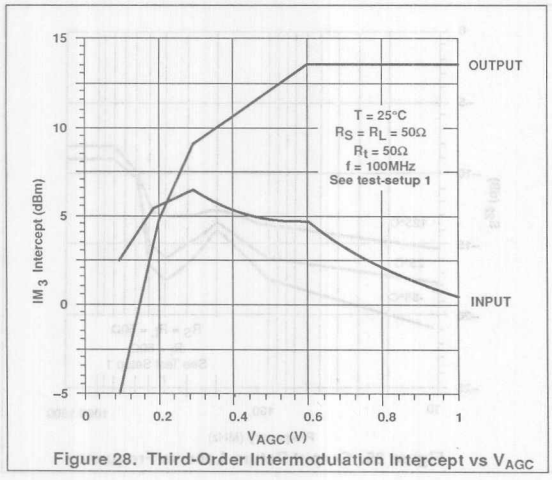


Figure 28. Third-Order Intermodulation Intercept vs V_{AGC}

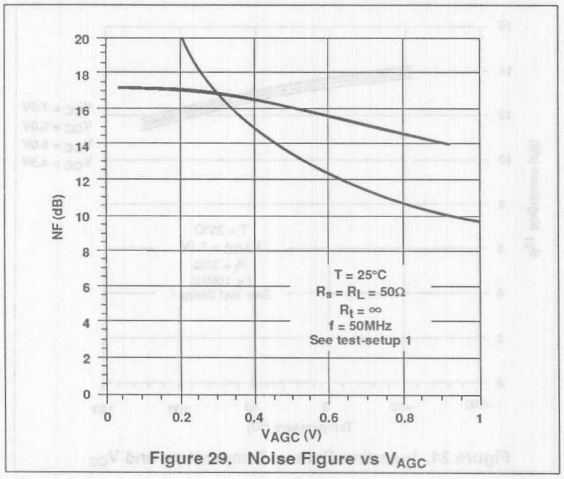


Figure 29. Noise Figure vs V_{AGC}

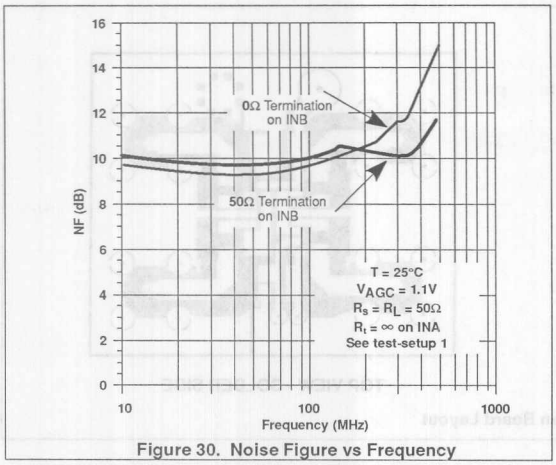


Figure 30. Noise Figure vs Frequency

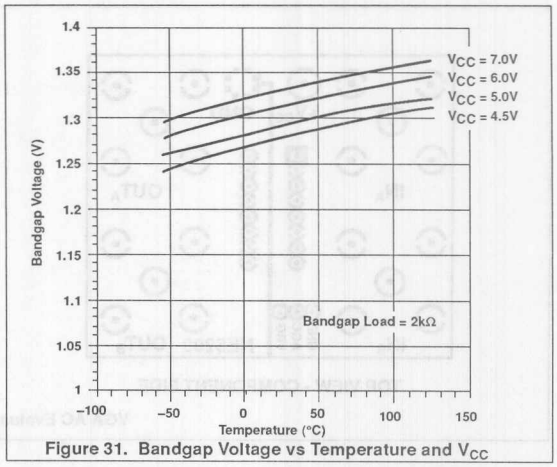


Figure 31. Bandgap Voltage vs Temperature and V_{CC}

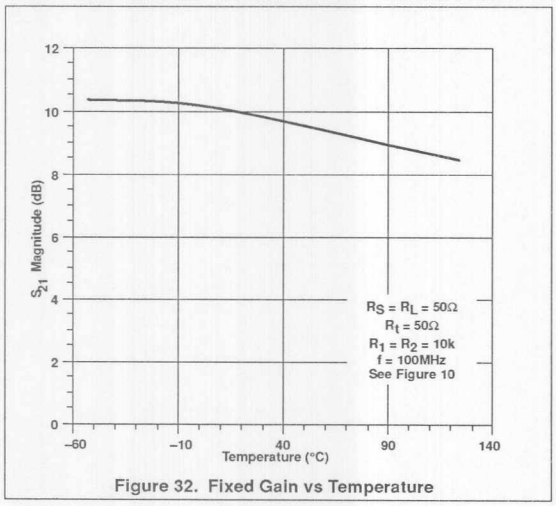
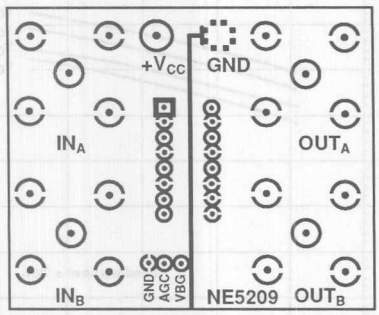
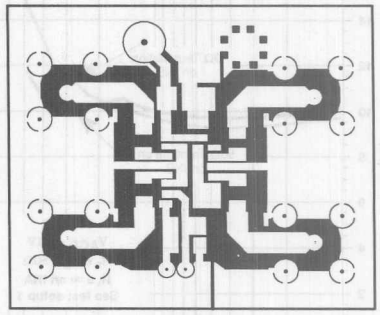


Figure 32. Fixed Gain vs Temperature

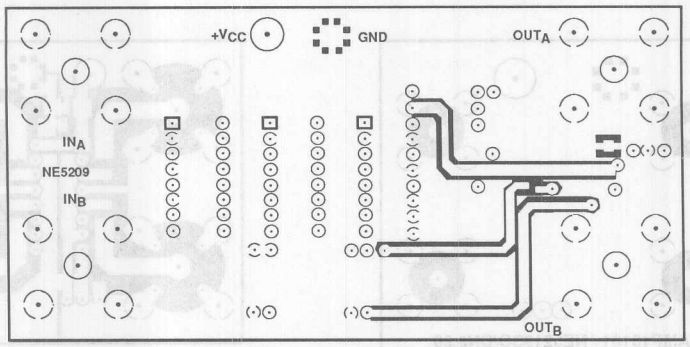


TOP VIEW - COMPONENT SIDE

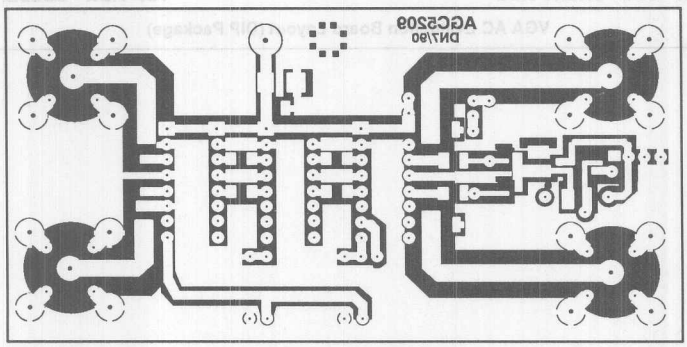


TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout

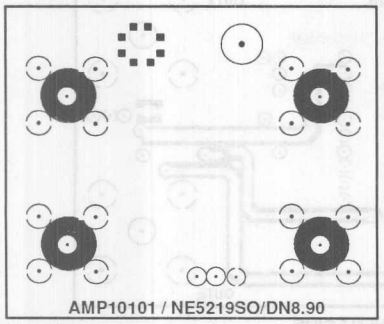


TOP VIEW - COMPONENT SIDE

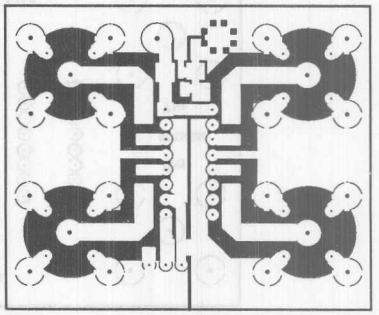


TOP VIEW - SOLDER SIDE

AGC Configuration Using Cascaded NE5209s - Layout



TOP VIEW - COMPONENT SIDE



TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout (DIP Package)

Wideband variable gain amplifier — NE/SA5219

DESCRIPTION

The NE5219 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5219 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5219 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

FEATURES

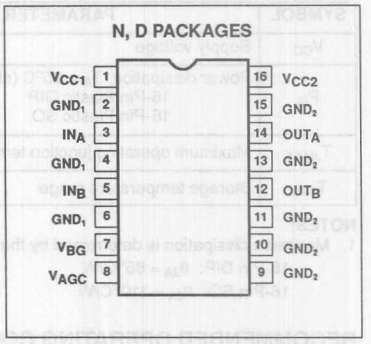
- 700MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

PIN CONFIGURATION

N, D PACKAGES



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE5219D
16-Pin Plastic DIP	0 to +70°C	NE5219N
16-Pin Plastic SO	-40 to +85°C	SA5219D
16-Pin Plastic DIP	-40 to +85°C	SA5219N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +8.0	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-Pin Plastic DIP 16-Pin Plastic SO	 1450 1100	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   16-Pin DIP: θ_{JA} = 85°C/W
   16-Pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	V_{CC1} = V_{CC2} = 4.5 to 7.0V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{CC}	Supply current	DC tested	36	43	50	mA
A_V	Voltage gain (single-ended in/single-ended out)	DC tested, R_L = 10kΩ	16	19	22	dB
A_V	Voltage gain (single-ended in/differential out)	DC tested, R_L = 10kΩ	22	25	28	dB
R_{IN}	Input resistance (single-ended)	DC tested at ±50μA	0.8	1.2	1.6	kΩ
R_{OUT}	Output resistance (single-ended)	DC tested at ±1mA	35	60	80	Ω
V_{OS}	Output offset voltage (output referred)			±20	±150	mV
V_{IN}	DC level on inputs		1.6	2.0	2.4	V
V_{OUT}	DC level on outputs		1.9	2.4	2.9	V
PSRR	Output offset supply rejection ratio		18	45		dB
V_{BG}	Bandgap reference voltage	4.5V<V_{CC}<7V R_{BG} = 10kΩ	1.2	1.32	1.45	V
R_{BG}	Bandgap loading		2	10		kΩ
V_{AGC}	AGC DC control voltage range			0-1.3		V
I_{BAGC}	AGC pin DC bias current	0V<V_{AGC}<1.3V		-0.7	-6	μA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC1} = V_{CC2} = +5.0V, V_{AGC} = 1.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
BW	-3dB bandwidth			700		MHz
GF	Gain flatness	DC - 500MHz		±0.4		dB
V_{IMAX}	Maximum input voltage swing (single-ended) for linear operation[1]			200		mV_{P-P}
V_{OMAX}	Maximum output voltage swing (single-ended)	R_L = 50Ω		400		mV_{P-P}
	for linear operation[1]	R_L = 1kΩ		1.9		V_{P-P}
NF	Noise figure (unmatched configuration)	R_S = 50Ω, f = 50MHz		9.3		dB
V_{IN-EQ}	Equivalent input noise voltage spectral density	f = 100MHz		2.5		$nV/\sqrt{Hz}$
S12	Reverse isolation	f = 100MHz		-60		dB
$\Delta G/\Delta V_{CC}$	Gain supply sensitivity (single-ended)			0.3		dB/V
$\Delta G/\Delta T$	Gain temperature sensitivity	R_L = 50Ω		0.013		dB/°C
C_{IN}	Input capacitance (single-ended)			2		pF
BW_{AGC}	-3dB bandwidth of gain control function			20		MHz
P_{O-1dB}	1dB gain compression point at output	f = 100MHz		-3		dBm
P_{I-1dB}	1dB gain compression point at input	f = 100MHz, V_{AGC} =0.1V		-10		dBm
$IP3_{OUT}$	Third-order intercept point at output	f = 100MHz, V_{AGC} >0.5V		+13		dBm
$IP3_{IN}$	Third-order intercept point at input	f = 100MHz, V_{AGC} <0.5V		+5		dBm
ΔG_{AB}	Gain match output A to output B	f = 100MHz, V_{AGC} = 1V		0.1		dB

NOTE:

1. With R_L > 1kΩ, overload occurs at input for single-ended gain < 13dB and at output for single-ended gain > 13dB. With R_L = 50Ω, overload occurs at input for single-ended gain < 6dB and at output for single-ended gain > 6dB.

NE5219 APPLICATIONS

The NE5219 is a wideband variable gain amplifier (VGA) circuit which finds many applications in the RF, IF and video signal processing areas. This application note describes the operation of the circuit and several applications of the VGA. The simplified equivalent schematic of the VGA is shown in Figure 1. Transistors Q1-Q6 form the wideband Gilbert multiplier input stage which is biased by current source I1. The top differential pairs are biased from a buffered and level-shifted signal derived from the V_{AGC} input and the RF input appears at the lower differential pair. The circuit topology and layout offer low input noise and wide bandwidth. The second stage is a differential transimpedance stage with current feedback which maintains the wide bandwidth of the input stage. The output stage is a pair of emitter followers with 50Ω output impedance. There is also an on-chip bandgap reference with buffered output at 1.3V, which can be used to derive the gain control voltage.

Both the inputs and outputs should be capacitor coupled or DC isolated from the signal sources and loads. Furthermore, the two inputs should be DC isolated from each other and the two outputs should likewise be DC isolated from each other. The NE5219 was designed to provide optimum performance from a 5V power source. However, there is some range around this value (4.5 - 7V) that can be used.

The input impedance is about 1kΩ. The main advantage to a differential input configuration is to provide the balun function. Otherwise, there is an advantage to common mode rejection, a specification that is not normally important to RF designs. The source impedance can be chosen for two different performance characteristics: Gain, or noise performance. Gain optimization will be realized if the input impedance is matched to about 1kΩ. A 4:1 balun will provide such a broadband match from a 50Ω source. Noise performance will be optimized if the input impedance is matched to about 200Ω. A 2:1 balun will provide such a broadband match from a 50Ω source. The minimum noise figure can then be expected to be about 7dB. Maximum gain will be about 23dB for a single-ended output. If the differential output *is used and properly matched, nearly* 30dB can be realized. With gain optimization, the noise figure will degrade to about 8dB. With no matching unit at the input, a 9dB noise figure can be expected from a 50Ω source. If the source is terminated, the noise figure will increase to about 15dB. All these noise figures will occur at maximum gain.

The NE5219 has an excellent noise figure vs gain relationship. With any VGA circuit, the noise performance will degrade with decreasing gain. The 5219 has about a 1.2dB noise figure degradation for each 2dB gain reduction. With the input matched for optimum gain, the 8dB noise figure at 23dB gain will degrade to about a 20dB noise figure at 0dB gain.

The NE5219 also displays excellent linearity between voltage gain and control voltage. Indeed, the relationship is of sufficient linearity that high fidelity AM modulation is possible using the NE5219. A maximum control voltage frequency of about 20MHz permits video baseband sources for AM.

A stabilized bandgap reference voltage is made available on the NE5219 (Pin 7). For fixed gain applications this voltage can be resistor divided, and then fed to the gain control terminal (Pin 8). Using the bandgap voltage reference for gain control produces very stable gain characteristics over wide temperature ranges. The gain setting resistors are not part of the RF signal path,

and thus stray capacitance here is not important.

The wide bandwidth and excellent gain control linearity make the NE5219 VGA ideally suited for the automatic gain control (AGC) function in RF and IF processing in cellular radio base stations, Direct Broadcast Satellite (DBS) decoders, cable TV systems, fiber optic receivers for wideband data and video, and other radio communication applications. A typical AGC configuration using the NE5219 is shown in Figure 2. Three NE5219s are cascaded with appropriate AC coupling capacitors. The output of the final stage drives the full-wave rectifier composed of two UHF Schottky diodes BAT17 as shown. The diodes are biased by R1 and R2 to V_{CC} such that a quiescent current of about 2mA in each leg is achieved. An NE5230 low voltage op amp is used as an integrator which drives the V_{AGC} pin on all three NE5219s. R3 and C3 filter the high frequency ripple from the full-wave rectified signal. A voltage divider is used to generate the reference for the non-inverting input of the op amp at about 1.7V. Keeping D3 the same type as D1 and D2 will provide a first order compensation for the change in Schottky voltage over the operating temperature range and improve the AGC performance. R6 is a variable resistor for adjustments to the op amp reference voltage. In low cost and large volume applications this could be replaced with a fixed resistor, which would result in a slight loss of the AGC dynamic range. Cascading three NE5219s will give a dynamic range in excess of 60dB.

The NE5219 is a very user-friendly part and will not oscillate in most applications. However, in an application such as with gains in excess of 60dB and bandwidth beyond 100MHz, good PC board layout with proper supply decoupling is strongly recommended.

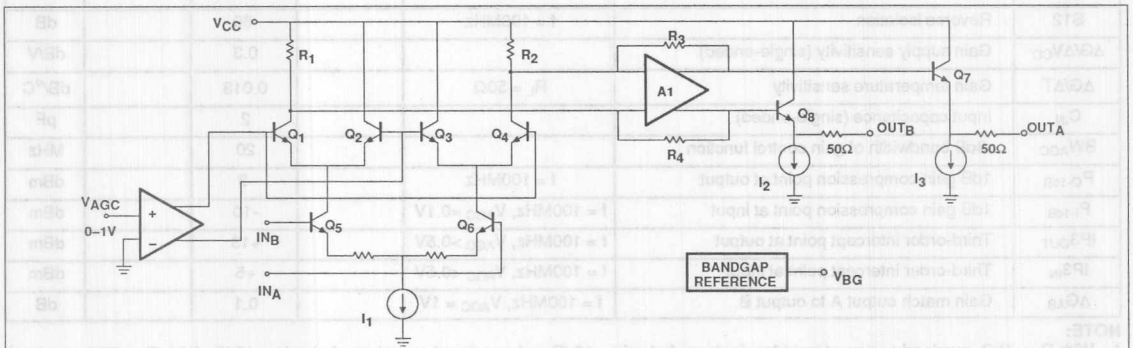


Figure 1. Equivalent Schematic of the VGA

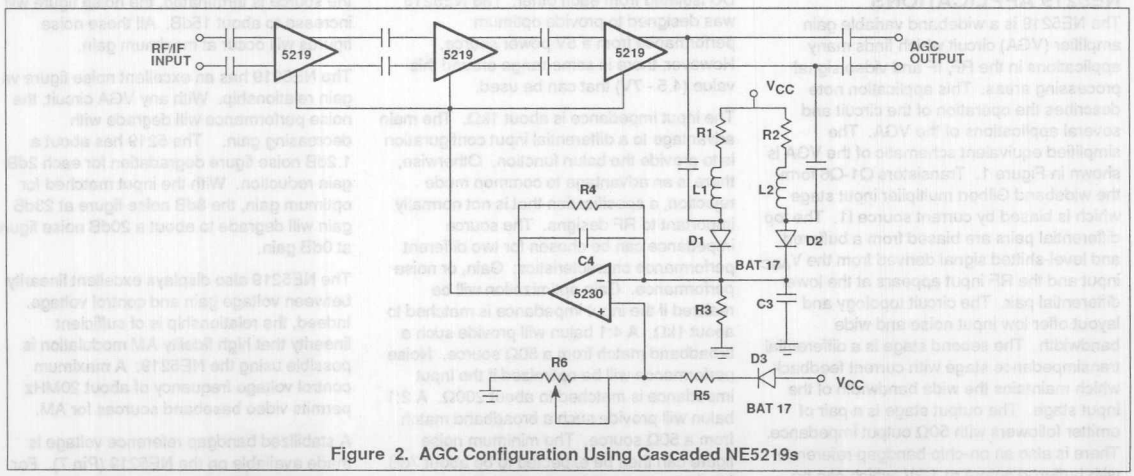


Figure 2. AGC Configuration Using Cascaded NE5219s

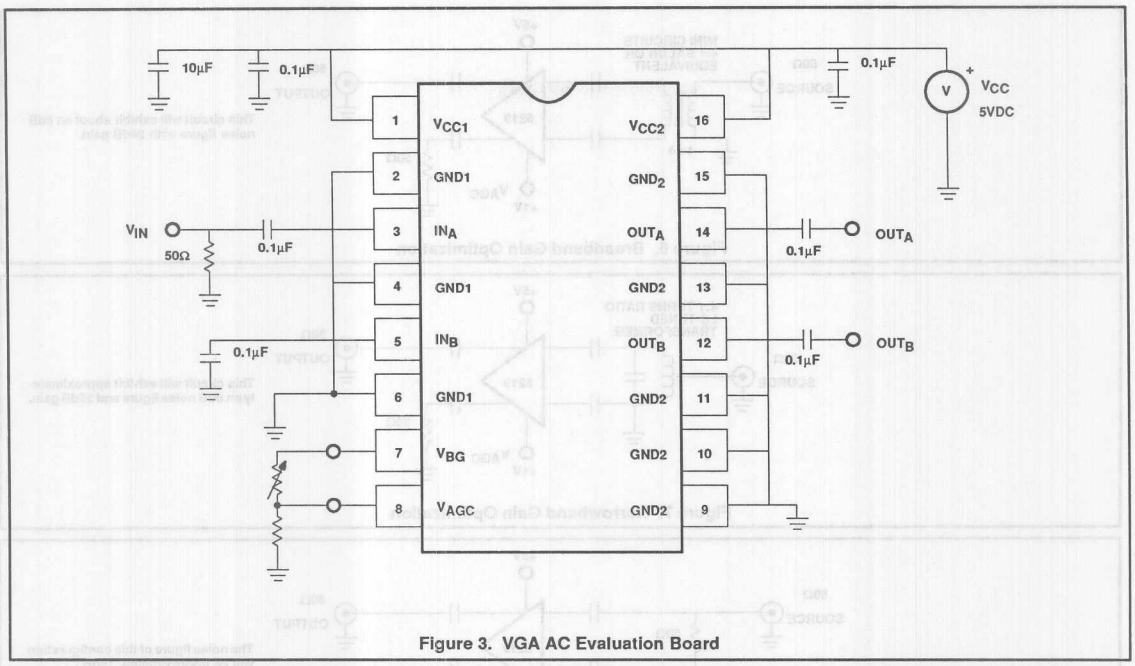
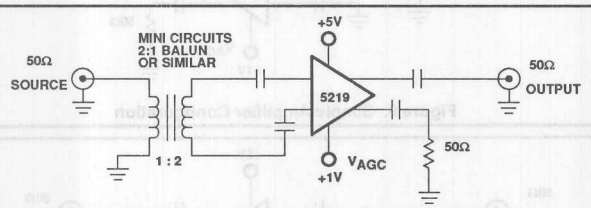
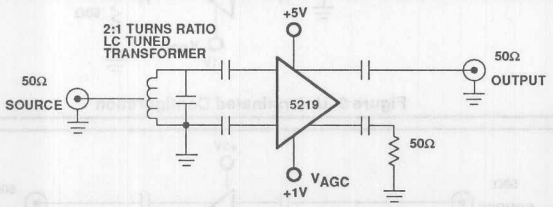


Figure 3. VGA AC Evaluation Board



This circuit will exhibit about a 7dB noise figure with approximately 22dB gain.

Figure 4. Broadband Noise Optimization



This circuit will exhibit about a 7dB noise figure with approximately 22dB gain. Narrowband circuits have the advantage of greater stability, particularly when multiple devices are cascaded.

Figure 5. Narrowband Noise Optimization

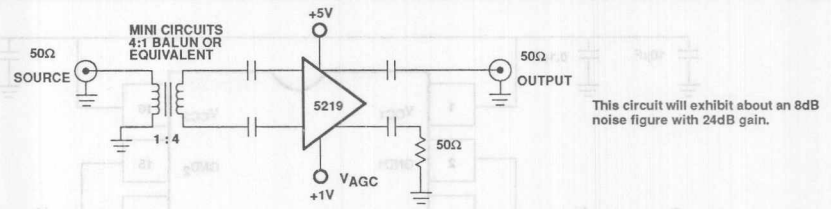


Figure 6. Broadband Gain Optimization

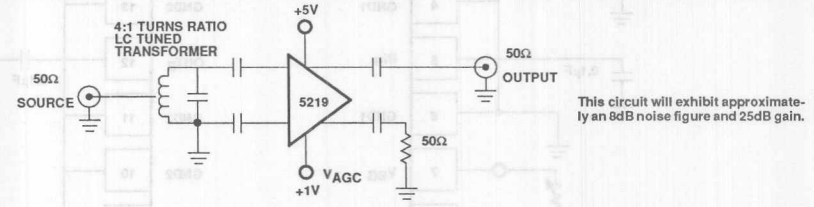


Figure 7. Narrowband Gain Optimization

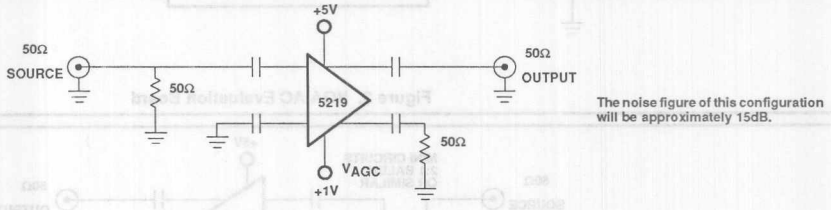


Figure 8. Simple Amplifier Configuration

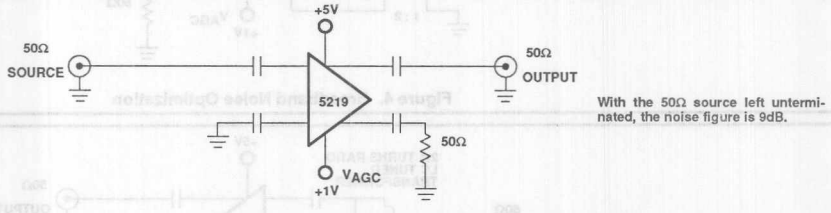


Figure 9 Unterminated Configuration

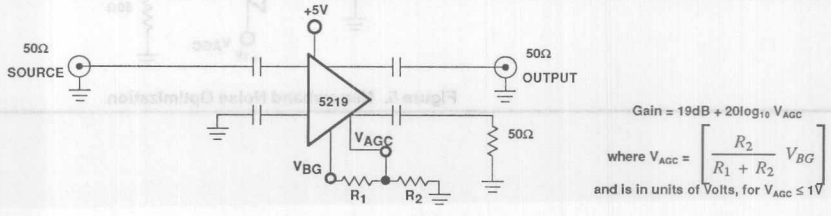


Figure 10. User-Programmable Fixed Gain Block

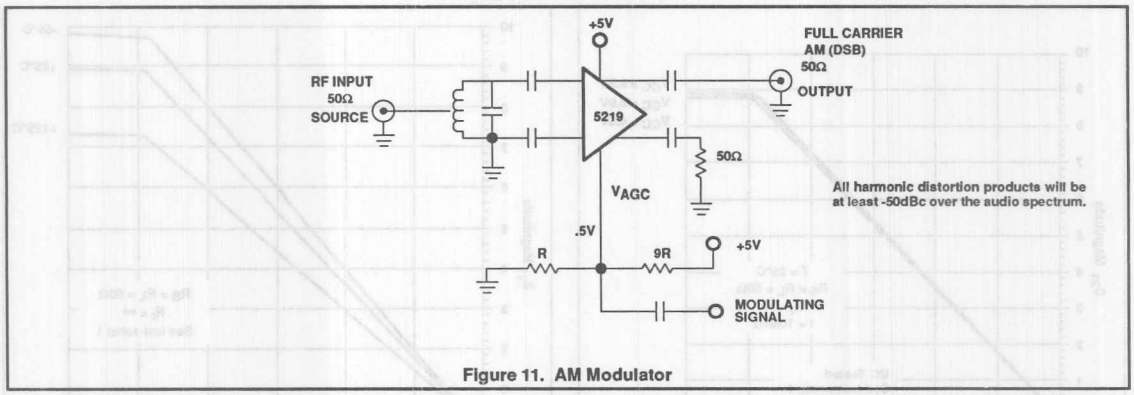


Figure 11. AM Modulator

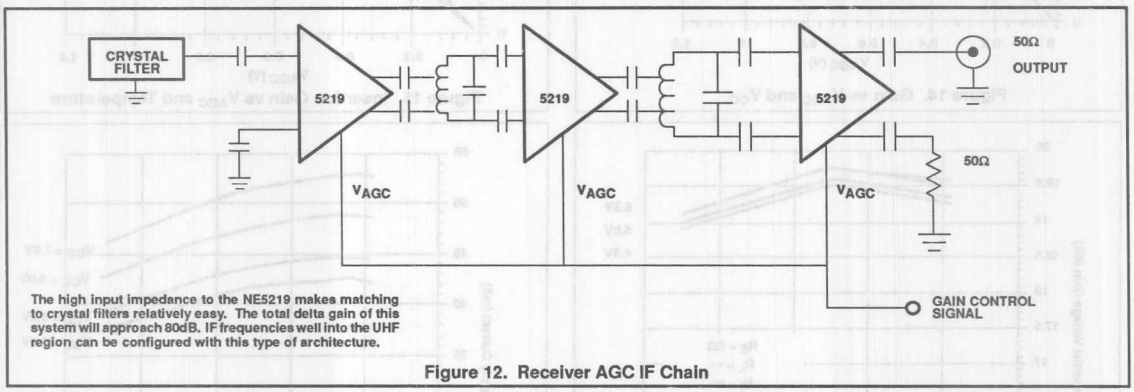


Figure 12. Receiver AGC IF Chain

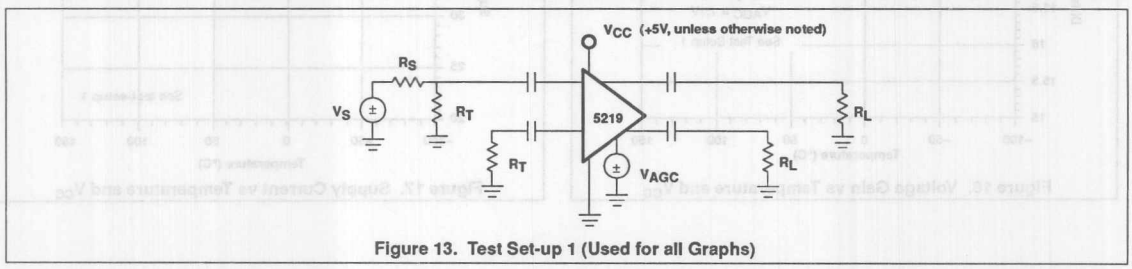


Figure 13. Test Set-up 1 (Used for all Graphs)

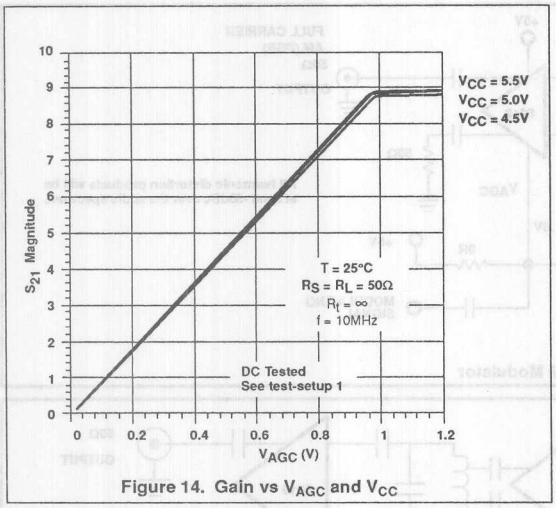


Figure 14. Gain vs V_{AGC} and V_{CC}

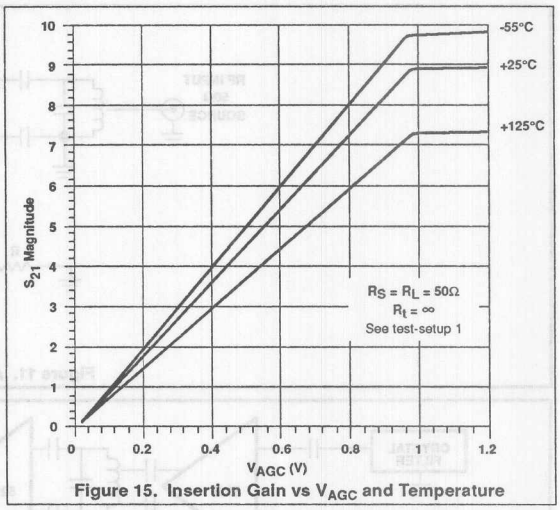


Figure 15. Insertion Gain vs V_{AGC} and Temperature

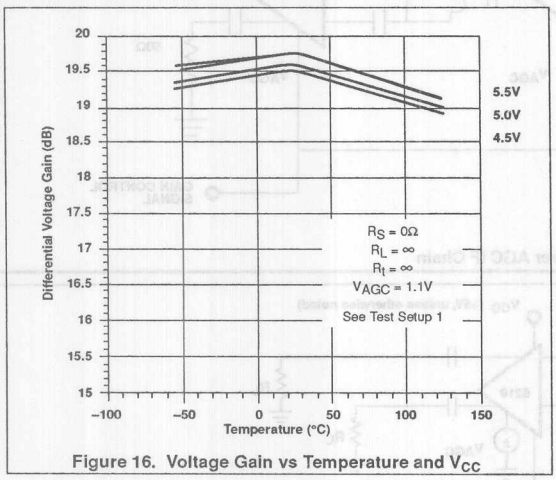


Figure 16. Voltage Gain vs Temperature and V_{CC}

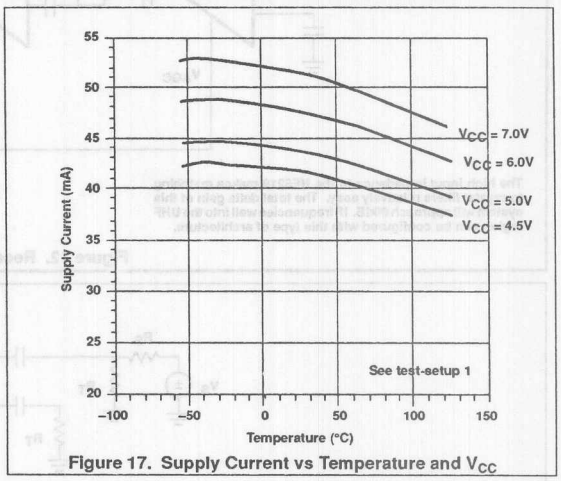


Figure 17. Supply Current vs Temperature and V_{CC}

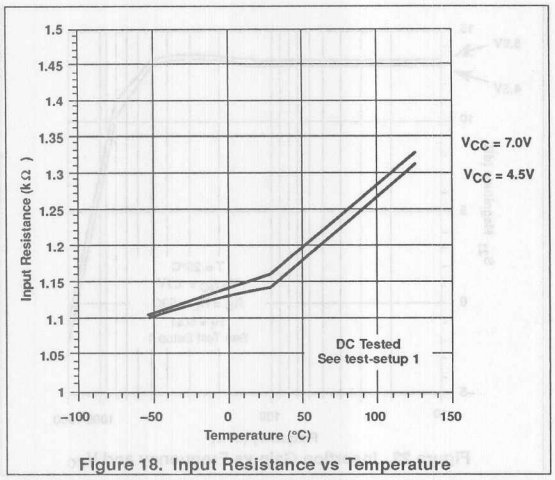


Figure 18. Input Resistance vs Temperature

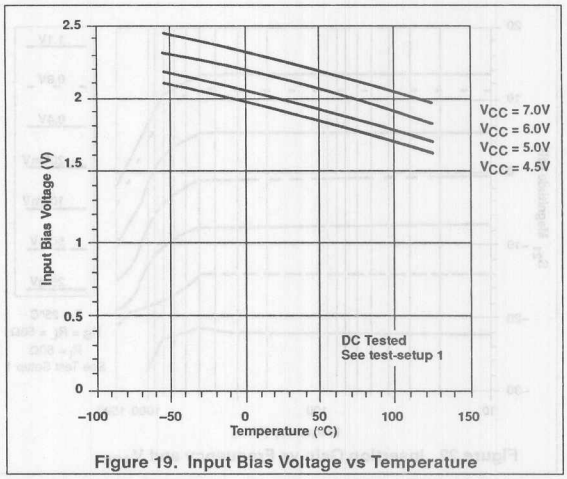


Figure 19. Input Bias Voltage vs Temperature

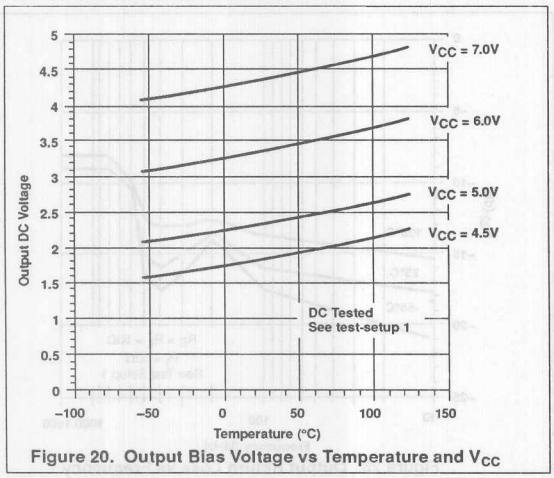


Figure 20. Output Bias Voltage vs Temperature and V_{CC}

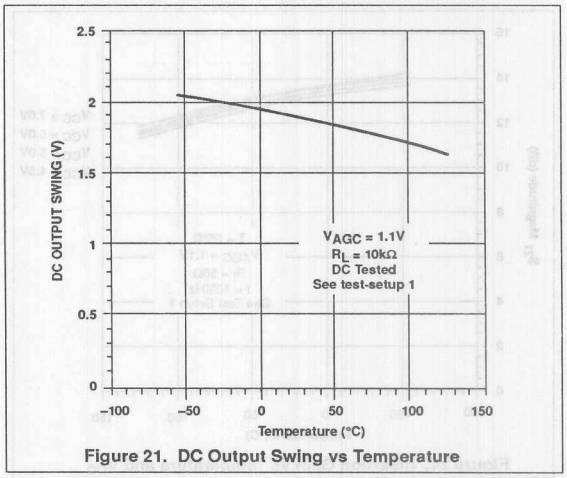


Figure 21. DC Output Swing vs Temperature

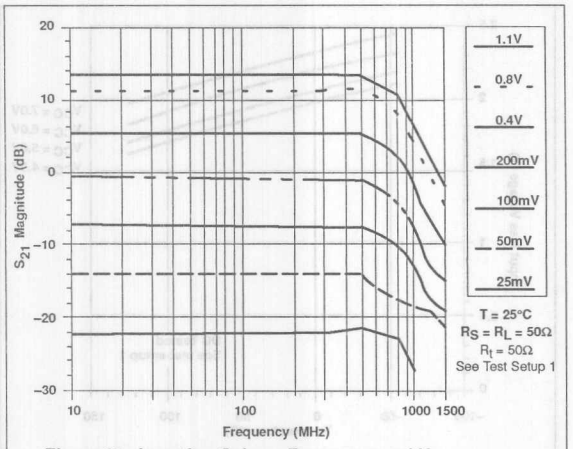


Figure 22. Insertion Gain vs Frequency and V_{AGC}

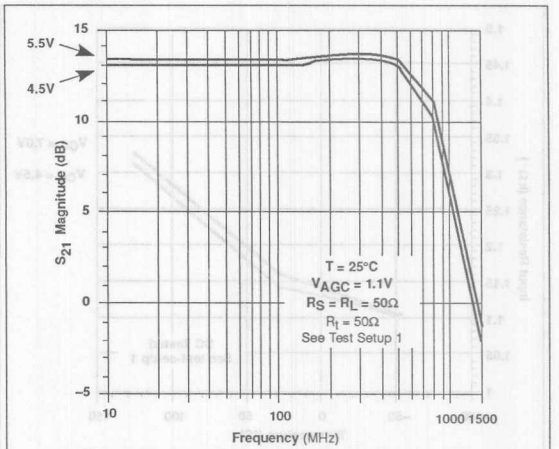


Figure 23. Insertion Gain vs Frequency and V_{CC}

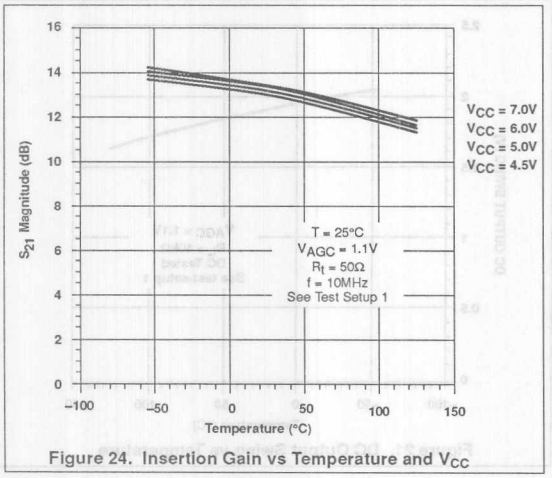


Figure 24. Insertion Gain vs Temperature and V_{CC}

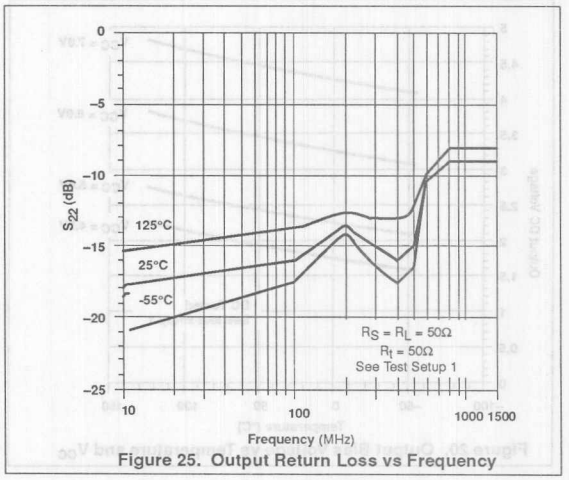


Figure 25. Output Return Loss vs Frequency

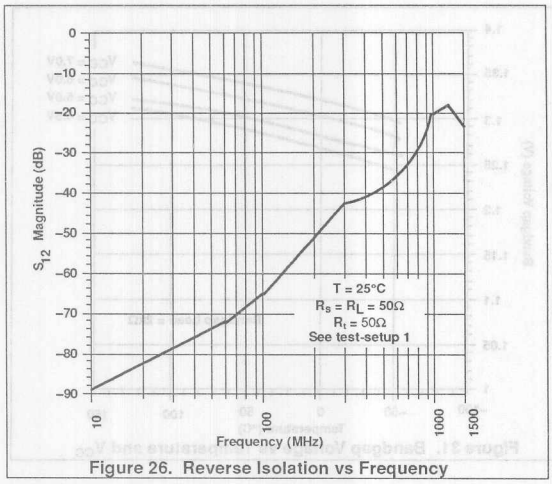


Figure 26. Reverse Isolation vs Frequency

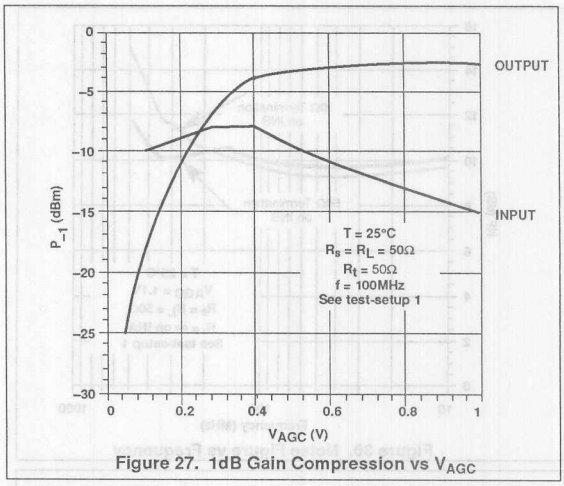


Figure 27. 1dB Gain Compression vs V_{AGC}

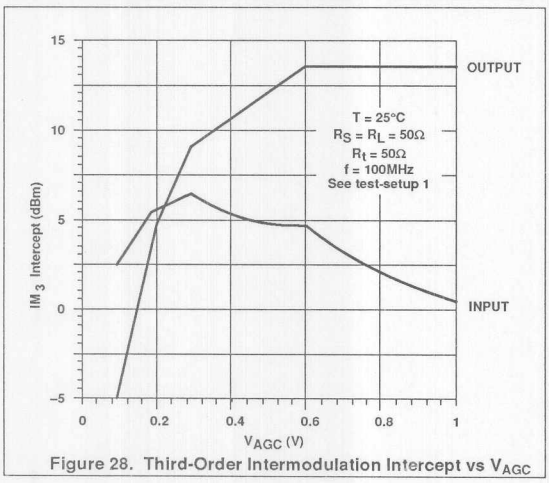


Figure 28. Third-Order Intermodulation Intercept vs V_{AGC}

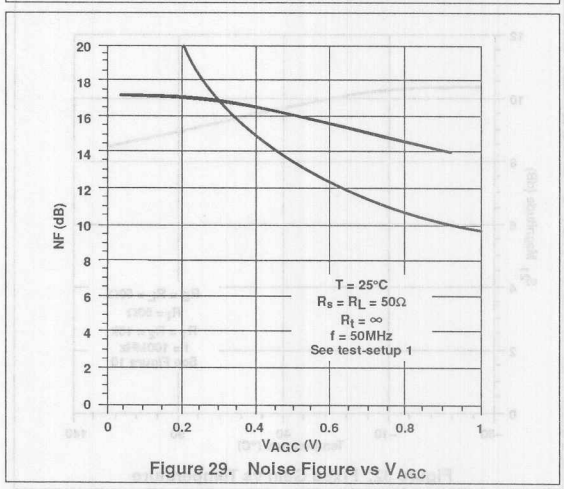


Figure 29. Noise Figure vs V_{AGC}

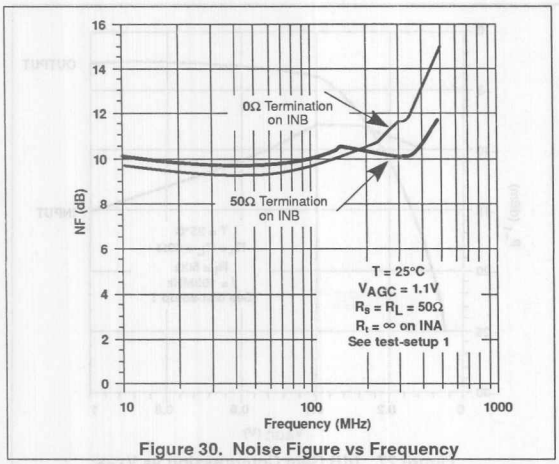


Figure 30. Noise Figure vs Frequency

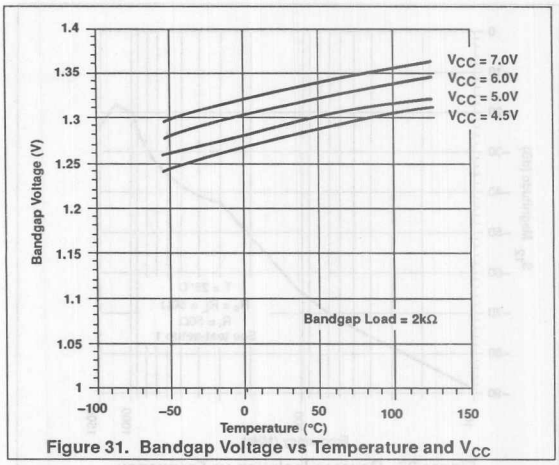


Figure 31. Bandgap Voltage vs Temperature and V_{CC}

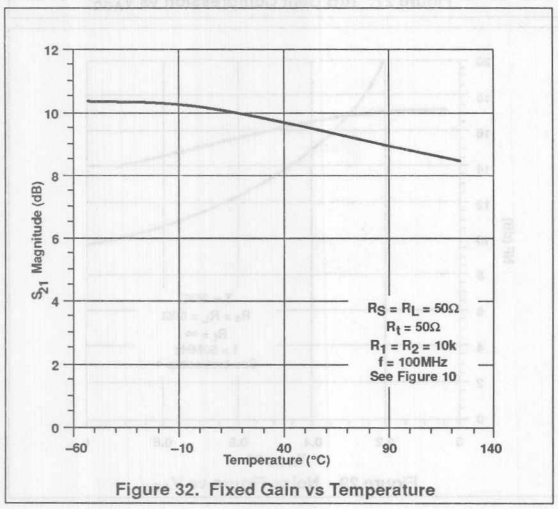
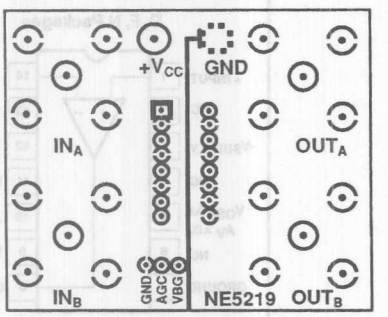
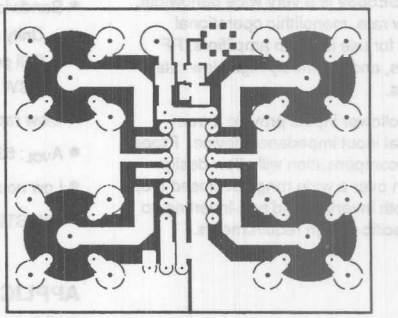


Figure 32. Fixed Gain vs Temperature

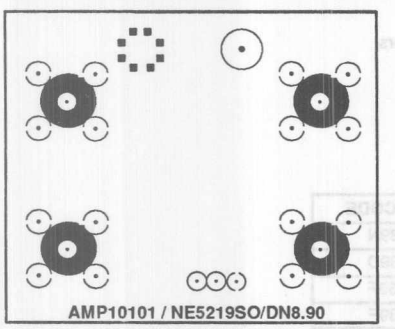


TOP VIEW - COMPONENT SIDE

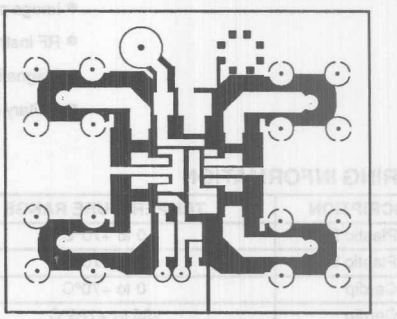


TOP VIEW - SOLDER SIDE

VGA AC Evaluation Board Layout (DIP Package)



BOTTOM VIEW - D Package



TOP VIEW - D Package

VGA AC Evaluation Board Layout (SO Package)

High frequency operational amplifier — NE/SE5539

DESCRIPTION

The NE/SE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

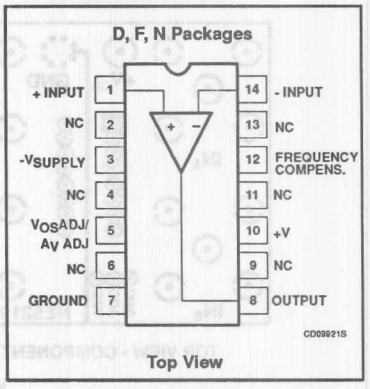
FEATURES

- Bandwidth
  - Unity gain - 350MHz
  - Full power - 48MHz
  - GBW - 1.2GHz at 17dB
- Slew rate: 600/Vμs
- A_{VOL}: 52dB typical
- Low noise - 4nV√Hz typical
- MIL-STD processing available

APPLICATIONS

- High speed datacom
- Video monitors & TV
- Satellite communications
- Image processing
- RF instrumentation & oscillators
- Magnetic storage
- Military communications

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5539N
14-Pin Plastic SO	0 to +70°C	NE5539D
14-Pin Cerdip	0 to +70°C	NE5539F
14-Pin Cerdip	-55 to +125°C	SE5539F

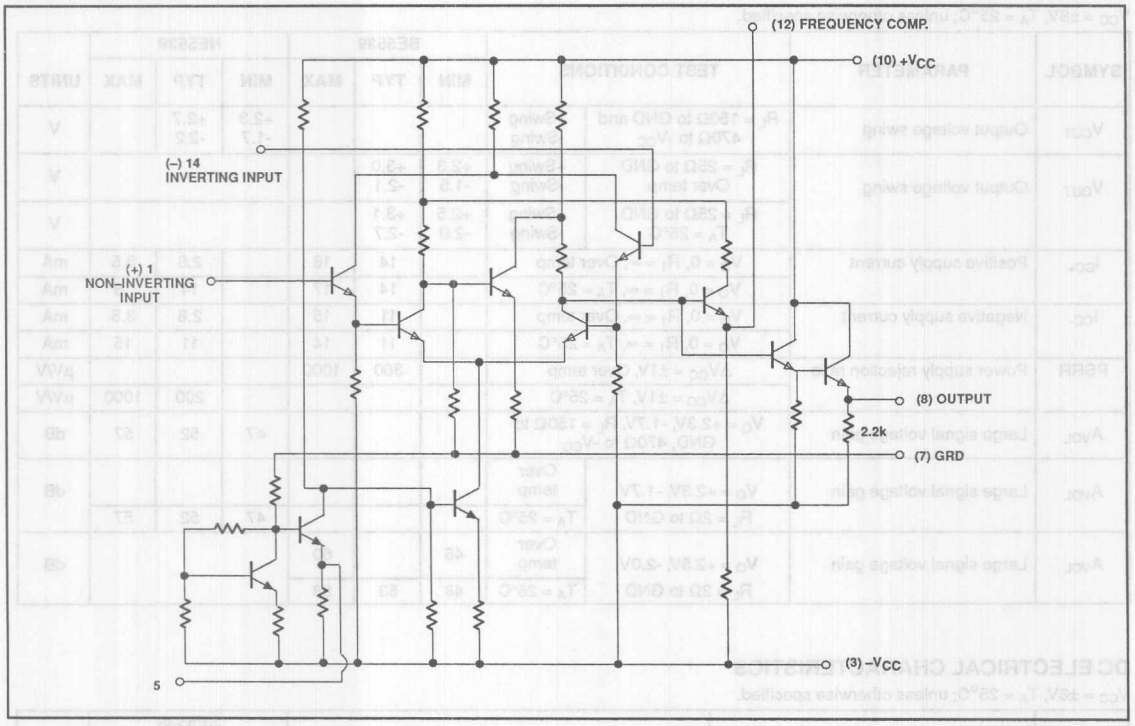
ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	±12	V
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[2] F package N package D package	 1.17 1.45 0.99	 W W W
T_A	Operating temperature range NE SE	 0 to 70 -55 to +125	 °C °C
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Max junction temperature	150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

1. Differential input voltage should not exceed 0.25V to prevent excesive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.
2. Derate above 25°C, at the following rates:
   F package at 9.3mW/°C
   N package at 11.6mW/°C
   D package at 7.9mW/°C

EQUIVALENT CIRCUIT



High frequency operational amplifier — NE/SE5539

DC ELECTRICAL CHARACTERISTICS

V_{CC} = ±8V, T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539 MIN	SE5539 TYP	SE5539 MAX	NE5539 MIN	NE5539 TYP	NE5539 MAX	UNITS
V_{OUT}	Output voltage swing	R_L = 150Ω to GND and 470Ω to -V_{CC}	+Swing -Swing				+2.3 -1.7	+2.7 -2.2		V
V_{OUT}	Output voltage swing	R_L = 25Ω to GND Over temp	+Swing -Swing	+2.3 -1.5	+3.0 -2.1					V
		R_L = 25Ω to GND T_A = 25°C	+Swing -Swing	+2.5 -2.0	+3.1 -2.7					V
I_{CC+}	Positive supply current	V_O = 0, R_1 = ∞, Over temp			14	18		2.8	3.5	mA
		V_O = 0, R_1 = ∞, T_A = 25°C			14	17		14	18	mA
I_{CC-}	Negative supply current	V_O = 0, R_1 = ∞, Over temp			11	15		2.8	3.5	mA
		V_O = 0, R_1 = ∞, T_A = 25°C			11	14		11	15	mA
PSRR	Power supply rejection ratio	ΔV_{CC} = ±1V, Over temp			300	1000				µV/V
		ΔV_{CC} = ±1V, T_A = 25°C						200	1000	µV/V
A_{VOL}	Large signal voltage gain	V_O = +2.3V, -1.7V, R_L = 150Ω to GND, 470Ω to -V_{CC}					47	52	57	dB
A_{VOL}	Large signal voltage gain	V_O = +2.3V, -1.7V	Over temp							dB
		R_L = 2Ω to GND	T_A = 25°C				47	52	57	
A_{VOL}	Large signal voltage gain	V_O = +2.5V, -2.0V	Over temp	46		60				dB
		R_L = 2Ω to GND	T_A = 25°C	48	53	58				

DC ELECTRICAL CHARACTERISTICS

V_{CC} = ±6V, T_A = 25°C; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			SE5539 MIN	SE5539 TYP	SE5539 MAX	UNITS
V_{OS}	Input offset voltage			Over temp		2	5	mV
				T_A = 25°C		2	3	
I_{OS}	Input offset current			Over temp		0.1	3	µA
				T_A = 25°C		0.1	1	
I_B	Input bias current			Over temp		5	20	µA
				T_A = 25°C		4	10	
CMRR	Common-mode rejection ratio	V_{CM} = ±1.3V, R_S = 100Ω			70	85		dB
I_{CC+}	Positive supply current			Over temp		11	14	mA
				T_A = 25°C		11	13	
I_{CC-}	Negative supply current			Over temp		8	11	mA
				T_A = 25°CmA		8	10	
PSRR	Power supply rejection ratio	ΔV_{CC} = ±1V		Over temp		300	1000	µV/V
				T_A = 25°C				
V_{OUT}	Output voltage swing	R_L = 150Ω to GND and 390Ω to –V_{CC}	Over temp	+Swing	+1.4	+2.0		V
				–Swing	–1.1	–1.7		
			T_A = 25°C	+Swing	+1.5	+2.0		
				–Swing	–1.4	–1.8		

AC ELECTRICAL CHARACTERISTICS

V_{CC} = ±8V, R_L = 150Ω to GND and 470Ω to -V_{CC}, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
BW	Gain bandwidth product	A_{CL} = 7, V_O = 0.1 V_{P-P}		1200			1200		MHz
	Small signal bandwidth	A_{CL} = 2, R_L = 150Ω[1]		110			110		MHz
t_S	Settling time	A_{CL} = 2, R_L = 150Ω[1]		15			15		ns
SR	Slew rate	A_{CL} = 2, R_L = 150Ω[1]		600			600		V/µs
t_{PD}	Propagation delay	A_{CL} = 2, R_L = 150Ω[1]		7			7		ns
	Full power response	A_{CL} = 2, R_L = 150Ω[1]		48			48		MHz
	Full power response	A_V = 7, R_L = 150Ω[1]		20			20		MHz
	Input noise voltage	R_S = 50Ω, 1MHz		4			4		nV/√Hz
	Input noise current	1MHz		6			6		pA/√Hz

NOTES:
1. External compensation.

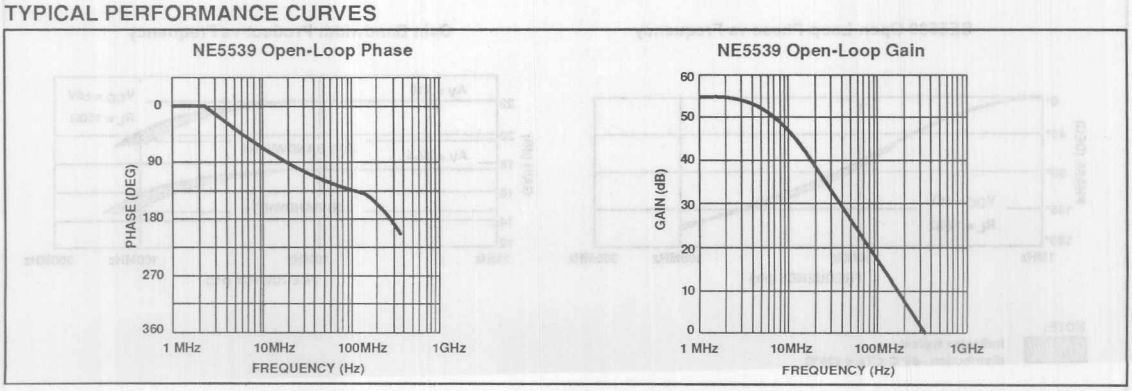
AC ELECTRICAL CHARACTERISTICS

V_{CC} = ±6V, R_L = 150Ω to GND and 390Ω to -V_{CC}, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNITS
			MIN	TYP	MAX	
BW	Gain bandwidth product	A_{CL} = 7		700		MHz
	Small signal bandwidth	A_{CL} = 2[1]		120		MHz
t_S	Settling time	A_{CL} = 2[1]		23		ns
SR	Slew rate	A_{CL} = 2[1]		330		V/µs
t_{PD}	Propagation delay	A_{CL} = 2[1]		4.5		ns
	Full power response	A_{CL} = 2[1]		20		MHz

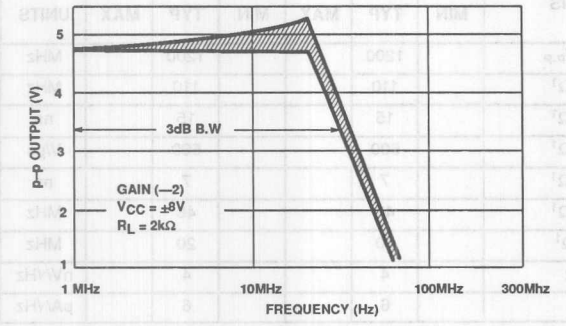
NOTES:
1. External compensation.

TYPICAL PERFORMANCE CURVES

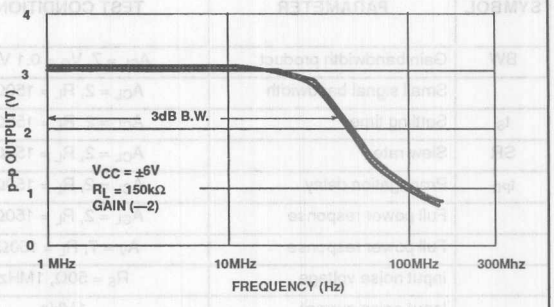


TYPICAL PERFORMANCE CURVES (Continued)

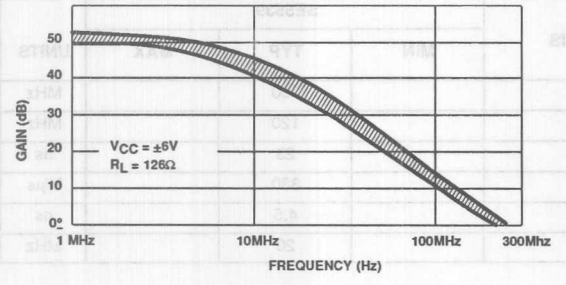
Power Bandwidth (SE)



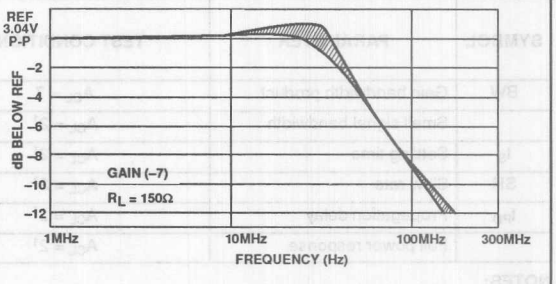
Power Bandwidth (NE)



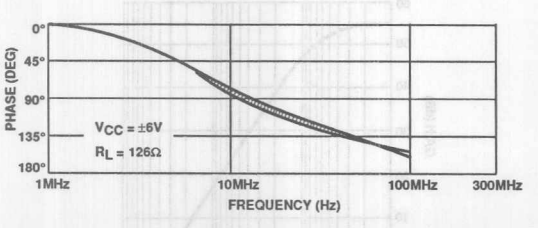
SE5539 Open-Loop Gain vs Frequency



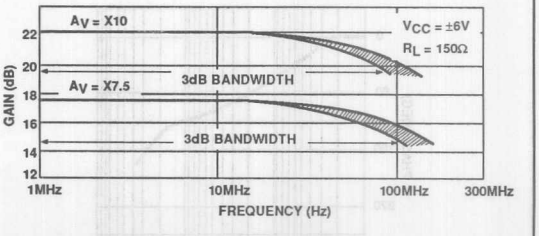
Power Bandwidth



SE5539 Open-Loop Phase vs Frequency



Gain Bandwidth Product vs Frequency

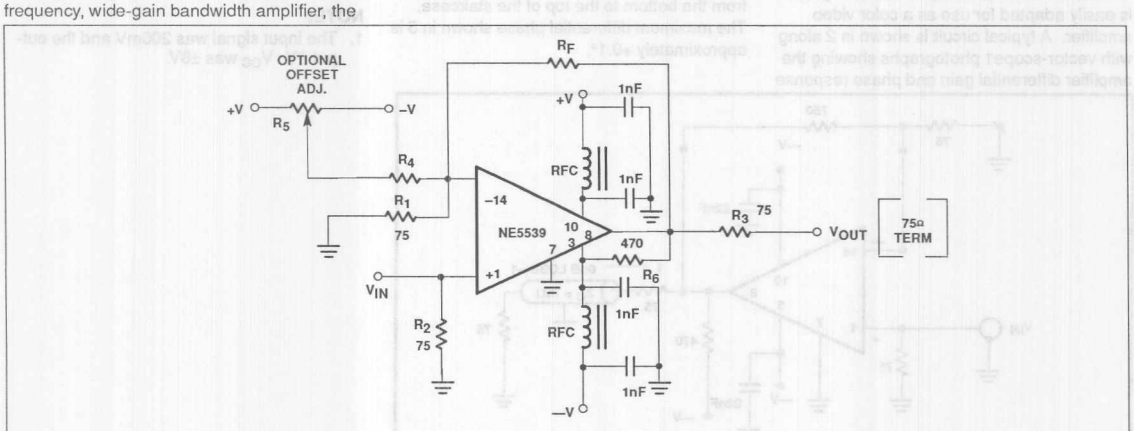


NOTE:

Indicates typical distribution $-55°C \leq T_A \leq 125°C$

CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide-gain bandwidth amplifier, the physical circuit is extremely critical. Bread-boarding is not recommended. A double-sided copper-clad printed circuit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in 1.



R_1 = 75Ω 5% CARBON
R_2 = 75Ω 5% CARBON
R_3 = 75Ω 5% CARBON
R_4 = 36K 5% CARBON

R_5 = 20k TRIMPOT (CERMET)
R_F = 1.5k (28dB GAIN)
R_6 = 470Ω 5% CARBON

RFC 3T # 26 BUSS WIRE ON FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)

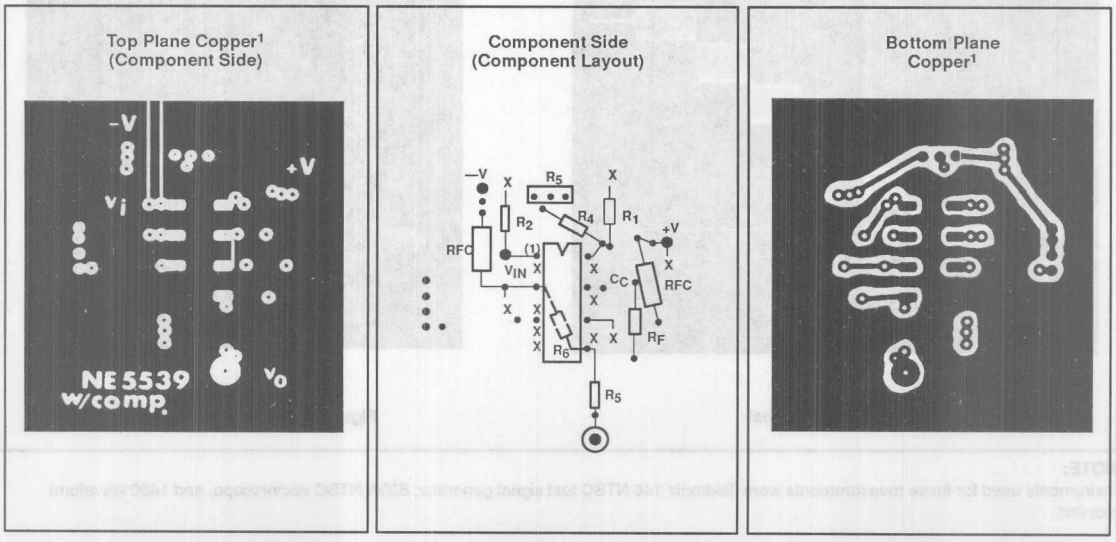


Figure 1. 28dB Non-Inverting Amp Sample PC Layout

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in 2 along with vector-scope1 photographs showing the amplifier differential gain and phase response to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75W input and output termionation impedance with a gain of approximately 10 (20dB).

NOTE:

1. The input signal was 200mV and the output 2V. V_{CC} was ±8V.

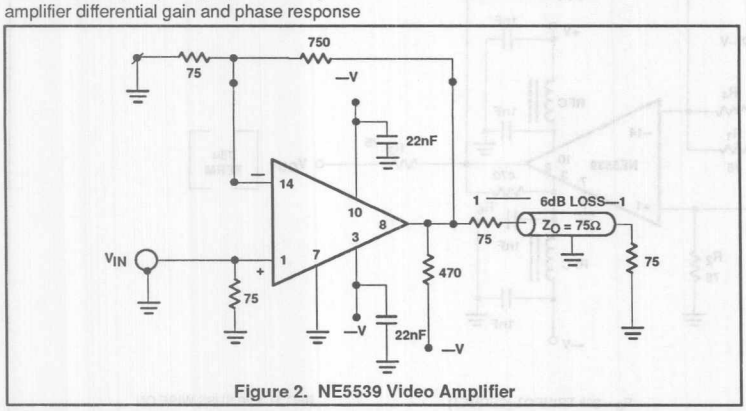


Figure 2. NE5539 Video Amplifier

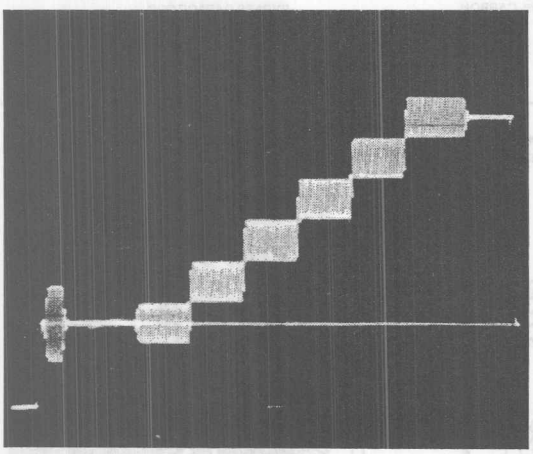


Figure 3. Input Signal

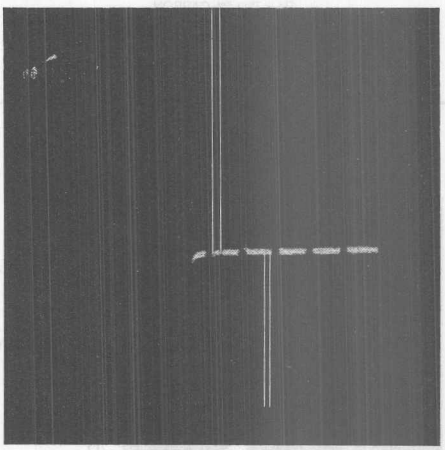


Figure 4. Differential Gain <0.5%

NOTE:

Instruments used for these measurements were Tektronix 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

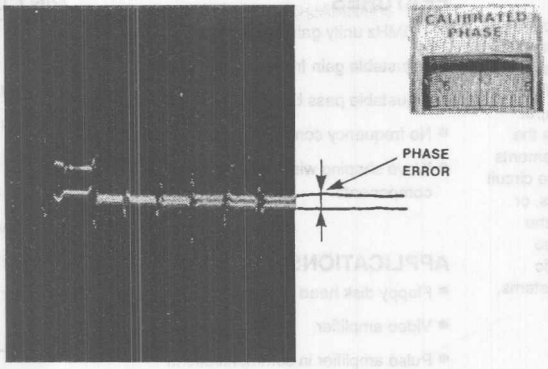


Figure 5. Differential Gain +0.1°

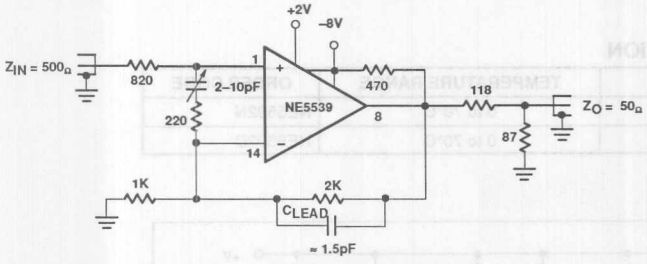


Figure 6. Non-Inverting Follower

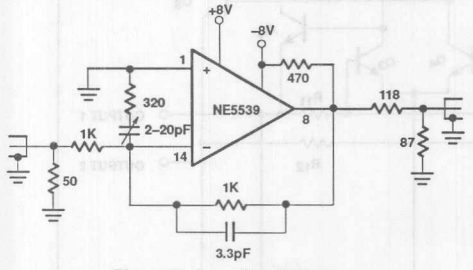


Figure 7. Inverting Follower

Video amplifier — NE5592

DESCRIPTION

The NE5592 is a dual monolithic, two-stage, differential output, wideband video amplifier. It offers a fixed gain of 400 without external components and an adjustable gain from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

FEATURES

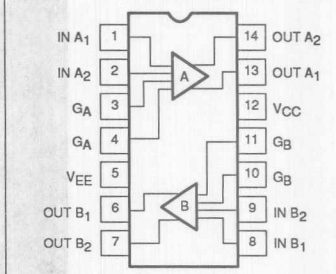
- 110MHz unity gain bandwidth
- Adjustable gain from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external components

APPLICATIONS

- Floppy disk head amplifier
- Video amplifier
- Pulse amplifier in communications
- Magnetic memory
- Video recorder systems

PIN CONFIGURATION

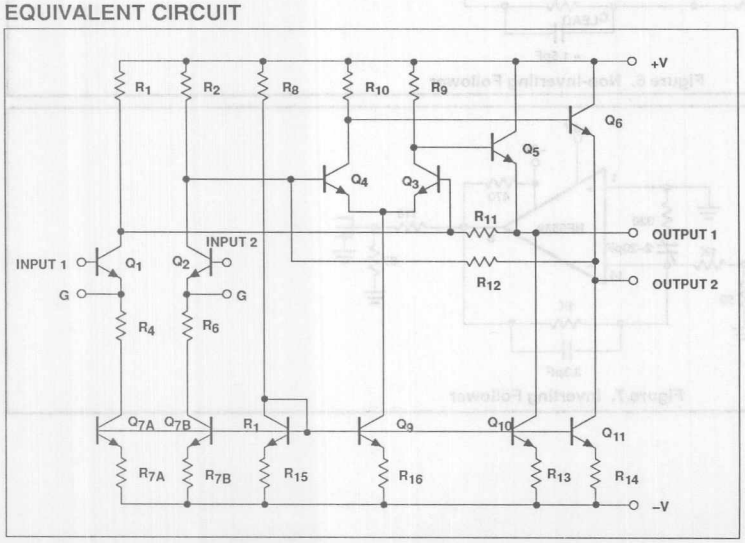
D, N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to 70°C	NE5592N
14-Pin SO package	0 to 70°C	NE5592D

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common mode Input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating temperature range NE5592	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, T_A=25°C (still air)[1]		
	D package	1.03	W
	N package	1.48	W

NOTES:

1. Derate above 25°C at the following rates:
   D package 8.3mW/°C
   N package 11.9mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=+25°C, V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltage is V_S = ±6.0V, and gain select pins are connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	R_L=2kΩ, V_{OUT}=3V_{P-P}	400	480	600	V/V
R_{IN}	Input resistance		3	14		kΩ
C_{IN}	Input capacitance			2.5		pF
I_{OS}	Input offset current			0.3	3	µA
I_{BIAS}	Input bias current			5	20	µA
	Input noise voltage	BW 1kHz to 10MHz		4		nV/√Hz
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	V_{CM} ± 1V, f<100kHz V_{CM} ± 1V, f=5MHz	60	93 87		dB dB
PSRR	Supply voltage rejection ratio	ΔV_S= ± 0.5V	50	85		dB
	Channel separation	V_{OUT}=1V_{P-P}; f=100kHz (output referenced) R_L=1kΩ	65	70		dB
V_{OS}	Output offset voltage gain select pins open	R_L=∞ R_L=∞		0.5 0.25	1.5 0.75	V V
V_{CM}	Output common-mode voltage	R_L=∞	2.4	3.1	3.4	V
V_{OUT}	Output differential voltage swing	R_L=2kΩ	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current (total for both sides)	R_L=∞		35	44	mA

DC ELECTRICAL CHARACTERISTICS

V_{SS}=±6V, V_{CM}=0, 0°C ≤ T_A ≤ 70°C, unless otherwise specified. Recommended operating supply voltage is V_S = ±6.0V, and gain select pins are connected together.

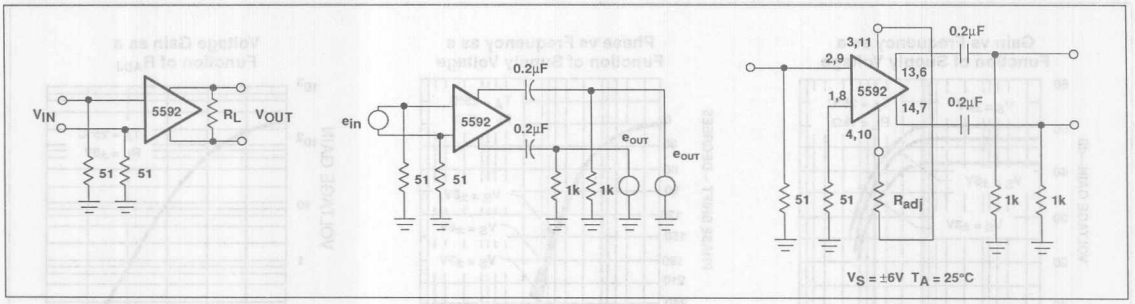
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
A_{VOL}	Differential voltage gain	R_L=2kΩ, V_{OUT}=3V_{P-P}	350	430	600	V/V
R_{IN}	Input resistance		1	11		kΩ
I_{OS}	Input offset current				5	µA
I_{BIAS}	Input bias current				30	µA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio	V_{CM} ± 1V, f<100kHz R_S=ϕ	55			dB
PSRR	Supply voltage rejection ratio	ΔV_S= ± 0.5V	50			dB
	Channel separation	V_{OUT}=1V_{P-P}; f=100kHz (output referenced) R_L=1kΩ		70		dB
V_{OS}	Output offset voltage					
	gain select pins connected together	R_L=∞			1.5	V
	gain select pins open	R_L=∞			1.0	V
V_{OUT}	Output differential voltage swing	R_L=2kΩ	2.8			V
I_{CC}	Power supply current					
	(total for both sides)	R_L=∞			47	mA

AC ELECTRICAL CHARACTERISTICS

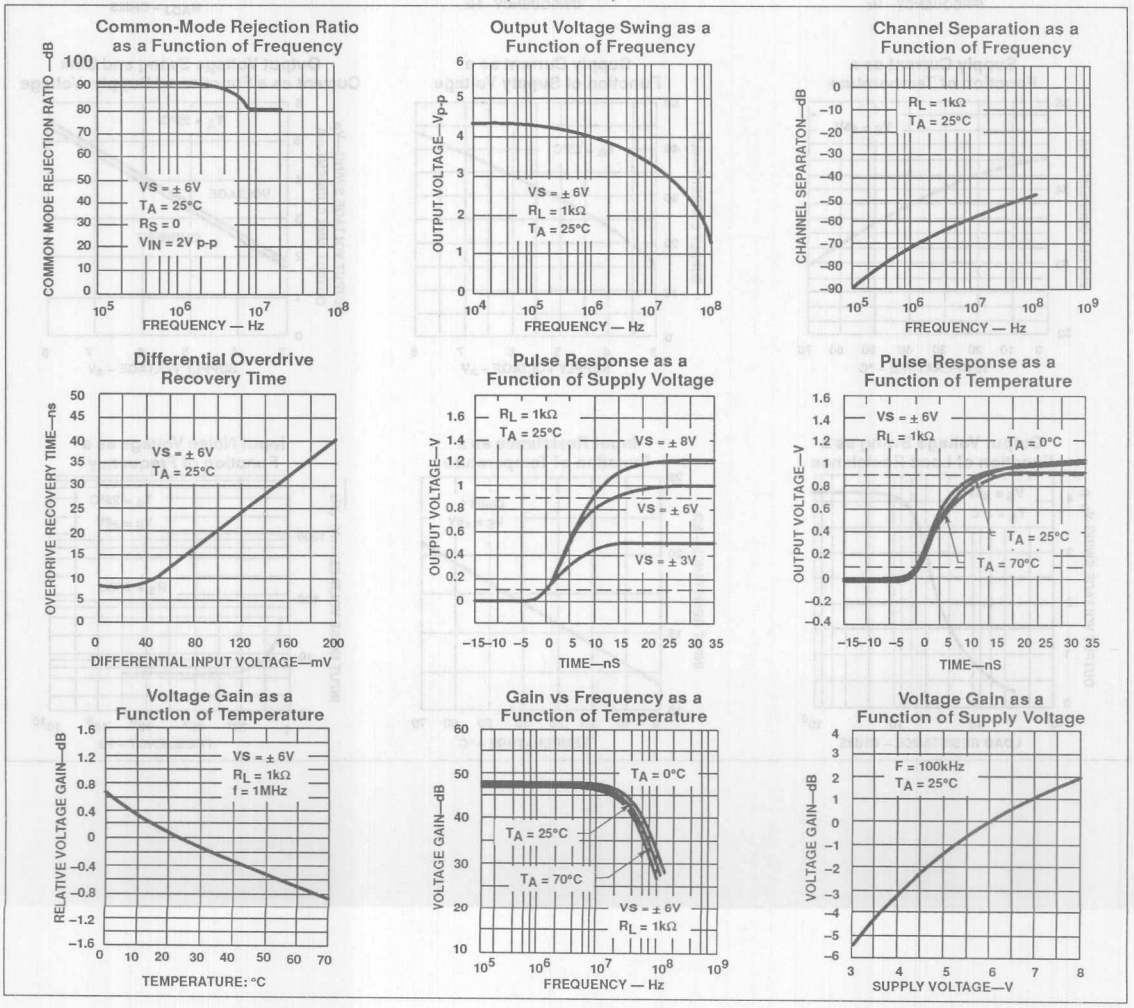
T_A=+25°C V_{SS}=±6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltage V_S=±6.0V. Gain select pins connected together.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
BW	Bandwidth	V_{OUT}=1V_{P-P}		25		MHz
t_R	Rise time			15	20	ns
t_{PD}	Propagation delay	V_{OUT}=1V_{P-P}		7.5	12	ns

TEST CIRCUITS T_A=25°C unless otherwise specified.

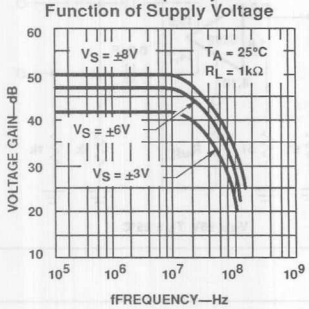


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

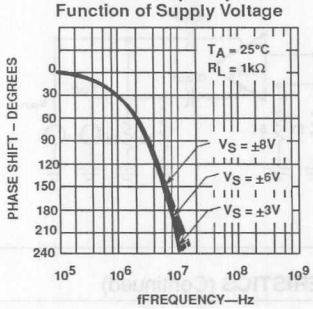


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

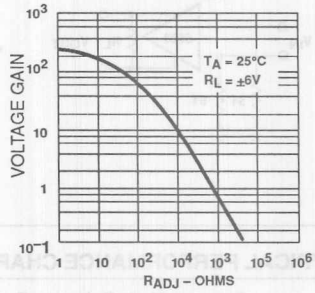
Gain vs Frequency as a Function of Supply Voltage



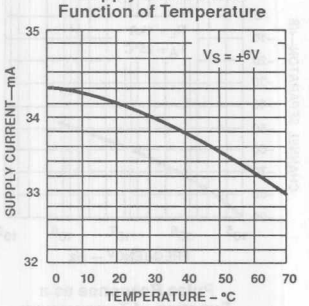
Phase vs Frequency as a Function of Supply Voltage



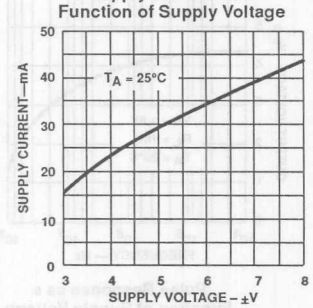
Voltage Gain as a Function of R_{ADJ}



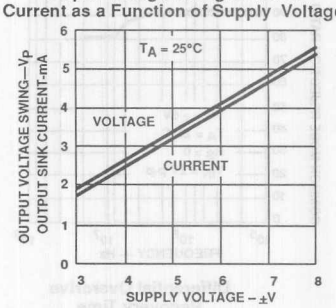
Supply Current as a Function of Temperature



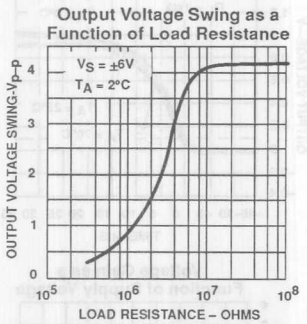
Supply Current as a Function of Supply Voltage



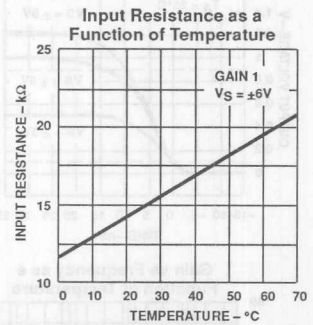
Output Voltage Swing and Sink Current as a Function of Supply Voltage



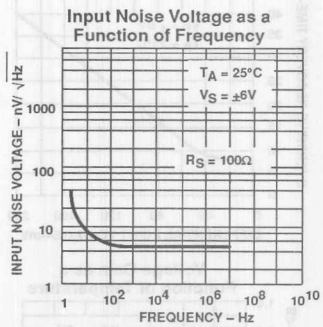
Output Voltage Swing as a Function of Load Resistance



Input Resistance as a Function of Temperature



Input Noise Voltage as a Function of Frequency



Video amplifier

NE592

DESCRIPTION

The NE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

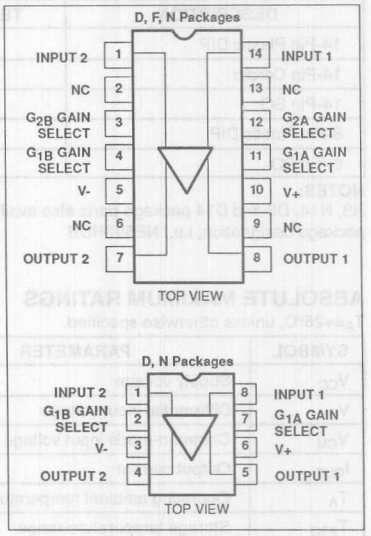
FEATURES

- 120MHz unity gain bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external components
- MIL-STD processing available

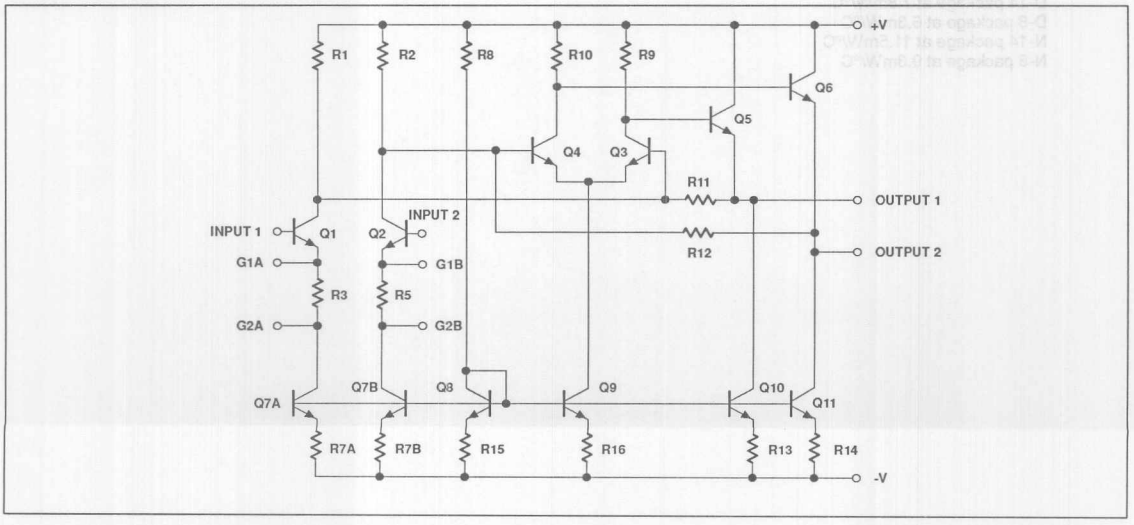
APPLICATIONS

- Floppy disk head amplifier
- Video amplifier
- Pulse amplifier in communications
- Magnetic memory
- Video recorder systems

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE592N14
14-Pin Cerdip	0 to +70°C	NE592F14
14-Pin SO	0 to +70°C	NE592D14
8-Pin Plastic DIP	0 to +70°C	NE592N8
8-Pin SO	0 to +70°C	NE592D8

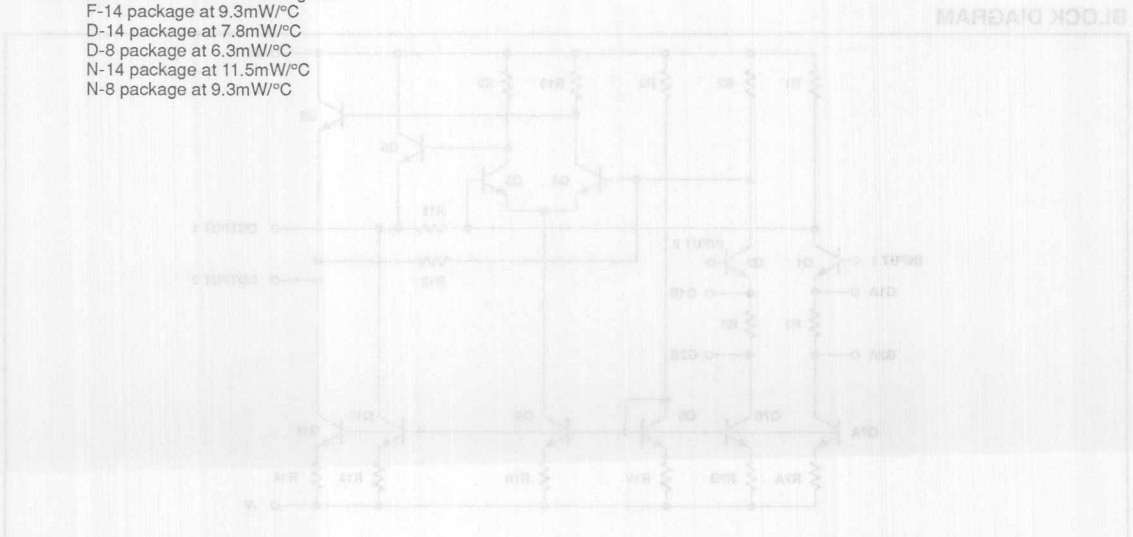
NOTES:
N8, N14, D8 and D14 package parts also available in "High" gain version by adding "H" before package designation, i.e., NE592HDB

ABSOLUTE MAXIMUM RATINGS

T_A=+25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, T_A=25°C (still air)[1]		
	F-14 package	1.17	W
	D-14 package	0.98	W
	D-8 package	0.79	W
	N-14 package	1.44	W
	N-8 package	1.17	W

NOTES:
2. Derate above 25°C at the following rates:
F-14 package at 9.3mW/°C
D-14 package at 7.8mW/°C
D-8 package at 6.3mW/°C
N-14 package at 11.5mW/°C
N-8 package at 9.3mW/°C



DC ELECTRICAL CHARACTERISTICS

T_A=+25°C V_{SS}=+6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltages V_S=+6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			UNIT
			Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part					
	Gain 1[1]	R_L=2kΩ, V_{OUT}=3V_{P-P}	250	400	600	V/V
	Gain 2[2,4]		80	100	120	V/V
	High gain part		400	500	600	V/V
R_{IN}	Input resistance					
	Gain 1[1]			4.0		kΩ
	Gain 2[2,4]		10	30		kΩ
C_{IN}	Input capacitance[2]	Gain 2[4]		2.0		pF
I_{OS}	Input offset current			0.4	5.0	μA
I_{BIAS}	Input bias current			9.0	30	μA
V_{NOISE}	Input noise voltage	BW 1kHz to 10MHz		12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio					
	Gain 2[4]	V_{CM}±1V, f<100kHz	60	86		dB
	Gain 2[4]	V_{CM}±1V, f=5MHz		60		dB
PSRR	Supply voltage rejection ratio					
	Gain 2[4]	ΔV_S=±0.5V	50	70		dB
V_{OS}	Output offset voltage					
	Gain 1	R_L=∞			1.5	V
	Gain 2[4]	R_L=∞			1.5	V
	Gain 3[3]	R_L=∞		0.35	0.75	V
V_{CM}	Output common-mode voltage	R_L=∞	2.4	2.9	3.4	V
V_{OUT}	Output voltage swing differential	R_L=2kΩ	3.0	4.0		V
R_{OUT}	Output resistance			20		Ω
I_{CC}	Power supply current	R_L=∞		18	24	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin version only.

DC ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics V_{SS}=±6V, V_{CM}=0, 0°C ≤T_A≤70°C, unless otherwise specified. Recommended operating supply voltages V_S=+6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			UNIT
			Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part					
	Gain 1[1]	R_L=2kΩ, V_{OUT}=3V_{P-P}	250		600	V/V
	Gain 2[2, 4]		80		120	V/V
	High gain part		400	500	600	V/V
R_{IN}	Input resistance					
	Gain 2[2, 4]		8.0			kΩ
I_{OS}	Input offset current				6.0	µA
I_{BIAS}	Input bias current				40	µA
V_{IN}	Input voltage range		±1.0			V
CMRR	Common-mode rejection ratio					
	Gain 2[4]	V_{CM}±1V, f<100kHz	50			dB
PSRR	Supply voltage rejection ratio					
	Gain 2[4]	ΔV_S=±0.5V	50			dB
V_{OS}	Output offset voltage					
	Gain 1	R_L=∞			1.5	V
	Gain 2[4]				1.5	
	Gain 3[3]				1.0	
V_{OUT}	Output voltage swing differential	R_L=2kΩ	2.8			V
I_{CC}	Power supply current	R_L=∞			27	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

AC ELECTRICAL CHARACTERISTICS

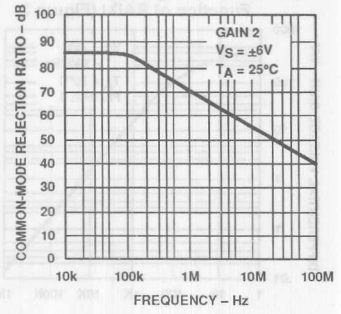
T_A=+25°C V_{SS}=+6V, V_{CM}=0, unless otherwise specified. Recommended operating supply voltages V_S=±6.0V. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			UNIT
			Min	Typ	Max	
BW	Bandwidth					
	Gain 1[1]			40		MHz
	Gain 2[2, 4]			90		MHz
t_R	Rise time					
	Gain 1[1]	V_{OUT}=1V_{P-P}		10.5	12	ns
	Gain 2[2, 4]			4.5		ns
t_{PD}	Propagation delay					
	Gain 1[1]	V_{OUT}=1V_{P-P}		7.5	10	ns
	Gain 2[2, 4]			6.0		ns

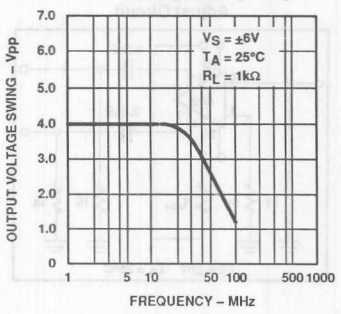
NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

TYPICAL PERFORMANCE CHARACTERISTICS

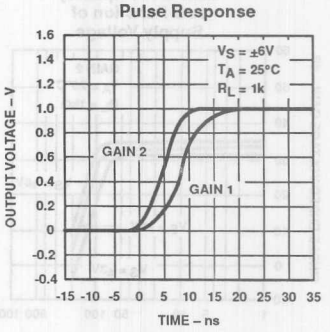
Common-Mode Rejection Ratio as a Function of Frequency



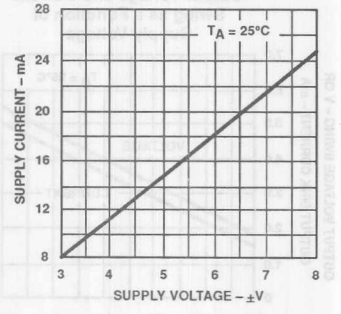
Output Voltage Swing as a Function of Frequency



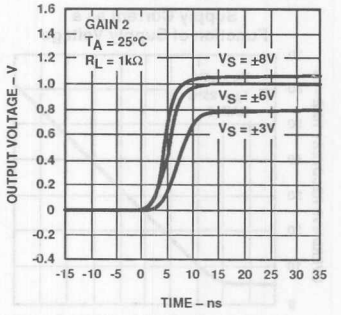
Pulse Response



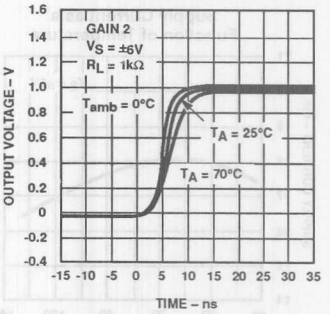
Differential Overdrive Recovery Time



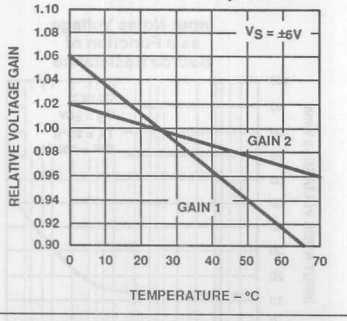
Pulse Response as a Function of Supply Voltage



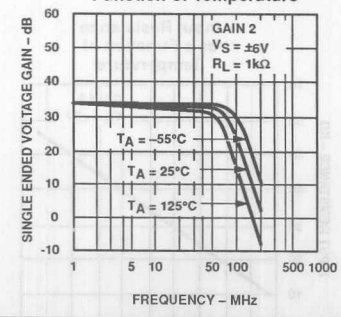
Pulse Response as a Function of Temperature



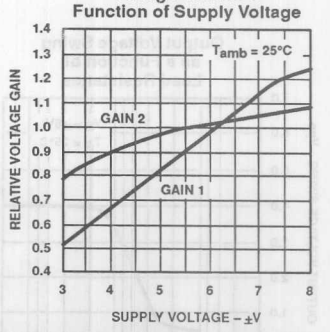
Voltage Gain as a Function of Temperature



Gain vs. Frequency as a Function of Temperature

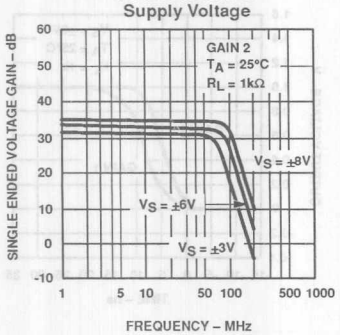


Voltage Gain as a Function of Supply Voltage

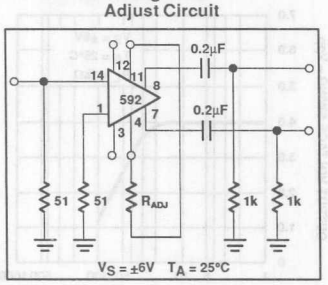


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

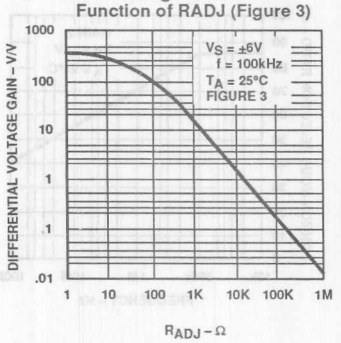
Gain vs. Frequency as a Function of Supply Voltage



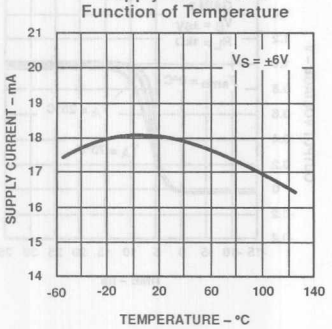
Voltage Gain Adjust Circuit



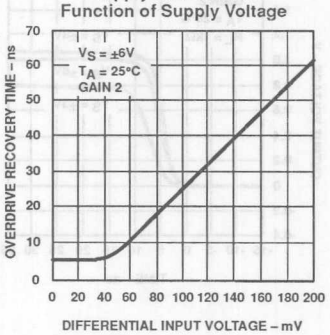
Voltage Gain as a Function of RADJ (Figure 3)



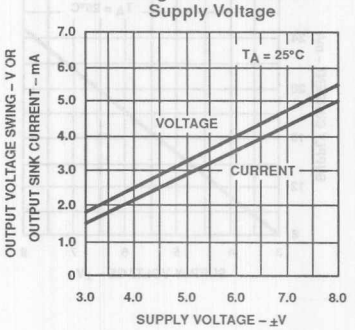
Supply Current as a Function of Temperature



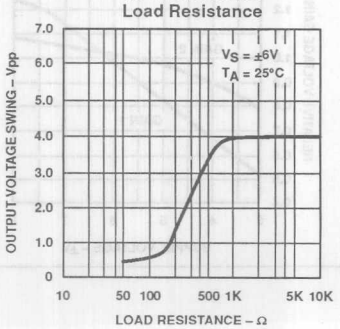
Supply Current as a Function of Supply Voltage



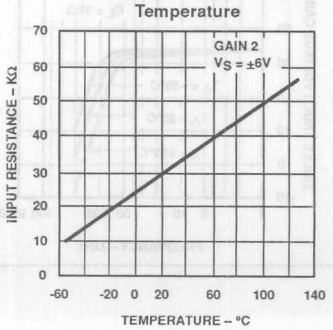
Output Voltage and Current Swing as a Function of Supply Voltage



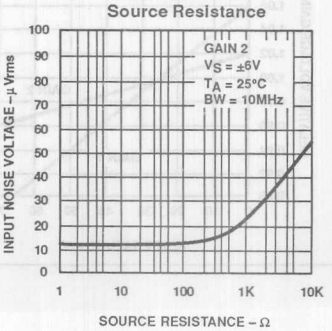
Output Voltage Swing as a Function of Load Resistance



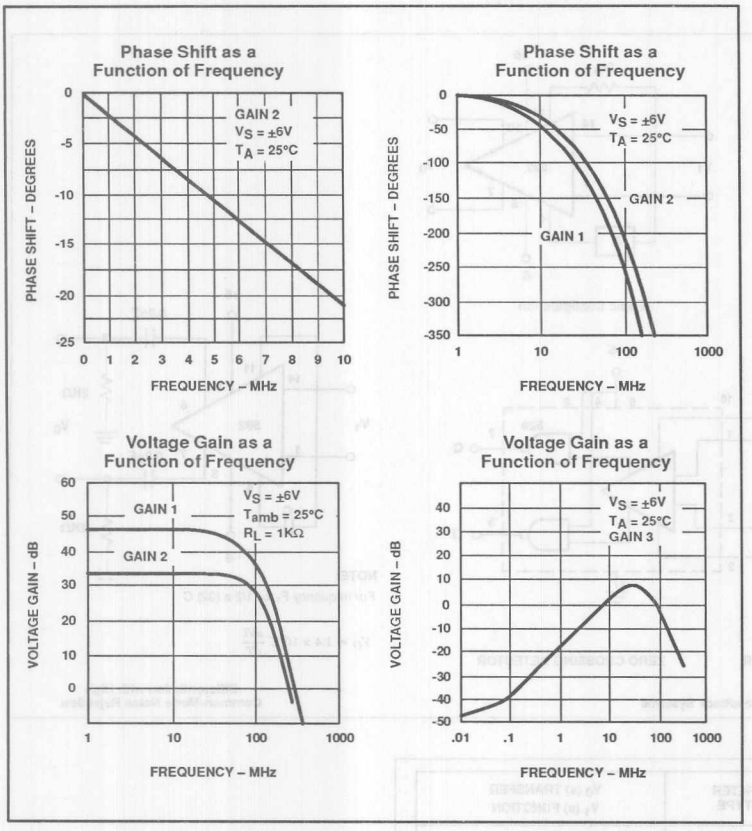
Input Resistance as a Function of Temperature



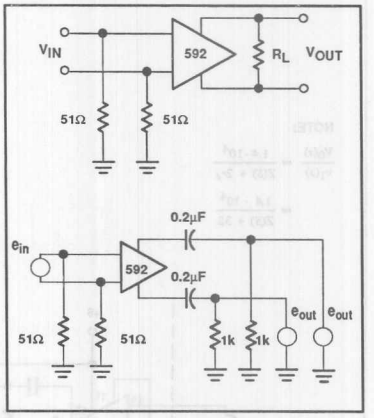
Input Noise Voltage as a Function of Source Resistance



Video amplifier NE592



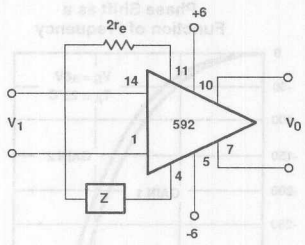
TEST CIRCUITS $T_A = 25°C$, unless otherwise specified.



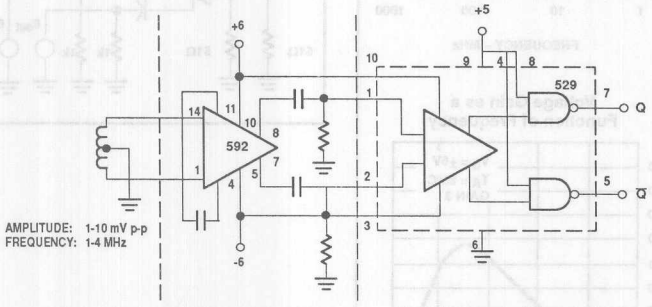
TYPICAL APPLICATIONS

NOTE:

$$\frac{V_0(s)}{v_1(s)} \approx \frac{1.4 \cdot 10^4}{Z(S) + 2r_e} \approx \frac{1.4 \cdot 10^4}{Z(S) + 32}$$

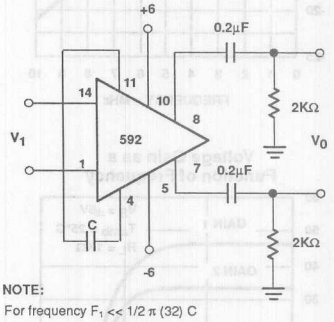


Basic Configuration



READ HEAD | DIFFERENTIATOR/AMPLIFIER | ZERO CROSSING DETECTOR

Disc/Tape Phase-Modulated Readback Systems

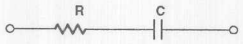
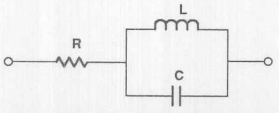


NOTE:
For frequency $F_1 << 1/2\pi$ (32) C

$$V_O \approx 1.4 \times 10^4 C \frac{dVi}{dT}$$

Differentiation with High Common-Mode Noise Rejection

FILTER NETWORKS

Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L} \left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R} \left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L} \left[\frac{s}{s^2 + R/Ls + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R} \left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTES:
In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.
$S = j\omega$
$\omega = 2\pi f$

Differential video amplifier — μA733/733C

DESCRIPTION

The 733 is a monolithic differential input, differential output, wide-band video amplifier. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth, and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter-follower outputs to the inputs of the second stage. The emitter-follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high-performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

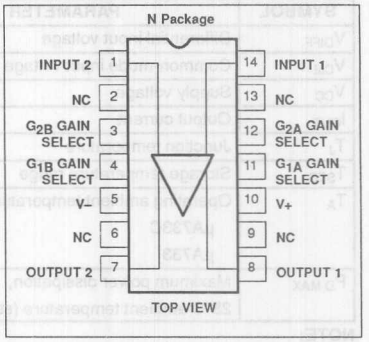
FEATURES

- 120MHz bandwidth
- 250kΩ input resistance
- Selectable gains of 10, 100, and 400
- No frequency compensation required
- MIL-STD-883A, B, C available

APPLICATIONS

- Video amplifier
- Pulse amplifier in communications
- Magnetic memories
- Video recorder systems

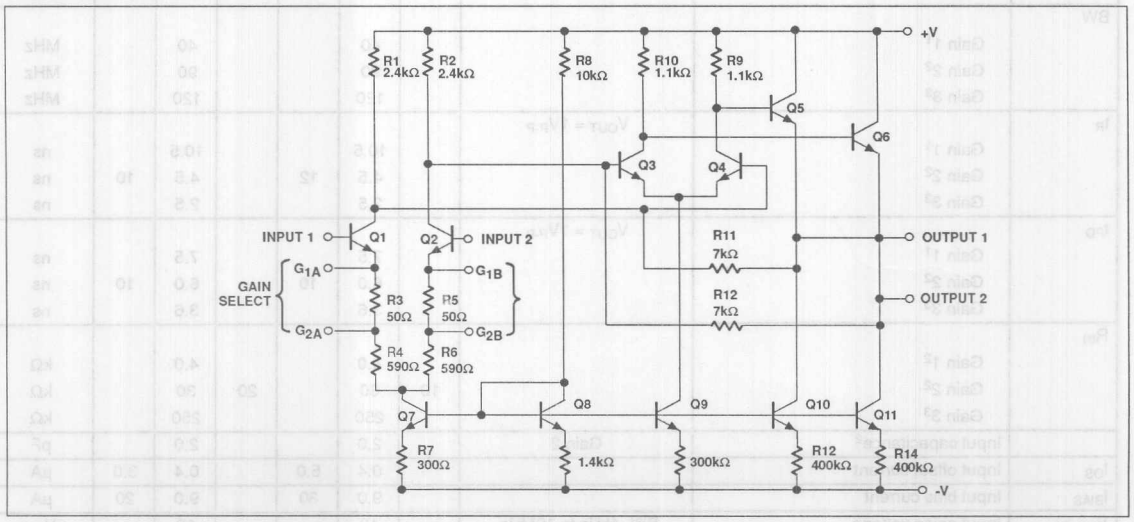
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE
14-Pin Plastic DIP	-55°C to +125°C	μA733N
14-Pin Plastic DIP	0 to +70°C	μA733CN

CIRCUIT SCHEMATIC



Differential video amplifier μA733/733C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DIFF}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
V_{CC}	Supply voltage	±8	V
I_{OUT}	Output current	10	mA
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range		
	μA733C	0 to +70	°C
	μA733	-55 to +125	°C
$P_{D\,MAX}$	Maximum power dissipation, 25°C ambient temperature (still-air)[1]	1420	mW

NOTE:
1. The following derating factors should be applied 25°C:
   N package at 11.4mW/°C

DC ELECTRICAL CHARACTERISTICS

T_A=+25°C, V_S=±6V, V_{CM}=0, unless otherwisespecified. Recommended operating supply voltages V_S=±6.0V.

SYMBOL	PARAMETER	TEST CONDITIONS	μA733C			μA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Differential voltage gain	R_l = 2kΩ, V_{OUT} = 3V_{P-P}							
	Gain 1[2]		250	400	600	300	400	500	V/V
	Gain 2[2]		80	100	120	90	100	110	V/V
	Gain 3[3]		8	10	12	9	10	11	V/V
BW									
	Gain 1[1]			40			40		MHz
	Gain 2[2]			90			90		MHz
	Gain 3[3]			120			120		MHz
t_R		V_{OUT} = 1V_{P-P}							
	Gain 1[1]			10.5			10.5		ns
	Gain 2[2]			4.5	12		4.5	10	ns
	Gain 3[3]			2.5			2.5		ns
t_{PD}		V_{OUT} = 1V_{P-P}							
	Gain 1[1]			7.5			7.5		ns
	Gain 2[2]			6.0	10		6.0	10	ns
	Gain 3[3]			3.6			3.6		ns
R_{IN}									
	Gain 1[2]			4.0			4.0		kΩ
	Gain 2[2]		10	30		20	30		kΩ
	Gain 3[3]			250			250		kΩ
	Input capacitance[2]	Gain 2		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW=1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR									
	Gain 2	V_{CM}=±1V, f≤100kHz	60	86		60	86		dB
	Gain 2	V_{CM}=±1V, f=5MHz		60			60		dB

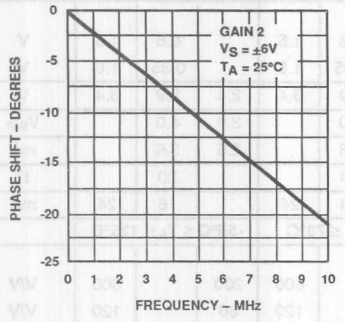
DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	μA733C			μA733			UNIT
			Min	Typ	Max	Min	Typ	Max	
SVRR	Supply voltage rejection ratio Gain 2	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
	Output offset voltage	$R_L = \infty$							
	Gain 1[1]			0.6	1.5		0.6	1.5	V
	Gain 2 and 3[2, 3]			0.35	1.5		0.35	1.0	V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
	Output voltage swing, differential	R_L=2kΩ	3.0	4.0		3.0	4.0		V_{P-P}
I_{SINK}	Output sink current		2.5	3.6		2.5	3.6		mA
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA
THE FOLLOWING SPECIFICATIONS APPLY OVER TEMPERATURE			0°C ≤ T_A ≤ 70°C			-55°C ≤ T_A ≤ 125°C			
	Differential voltage gain	R_l = 2kΩ, V_{OUT} = $3V_{P-P}$							
	Gain 1[1]		250		600	200		600	V/V
	Gain 2[2]		80		120	80		120	V/V
	Gain[3]		8		12	8		12	V/V
R_{IN}	Input resistance								
	Gain 2[2]		8			8			kΩ
I_{OS}	Input offset current				6			5	μA
I_{BIAS}	Input bias current				40			40	μA
V_{IN}	Input voltage range		±1.0			±1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2	V_{CM}=±V, F≤100kHz	50			50			dB
SVRR	Supply voltage rejection ratio								
	Gain 2	ΔV_S=±0.5V	50			50			dB
V_{OS}	Output offset voltage	$R_L = \infty$							
	Gain 1[1]				1.5			1.5	V
	Gain 2 and 3[2, 3]				1.5			1.2	V
V_{DIFF}	Output voltage swing, differential	R_L = 2kΩ	2.8			2.5			V_{P-P}
I_{SINK}	Output sink current		2.5			2.2			mA
I_{CC}	Power supply current	$R_L \pm \infty$			27			27	mA

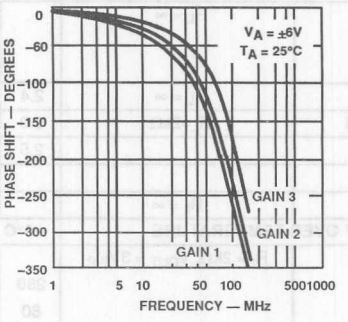
NOTES:
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

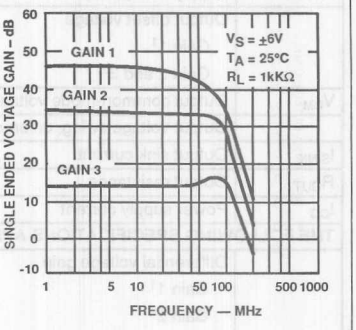
Phase Shift as a Function of Frequency



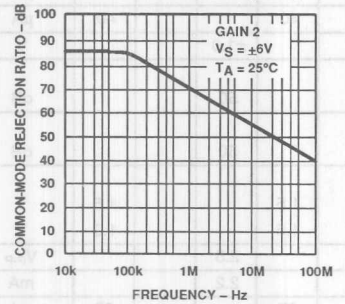
Phase Shift as a Function of Frequency



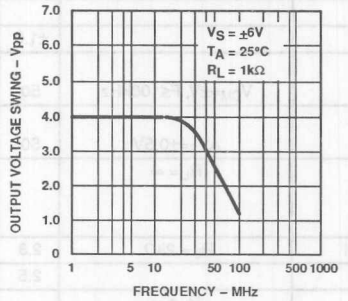
Voltage Gain as a Function of Temperature



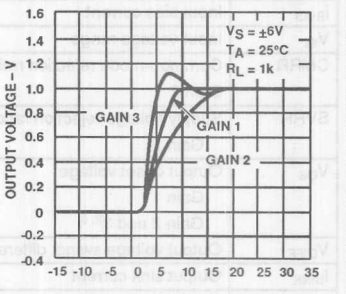
Common-Mode Rejection Ratio as a Function of Frequency



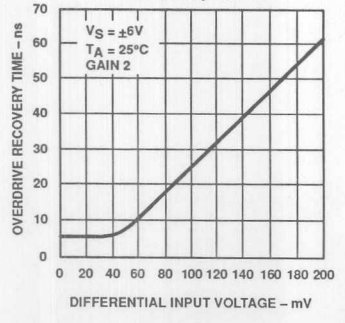
Output Voltage Swing as a Function of Frequency



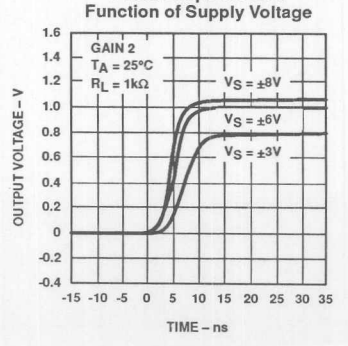
Pulse Response



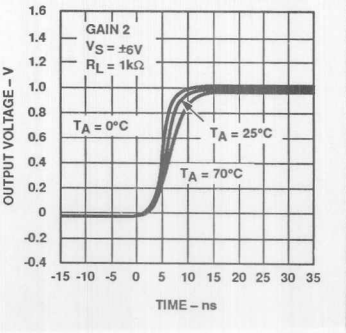
Differential Overdrive Recovery Time



Pulse Response as a Function of Supply Voltage

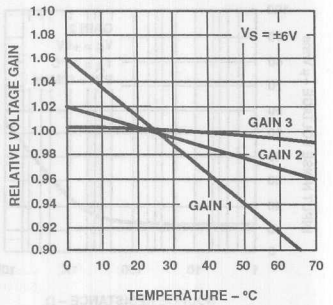


Pulse Response as a Function of Temperature

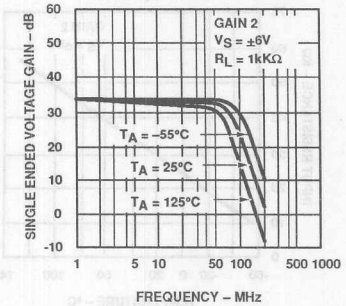


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

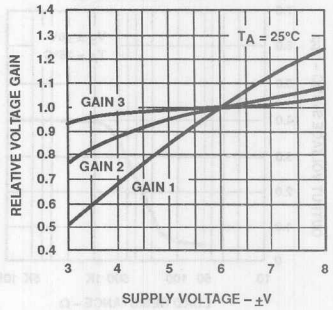
Voltage Gain as a Function of Temperature



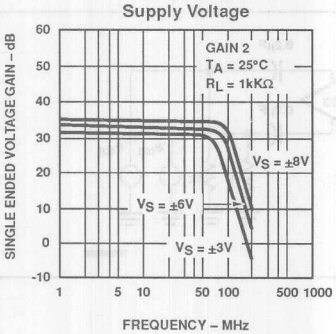
Gain vs. Frequency as a Function of Temperature



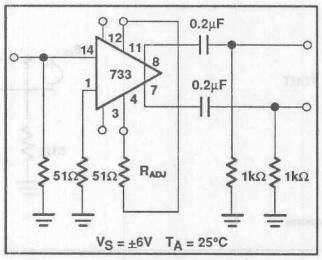
Voltage Gain as a Function of Supply Voltage



Gain vs. Frequency as a Function of Supply Voltage

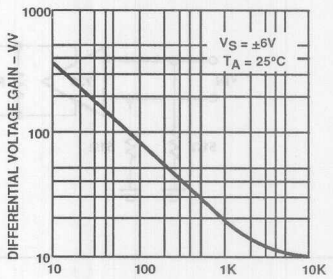


Voltage Gain Adjust Circuit

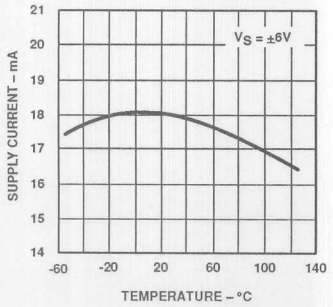


(Pin numbers apply to K Package)

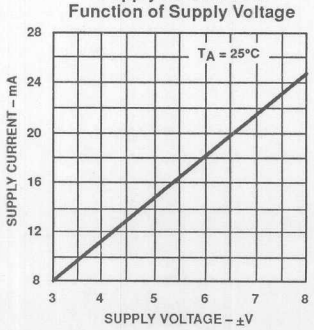
Voltage Gain as a Function of RADJ (Figure 3)



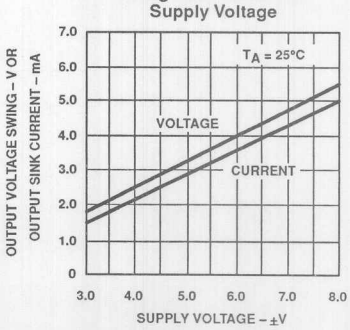
Supply Current as a Function of Temperature



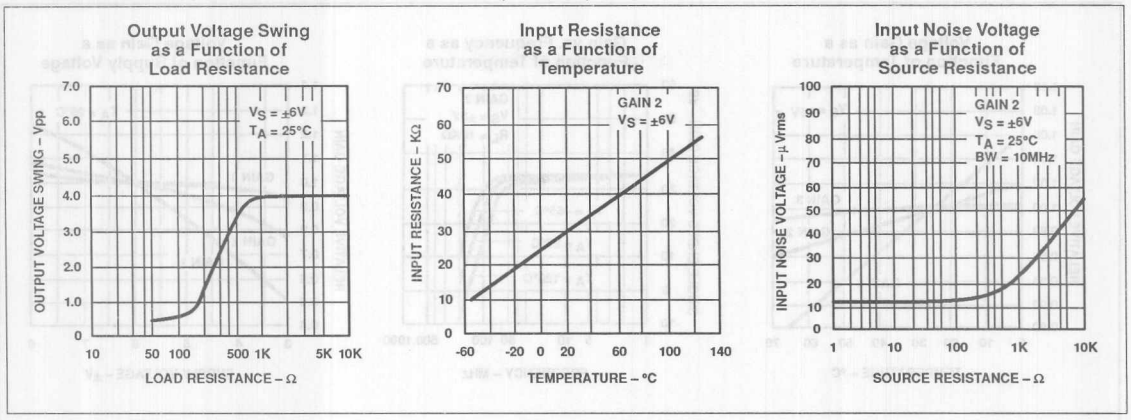
Supply Current as a Function of Supply Voltage



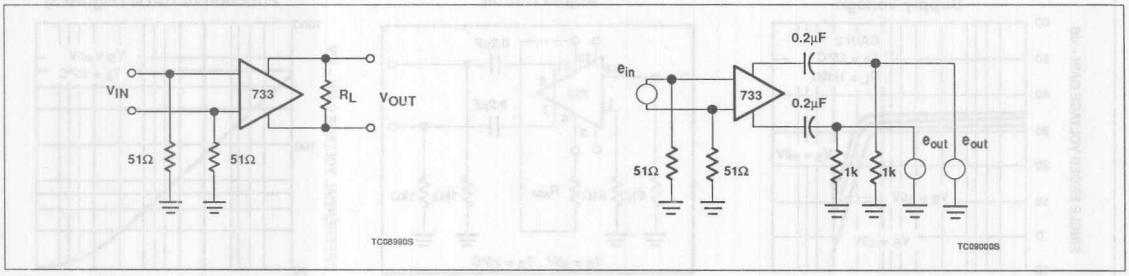
Output Voltage and Current Swing as a Function of Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TEST CIRCUITS T_A=25°C, unless otherwise specified.



Section 3
Comparators

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General Purpose/Linear ICs

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LM212 Dual voltage comparator 180
LM139/139A/239/239A/339/339A/2901/2903 Low power dual voltage comparator 197
AU2903 Low power dual voltage comparator 209
NE/SE524 High-speed dual-differential comparator/sense amp 204
NE522 High-speed dual-differential comparator/sense amp 213
NE527 Voltage comparator 218
NE529 Voltage comparator 229

DEVICE	COM-PLEXITY	TEMP RANGE*	MAX INP OFFSET VOLT (mV)	MAX INPUT CURRENT		SUPPLY VOLTAGE (V)	RESPONSE TIME (TYP) (ns)	COMMON MODE VOLTAGE RANGE (V)	OUTPUT VOLTAGE		OUTPUT STRUCTURE	VOLTAGE GAIN (TYP) (V/mV)	TTL FANOUT	MAX OFF INPUT VOLTAGE (V)
				BIAS (μ A)	OFFSET (μ A)				V OL MAX (V)	V OH MIN (V)				
LM111	SINGLE	M	3.0	0.10	0.01	± 15	200	−14.5/+13	0.4		OC	200	5	± 30
LM211	SINGLE	I	3.0	0.10	0.01	to	200	−14.5/+13	0.4		OC	200	5	± 30
LM311	SINGLE	C	7.5	0.25	0.05	+5 and GND	200	−14.5/+13	0.4		OC	200	5	± 30
NE527	SINGLE	C	10.0	4.00	1.0	± 10	16	± 5	0.5	2.7	TTL		5	± 5
SE527	SINGLE	M	6.00	4.00	1.00	+5	16	± 5	0.5	2.5	TTL		5	± 5
NE529	SINGLE	C	10.0	50.0	15.0	±10	12	± 5	0.5	2.7	TTL		5	± 5
SE529	SINGLE	M	6.00	36.0	9.00	and +5	12	± 5	0.5	2.5	TTL		5	± 5
AU2903	DUAL	AX	7.0	0.25	0.05	+2 to +36 GND	1300	0 to Vs−2	0.7		OC	100	2	36
LM119	DUAL	M	7.00	1.00	0.10	± 15	80	± 13	0.4		OC	40	2	± 5
LM219	DUAL	I	7.00	1.00	0.10	to	80	± 13	0.4		OC	40	2	± 5
LM319	DUAL	C	10.0	1.20	0.30	+5 and GND	80	± 13	0.4		OC	40	2	± 5
LM193 /193A	DUAL	M	9.00/4.0	0.30	0.10	± 1 to ± 18	1300	0 to Vs−2	0.7		OC	200	2	36
LM293/293A	DUAL	I	9.00/4.0	0.40	0.15	or	1300	0 to Vs−2	0.7		OC	200	2	36
LM393/393A	DUAL	C	9.00/4.0	0.40	0.15	+2 to +36 GND	1300	0 to Vs−2	0.7		OC	200	2	36
LM2903	DUAL	I	15.0	0.50	0.20		1300	0 to Vs−2	0.7		OC	100	2	36
NE/SE521	DUAL	M/C	15/10.0	40.0	12.0	+5 −5 GND	8	± 3	0.5	2.5/2.7	TTL		12	± 6
NE/SE522	DUAL	M/C	15/10.0	40.0	12.0	+5 −5 GND	10	± 3	0.5		OC		12	± 6
AU2901	QUAD	AX	7.0	0.25	0.05	+2 to +36 GND	1300	0 to Vs−2	0.7		OC	100	2	36
LM139 /139A	QUAD	M	9.00/4.0	0.30	0.10		1300	0 to Vs−2	0.7		OC	200	2	36
LM239/239A	QUAD	I	9.00/4.0	0.40	0.15	±1 to± 18 or	1300	0 to Vs−2	0.7		OC	200	2	36
LM339/339A	QUAD	C	9.00/4.0	0.40	0.15	+2 to +36	1300	0 to Vs−2	0.7		OC	200	2	36
LM2901	QUAD	I	15.0	0.50	0.20		1300	0 to Vs−2	0.7		OC	100	2	36
MC3302	QUAD	I	40.0	1.00	0.30	+2 to +28 GND	1300	0 to Vs−2	0.7		OC	100	2	36

* Temperature range
I = Industrial −25°C to +85°C
C = Commercial 0°C to +70°C
M = Military −55°C to +125°C
A = Automotive −40°C to +85°C
AX = Automotive extended −40°C to +125°C

Symbols and definitions for comparators

Common-Mode Rejection Ratio (CMRR)
The ratio of the change in input common-mode voltage (over a specified input common-mode range) to the corresponding change in V_{OS} (see definition below). CMRR is expressed in dB where CMRR (dB) = $20\log(\Delta CMV/\Delta V_{OS})$.

Differential Input Resistance (R_{IN})
The small-signal resistance looking into either input terminal with the other input terminal connected to a specified voltage.

Input Bias Current (I_{BIAS})
The current into either input terminal with both inputs connected to a common specified voltage.

Input Common-Mode Voltage Range (CMVR)
The range of input common-mode voltage for which operation within the specifications is guaranteed.

Input Offset Current (I_{OS})
The difference between the two input bias currents with both inputs connected to a common specified voltage.

Input Offset Current Drift (TCI_{OS})
The ratio of the change in I_{OS} to the corresponding change in temperature as that temperature deviates from 25°C.

Input Offset Voltage (V_{OS})
The minimum potential difference required between the input terminals to force the output to a specified voltage.

Input Offset Voltage Drift (TCV_{OS})
The ratio of the change in V_{OS} to the corresponding change in temperature as that temperature deviates from 25°C.

Input to Output Propagation Delay (t_{PD})
The propagation delay measured from the time the differential input signal equals V_{OS} to the 50% point of the output transition with the comparator in the compare mode. The propagation delay is specified for a given initial input voltage ($-V_{IN}$) and overdrive (V_{OD}, see definition below) and can also be specified for both positive - (t_{PD+}) and negative -(t_{PD-}) going output transitions and is cpecified for a particular value of V_{OD} (see definition below).

Latch Disable Propagation Delay (t_{LPD})
The propagation delay measured between the 50% point of the latch-to-compare transition of the latch enable signal and the 50% point of the output transition. This propagation delay can be specified for both positive - (t_{lPD+}) and negative - (t_{lPD-}) going output transitions and is specified for a particular value of V_{OD} (see definition below).

Latch Hold Time (t_H)
The minimum time after the compare-to-latch transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the output. Hold time is measured from the 50% transition point of the latch enable signal to the point at which the differential input signal equals V_{OS} and is specified for a particular value of V_{OD} (see definition below).

Latch Pulse Width (t_W)
The minimum time that the latch enable signal must be in the compare mode in order to acquire and subsequently hold an input signal change. Pulse width is measured between the 50% transition points of the latch enable pulse and is specified for a particular value of V_{OD} (see definition below).

Latch Setup Time (t_S)
The minimum time before the compare-to-latch transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the output. Setup time is measured from the point at which the differential input voltage equals V_{OS} to the 50% transition point of the latch enable signal and is specified for a particular value of V_{OD} (see definition below).

Output High Current (I_{OH})
The current that can be sourced at the output terminal at a specified output voltage.

Output High Voltage (V_{OH})
The high output voltage at a specified output source current and differential input voltage.

Output High Current (I_{OL})
The current that can be sunk at the output terminal at a specified output voltage.

Output Low Voltage (V_{OL})
The low output voltage at a specified output sink current and differential input voltage.

Overdrive (V_{OD})
The input overdrive (V_{OD}) is the applied differential input voltage (V_{IN}) in excess of the comparator input offset voltage (V_{OS}); i.e., $V_{OD} = V_{IN} - V_{OS}$. The dynamic response of a comparator depends on the input overdrive and, for this reason, such parameters as propagation delay and latch setup time, hold time, and pulse width are specified for a particular value of V_{OD}.

Power Supply Rejection Ratio (PSRR)
The ratio of the change in power supply voltage (over a specified power supply voltage range) to the corresponding change in V_{OS}. PSRR is expressed in dB where $PSRR(dB) = 20\log(\Delta PSV/\Delta V_{OS})$.

Voltage Gain (A_V)
The ratio of the change in output voltage (over a specified output voltage range) to the change in differential input voltage.

DESCRIPTION

The LM111 series are voltage comparators that have input currents approximately a hundred times lower than devices like the μA710. They are designed to operate over a wider range of supply voltages; from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL, and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50mA.

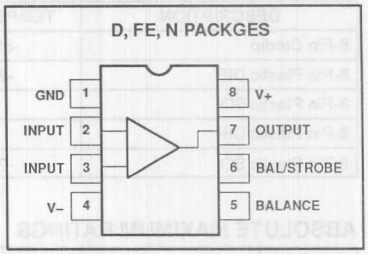
Both the inputs and the outputs of the LM111 series can be isolated from system ground, and the output can drive loads referred to ground, the positive supply, or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire-ORed.

Although slower than the μA710 (200ns response time vs 40ns), the devices are also much less prone to spurious oscillations. The LM111 series has the same pin configuration as the μA710 series.

FEATURES

- Operates from single 5V supply
- Maximum input bias current: 150nA (LM311—250nA)
- Maximum offset current: 20nA (LM311—50nA)
- Differential input voltage range: ±30V
- Power consumption: 135mW at ±15V
- High sensitivity—200V/mV
- Zero crossing detector

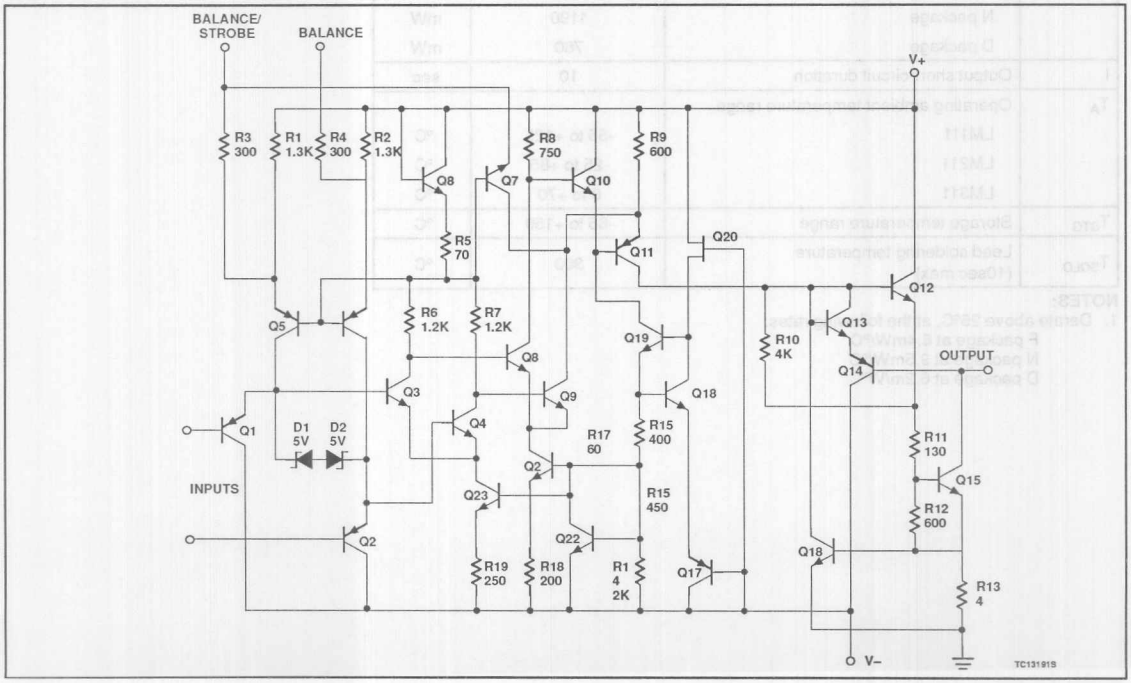
PIN CONFIGURTION



APPLICATIONS

- Precision squarer
- Positive/negative peak detector
- Low voltage adjustable reference supply
- Switching power amplifier

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Cerdip	-55°C to +125°C	LM111FE
8-Pin Plastic DIP	-25°C to +85°C	LM211N
8-Pin Plastic SO	0 to +70°C	LM311D
8-Pin Plastic DIP	0 to +70°C	LM311N
8-Pin Plastic SO	-25°C to +85°C	LM211D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Total supply voltage	36	V
	Output to negative supply voltage:		
	LM111/LM211	50	V
	LM311	40	V
	Ground to negative supply voltage	30	V
	Differential input voltage	±30	V
V_{IN}	Input voltage[1]	±15	V
$P_{D\ MAX}$	Maximum power dissipation, T_A=25°C (still-air)[1]		
	F package	810	mW
	N package	1190	mW
	D package	780	mW
I	Output short-circuit duration	10	sec
T_A	Operating ambient temperature range		
	LM111	-55 to +125	°C
	LM211	-25 to +85	°C
	LM311	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. Derate above 25°C, at the following rates:
   F package at 6.4mW/°C
   N package at 9.5mW/°C
   D package at 6.2m/W°C

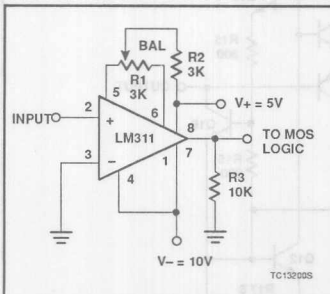
DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LM111/LM211			LM311			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[3]	T_A=25°C, R_S≤50kΩ		0.7	3.0		2.0	7.5	mV
I_{OS}	Input offset current[3]	T_A=25°C		4.0	10		6.0	50	nA
I_{BIAS}	Input bias current	T_A=25°C		60	100		100	250	nA
A_V	Voltage gain	T_A=25°C		200			200		V/mV
	Response time[4]	T_A=25°C		200			200		ns
	Saturation voltage	V_{IN}≤-5mV, I_{OUT}=50mA							
V_{SAT}		T_A=25°C		0.75	1.5		0.75	1.5	V
$I_{BAL/STR}$	Strobe on current	T_A=25°C		3.0			3.0		mA
	Output leakage current	V_{IN}≥5mV, V_{OUT}=35V							
$I_{LEAKAGE}$		T_A=25°C, I_{STROBE}=3mA		0.2	10		0.2	50	nA
V_{OS}	Input offset voltage[3]	R_S≤50kΩ			4.0			10	mV
I_{OS}	Input offset current[3]				20			70	nA
I_{BIAS}	Input bias current				150			300	nA
V_{IN}	Input voltage range	V=±15V (Pin 7 may go to 5V)	-14.5	13.8 -14.7	13.0	-14.5	13.8 -14.7	13.0	V
	Saturation voltage	V=p0≥4.5V, V-=0							
V_{OL}		V_{IN}≤-6mV, I_{SINK}≤8mA		0.23	0.4		0.23	0.4	V
I_{OH}	Output leakage current	V_{IN}≥5mV, V_{OUT}=35V		0.1	0.5				µA
I_{CC}	Positive supply current	T_A=25°C		5.1	6.0		5.1	7.5	mA
I_{EE}	Negative supply voltage	T_A=25°C		4.1	5.0		4.1	5.0	mA

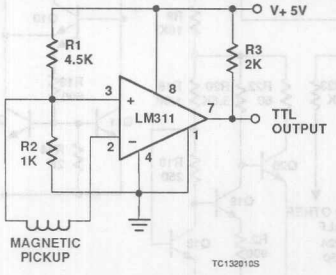
NOTES:

1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
2. These specifications apply for V_S=±15V and 0°C < T_A < 70°C unless otherwsie specified. With the LM211, however, all temperature specifications are limited to -25°C ≤ T_A ≤ 85°C and for the LM111 is limited to -55°C T_A < 125°C. The offset voltage, offset current, and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.
3. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
4. The response time specified is for a 100mV input step with 5mV overdrive.
5. Do not short the strobe pin to ground; it should be current driven at 3mA to 5mA.

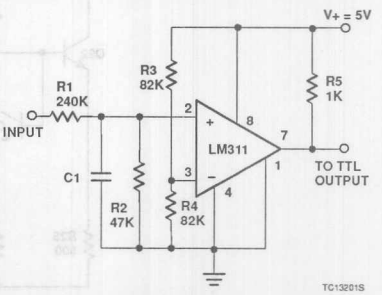
TYPICAL APPLICATIONS



Zero Detector
Driving MOS Logic



Detector for Magnetic
Transducer



TTL Interface with High
Level Logic

* Values shown are for a 0 to 30V logic swing and a 15V threshold.
** May be added to control speed and reduce susceptibility to noise spikes.

Dual voltage comparator LM319

DESCRIPTION

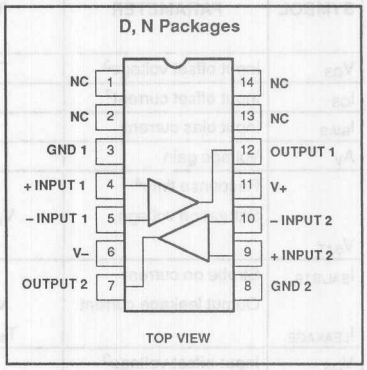
The LM319 series are precision high-speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the µA710. The uncommitted collector of the output stage makes the LM319 compatible with RTL, DTL, and TTL as well as capable of driving lamps and relays at currents up to 25mA.

Although designed primarily for applications requiring operation from digital logic supplies, the LM319 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high-speed, wide operating voltage range and low package count make the LM319 much more versatile than older devices like the µA711.

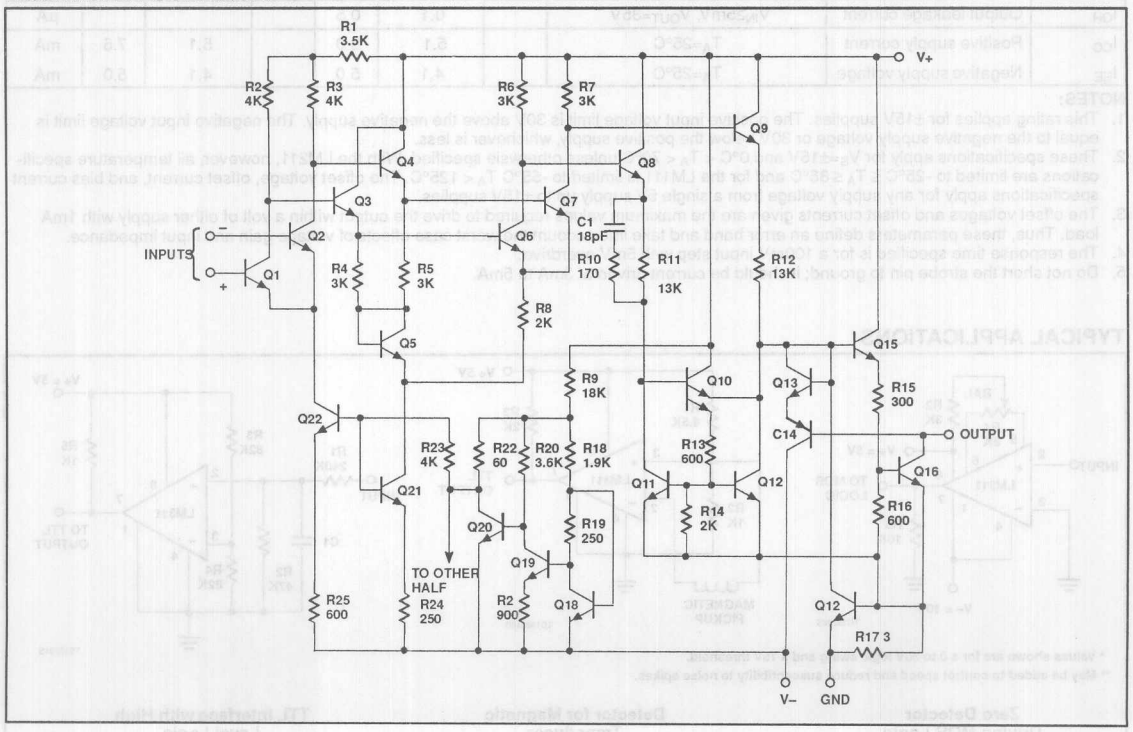
FEATURES

- Two independent comparators
- Operates from a single 5V supply
- Typically 80ns response time at ±15V
- Minimum fanout of 3 (each side)
- Maximum input current of 1µA over temperature
- Inputs and outputs can be isolated from system ground
- High common-mode slew rate

PIN CONFIGURATION



EQUIVALENT SCHEMATIC



Dual voltage comparator LM319

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	LM319D
14-Pin Plastic DIP	0 to +70°C	LM319N

ABSOLUTE MAXIMUM RATINGS

SYM-BOL	PARAMETER	RATING	UNIT
V_S	Total supply voltage	36	V
	Output to negative supply voltage	36	V
	Ground to negative supply voltage	25	V
	Ground to positive supply voltage	18	V
	Differential input voltage	±5	V
V_{IN}	Input voltage[1]	±15	V
	Maximum power dissipation, T_A=25°C (still-air)[2]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
	Output short-circuit duration	10	s
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. For supply voltages less than ±15V, the absolute maximum rating is equal to the supply voltage.
2. Derate above 25°C, at the following rates:
   N package at 11.4mW/°C
   D package at 8.3mW/°C

DC ELECTRICAL CHARACTERISTICS

V_S=+15V, 0°C ≤ T_A ≤ 70°C, unless otherwise specified. LM319,

SYMBOL	PARAMETER	TEST CONDITIONS	LM319			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage[1, 2]	R_S≤5kΩ, T_A=25°C		2.0	8.0	mV
		Over temp.			10	mV
I_{OS}	Input offset current[1, 2]	T_A=25°C		80	200	nA
		Over temp.			300	nA
I_B	Input bias current[1]	T_A=25°C		250	1000	nA
		Over temp.			1200	nA
A_V	Voltage gain	T_A=25°C	8	40		V/mV
V_{OL}	Saturation voltage	V_{IN}≤-10mV, I_{OUT}=25mA, T_A=25°C, V+≥4.5V, V-=0		0.75	1.5	V
		V_{IN}≤-10mV, I_{OUT}=3.2mA		0.3	0.4	V
I_{OH}	Output leakage current	V-=0V, V_{IN}≥10mV				
		V_{OUT}=35V, T_A=25°C		0.2	10	µA
V_{IN}	Input voltage range	V_S=±15V		±13		V
		V+=5V, V-=0V	1		3	V
V_{ID}	Differential input voltage				±5	V
I+	Positive supply current	V+=5V, V-=0V, T_A=25°C		4.3		mA
I+	Positive supply current	V_S=±15V, T_A=25°C		8.0	12.5	mA
I-	Negative supply current	V_S=±15V, T_A=25°C		3.0	5.0	mA

NOTES:

1. V_{OS}, I_{OS} and I_B specifications apply for a supply voltage range of V_S=±15V down to a single 5V supply.
2. The offset voltages and offset currents given are the maximum values required to drive the output to within 1V of either supply with a 1mA load. Thus these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

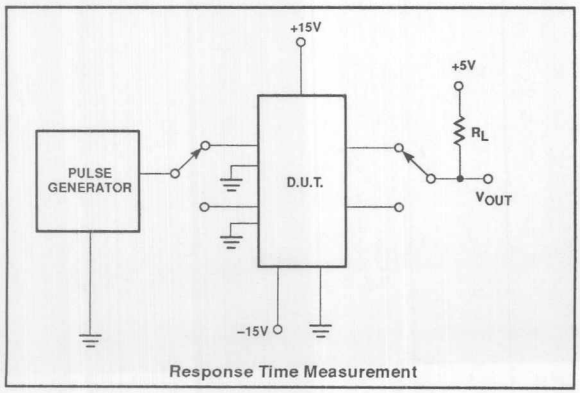
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_R	Response time[1]	V_S=±15V, T_A=25°C R_L=500Ω (see test figure)		80		ns

NOTES:

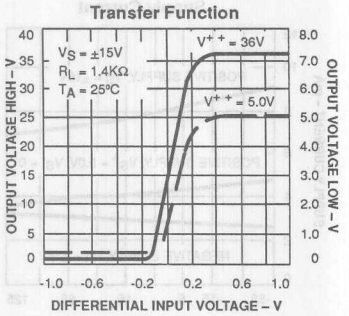
1. The response time specified is for a 100mV step with 5mV overdrive.

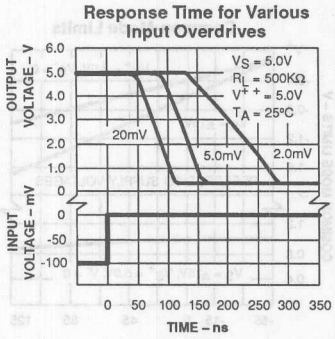
TEST CIRCUIT

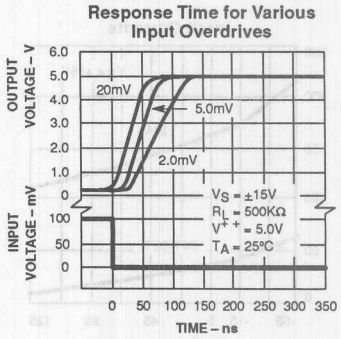


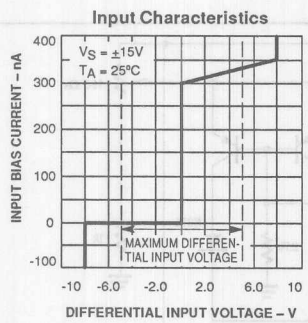
Response Time Measurement

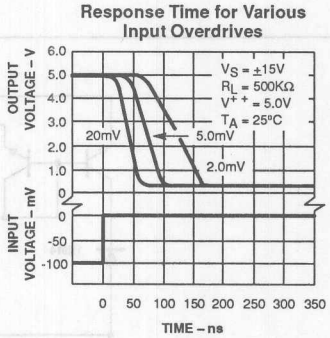
TYPICAL PERFORMANCE CHARACTERISTICS

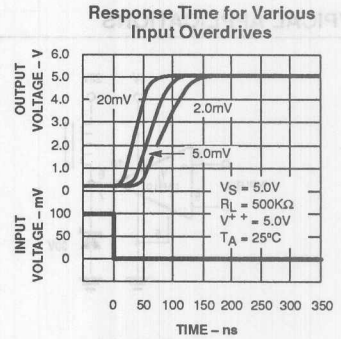


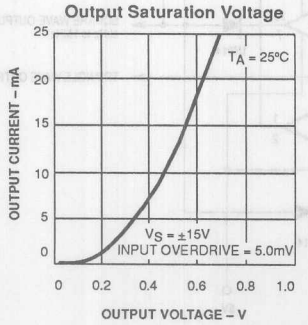


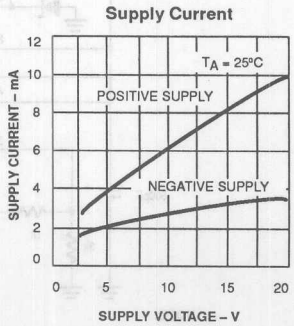


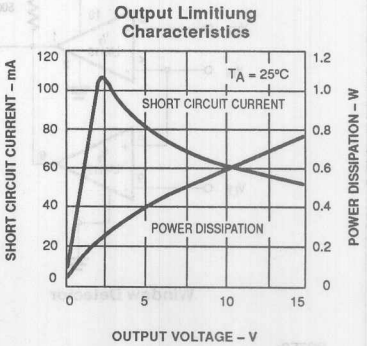




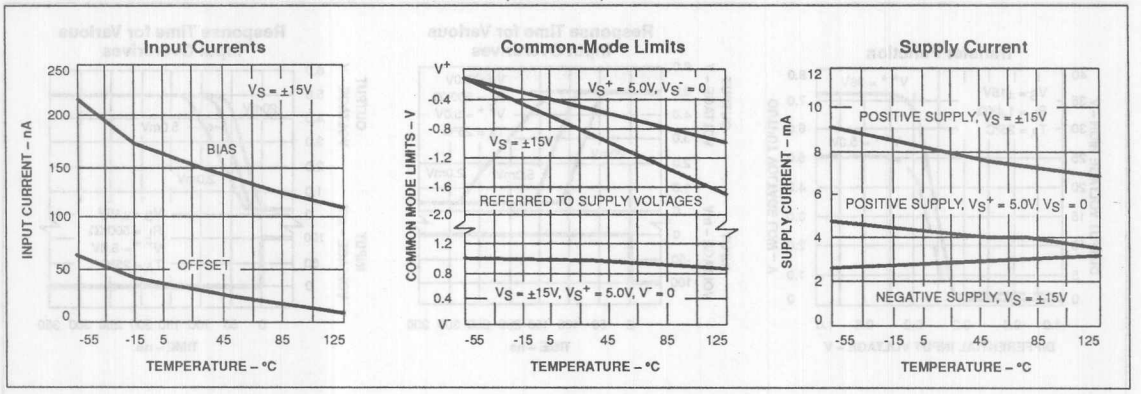




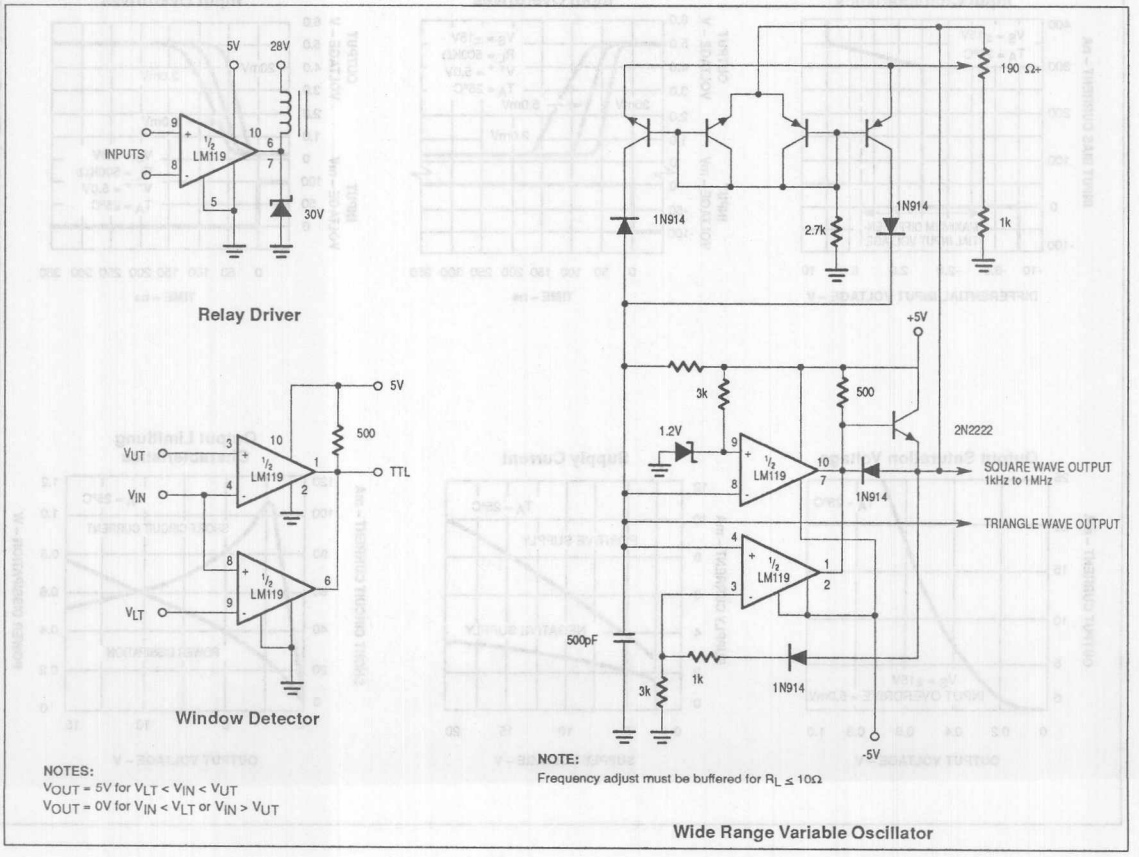




TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TYPICAL APPLICATIONS



Quad voltage comparator

LM139A/239A/339A/LM139 /239/339/LM2901/MC3302

DESCRIPTION

The LM139 series consists of four independent precision voltage comparators, with an offset voltage specification as low as 2.0mV max for each comparator, which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common–mode voltage range includes ground, even though they are operated from a single power supply voltage.

The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM139 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

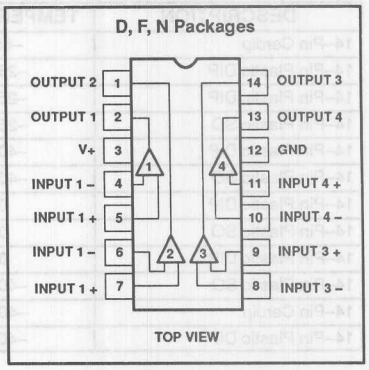
FEATURES

- Wide single supply voltage range 2.0V_{DC} to 36V_{DC} or dual supplies ±1.0V_{DC} to ±18V_{DC}
- Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/comparator at 5.0V_{DC})
- Low input biasing current 25nA
- Low input offset current ±5nA and offset voltage
- Input common–mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

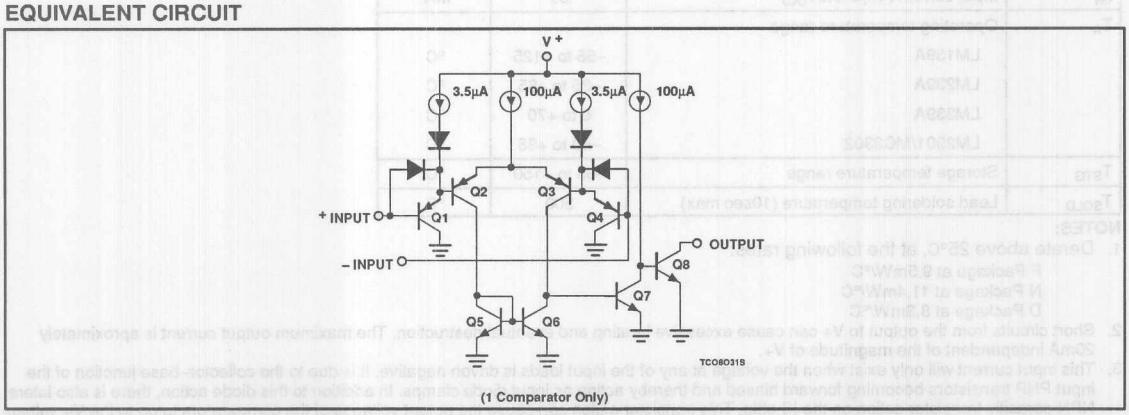
APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

PIN CONFIGURATION



EQUIVALENT CIRCUIT



(1 Comparator Only)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14–Pin Cerdip	–55 to +125°C	LM139F
14–Pin Plastic DIP	–25°C to +85°C	LM239AN
14–Pin Plastic DIP	–25°C to +85°C	LM239N
14–Pin Plastic SO	–25°C to +85°C	LM239D
14–Pin Plastic DIP	–40°C to +85°C	LM2901N
14–Pin Plastic SO	–40°C to +85°C	LM2901D
14–Pin Plastic DIP	0 to +70°C	LM339AN
14–Pin Plastic SO	0 to +70°C	LM339D
14–Pin Plastic DIP	0 to +70°C	LM339N
14–Pin Plastic SO	–40°C to +85°C	MC3302D
14–Pin Cerdip	–40°C to +85°C	MC3302F
14–Pin Plastic DIP	–40°C to +85°C	MC3302N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	V_{CC} supply voltage	36 or ±18	V_{DC}
V_{DIFF}	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	–0.3 to +36	V_{DC}
P_D	Maximum power dissipation, T_A=25°C (still–air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
	Output short–circuit to ground[2]	Continuous	
I_{IN}	Input current (V_{IN}<–0.3V_{DC})[3]	50	mA
T_A	Operating temperature range		
	LM139A	–55 to +125	°C
	LM239A	–25 to +85	°C
	LM339A	0 to +70	°C
	LM2901/MC3302	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   F Package at 9.5mW/°C
   N Package at 11.4mW/°C
   D Package at 8.3mW/°C
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is aproximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector–base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than –0.3V_{DC}.

DC AND AC ELECTRICAL CHARACTERISTICS

$V+=5V_{DC}$, LM139A/LM139: $-55°C \le T_A \le 125°C$; LM239: $-25°C \le T_A \le 85°C$; LM339: $0°C \le T_A \le 70°C$; LM339A: $0°C \le T_A \le 70°C$; LM239A: $-25°C \le T_A \le 85°C$; LM2901/LM3302: $-40°C \le T_A \le 85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM139A			LM239A/339A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	T_A=25°C Over temp.		±1.0	±2.0 ±4.0		±1.0	±2.0 ±4.0	mV mV
V_{CM}	Input common–mode voltage range[3]	T_A=25°C Over temp.	0 0		V+–1.5 V+–2.0	0 0		V+–1.5 V+–2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}'s≥0V_{DC} (or V– if need)			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A=25°C Over temp.		25	100 300		25	250 400	nA nA
I_{OS}	Input offset current	$I_{IN(+)}-I_{IN(-)}$ T_A=25°C Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}$=0, V_O≤1.5V_{DC}, T_A=25°C V_O=800mV, over temp.	6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)}$≥1V_{DC}, $V_{IN(-)}$=0 V_O=5V_{DC}, T_A=25°C V_O=30V_{DC}, over temp.		0.1	 1.0		0.1	 1.0	nA µA
I_{CC}	Supply current	V+=5V, R_L=∞ on comparators, T_A=25°C V+=30V		0.8	2.0		0.8	2.0	mA
A_V	Voltage gain	R_L≥15kΩ, V+=15V_{DC}	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4mA T_A=25°C Over temp.		250	400 700		250	400 700	mV mV
t_{LSR}	Large–signal response time	V_{IN}=TTL logic swing, V_{REF}=1.4V_{DC}, V_{RL}=5V_{DC}, R_L=5.1kΩ, T_A=25°C		300			300		ns
t_R	Response time[5]	V_{RL}=5V_{DC}, R_L=5.1kΩ, T_A=25°C		1.3			1.3		µs

See notes at the end of the Electrical Characteristics.

DC AND AC ELECTRICAL CHARACTERISTICS

$V+=5V_{DC}$, LM139A/LM139: $-55°C \le T_A \le 125°C$; LM239: $-25°C \le T_A \le 85°C$; LM339: $0°C \le T_A \le 70°C$; LM339A: $0°C \le T_A \le 70°C$; LM239A: $-25°C \le T_A \le 85°C$; LM2901/LM3302: $-40°C \le T_A \le 85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM139			LM239/339			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	T_A=25°C Over temp.		±2.0	±5.0 ±9.0		±2.0	±5.0 ±9.0	mV mV
V_{CM}	Input common–mode voltage range[3]	T_A=25°C Over temp.	0 0		V+–1.5 V+–2.0	0 0		V+–1.5 V+–2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}'s≥0V_{DC} (or V– if need)			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A=25°C Over temp.		25	100 300		25	250 400	nA nA
I_{OS}	Input offset current	$I_{IN(+)}$–$I_{IN(-)}$ T_A=25°C Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)}$≥1V_{DC}, $V_{IN}(+)$=0, V_O≤1.5V_{DC}, T_A=25°C V_O=800mV, over temp.	6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)}$≥1V_{DC}, $V_{IN(-)}$=0 V_O=5V_{DC}, T_A=25°C V_O=30V_{DC}, over temp.		0.1	 1.0		0.1	 1.0	nA µA
I_{CC}	Supply current	V+=5V, R_L=∞ on comparators, T_A=25°C V+=30V		0.8	2.0		0.8	2.0	mA
A_V	Voltage gain	R_L≥15kΩ, V+=15V_{DC}	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4mA T_A=25°C Over temp.		250	400 700		250	400 700	mV mV
t_{LSR}	Large–signal response time	V_{IN}=TTL logic swing, V_{REF}=1.4V_{DC}, V_{RL}=5V_{DC}, R_L=5.1kΩ, T_A=25°C		300			300		ns
t_R	Response time[5]	V_{RL}=5V_{DC}, R_L=5.1kΩ, T_A=25°C		1.3			1.3		µs

See notes on following page.

DC AND AC ELECTRICAL CHARACTERISTICS

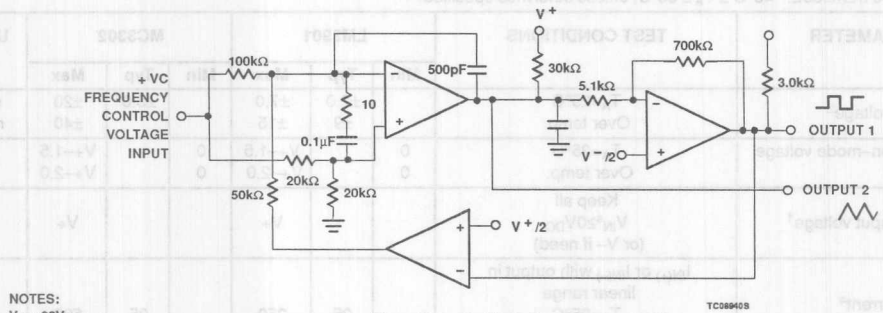
$V+=5V_{DC}$, LM139A/LM139: $-55°C \le T_A \le 125°C$; LM239: $-25°C \le T_A \le 85°C$; LM339: $0°C \le T_A \le 70°C$; LM339A: $0°C \le T_A \le 70°C$; LM239A: $-25°C \le T_A \le 85°C$; LM2901/LM3302: $-40°C \le T_A \le 85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM2901			MC3302			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A=25°C$ Over temp.		±2.0 ±9	±7.0 ±15		±3.0	±20 ±40	mV mV
V_{CM}	Input common–mode voltage range[3]	$T_A=25°C$ Over temp.	0 0		V+–1.5 V+–2.0	0 0		V+–1.5 V+–2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}'s$\ge 0V_{DC}$ (or V– if need)			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A=25°C$ Over temp.		 25 200	 250 500		 25	 500 1000	 nA nA
I_{OS}	Input offset current	$I_{IN(+)}-I_{IN(-)}$ $T_A=25°C$ Over temp.		 ±5 ±50	 ±50 ±200		 ±5	 ±100 ±300	 nA nA
I_{OL}	Output sink current	$V_{IN(-)}\ge 1V_{DC}$, $V_{IN}(+)=0$, $V_O\le 1.5V_{DC}$, $T_A=25°C$ $V_O=800mV$, over temp.	6.0	16		 2.0	6		mA mA
I_{OH}	Output leakage current	$V_{IN(+)}\ge 1V_{DC}$, $V_{IN}(-)=0$ $V_O=5V_{DC}$, $T_A=25°C$ $V_O=30V_{DC}$, over temp.		0.1	 1.0		0.1	 1.0	nA µA
I_{CC}	Supply current	V+=5V, $R_L=\infty$ on comparators, $T_A=25°C$ V+=30V		 0.8 1.0	 2.0 2.5		.8	1.8	mA
A_V	Voltage gain	$R_L\ge 15k\Omega$, $V+=15V_{DC}$	25	100		2	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)}\ge 1V_{DC}$, $V_{IN(+)}=0$, $I_{SINK}\le 4mA$ $T_A=25°C$ Over temp.		 400	 700		 150	 400 700	 mV mV
t_{LSR}	Large–signal response time	V_{IN}=TTL logic swing, $V_{REF}=1.4V_{DC}$, $V_{RL}=5V_{DC}$, $R_L=5.1k\Omega$, $T_A=25°C$		300			300		ns
t_R	Response time[5]	$V_{RL}=5V_{DC}$, $R_L=5.1k\Omega$, $T_A=25°C$		1.3			1.3		µs

NOTES:

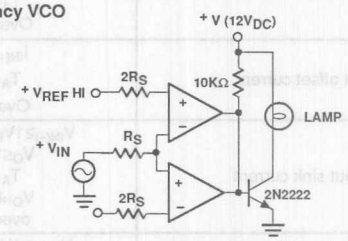
1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common–mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{DC}$ (or $0.3V_{DC}$ below the magnitude of the negative power supply, if used).
2. At output switch point, $V_O \approx 1.4V_{DC}$, $R_S=0\Omega$ with V+ from $5V_{DC}$ to $30V_{DC}$; and over the full input common–mode range ($0V_{DC}$ to $V+ - 1.5V_{DC}$). Inputs of unused comparators should be grounded.
3. The input common–mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common–mode voltage range is V+ – 1.5V, but either or both inputs can go to $30V_{DC}$ without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained (see typical *performance characteristics section*).

EQUIVALENT CIRCUIT

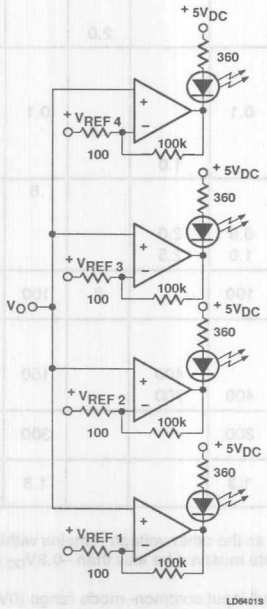


NOTES:
$V_+ = 30V_{DC}$
$+ 250m\ V_{DC} \leq V_C = 50V_{DC}$
$700H \leq f_O = 100kHz$

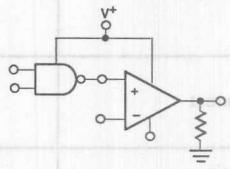
Two–Decade High–Frequency VCO



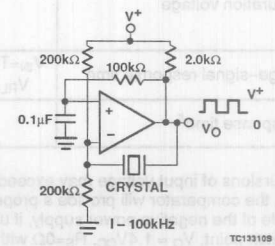
Limit Comparator



Visable Voltage Indicator



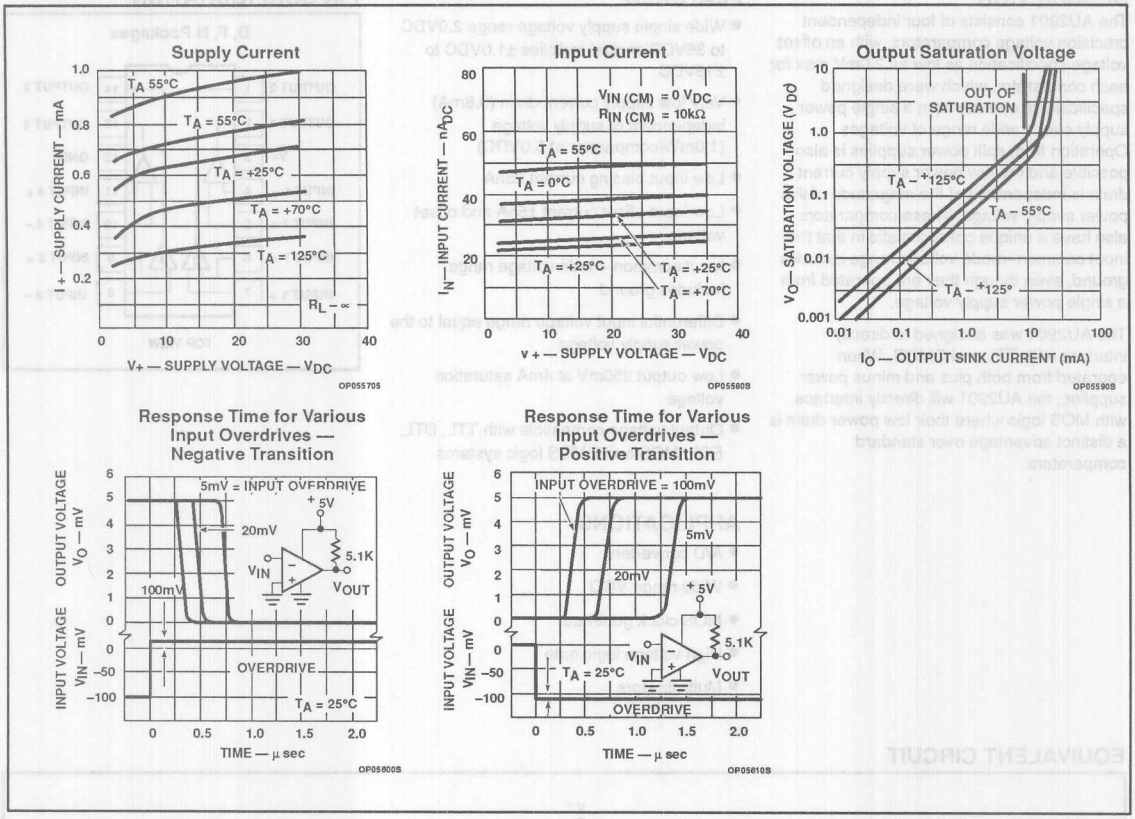
TTL–to–MOS Logic Converter



Crystal–Controlled Oscillator

NOTE:
Input of unused comparators should be grounded.

TYPICAL PERFORMANCE CHARACTERISTICS



Quad voltage comparator

AU2901

DESCRIPTION

The AU2901 consists of four independent precision voltage comparators, with an offset voltage specification as low as 2.0mV max for each comparator, which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common–mode voltage range includes ground, even though they are operated from a single power supply voltage.

The AU2901 was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the AU2901 will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

FEATURES

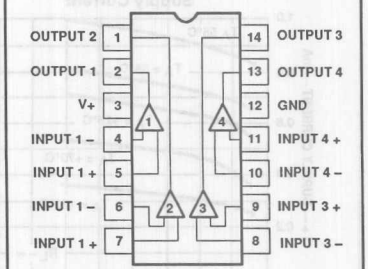
- Wide single supply voltage range 2.0VDC to 36VDC or dual supplies ±1.0VDC to ±18VDC
- Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/comparator at 5.0VDC)
- Low input biasing current 25nA
- Low input offset current ±5nA and offset voltage
- Input common–mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

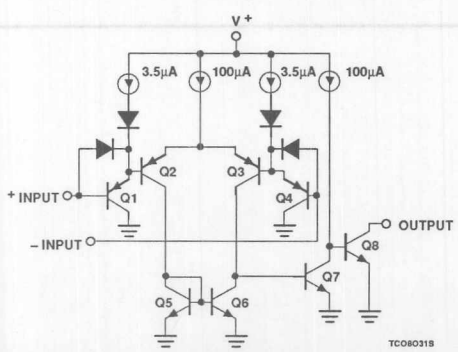
PIN CONFIGURATION

D, F, N Packages



TOP VIEW

EQUIVALENT CIRCUIT



(One Comparator Only)

Quad voltage comparator AU2901

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14–Pin Plastic SO	–40°C to +125°C	AU2901D
14–Pin Plastic DIP	–40°C to +125°C	AU2901N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	V_{CC} supply voltage	36 or ±18	V_{DC}
V_{DIFF}	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	–0.3 to +36	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A=25°C (still–air)[1]		
	N package	1420	mW
	D package	1040	mW
	Output short–circuit to ground[2]	Continuous	
I_{IN}	Input current (V_{IN}<–0.3V_{DC})[3]	50	mA
T_A	Operating temperature range		
	AU2901	–40 to +125	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   N Package at 11.4mW/°C
   D Package at 8.3mW/°C
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is aproximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector–base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than –0.3V_{DC}.

ELECTRICAL CHARACTERISTICS

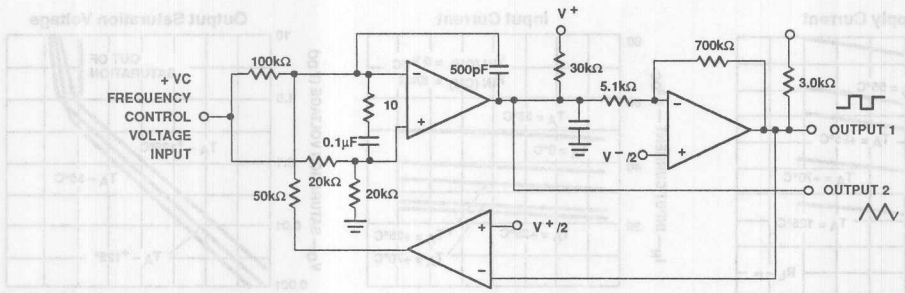
V+=5V_{DC}, AU2901: –40°C, T_A ≤ 125°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	AU2901			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage[2]	T_A = 25°C Over temp.		±2.0 ±9	±7.0 ±15	mV
V_{CM}	Input common–mode voltage[3] range	T_A = 25°C Over temp.	0 0		V+–1.5 V+–2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}'s ≥ 0V_{DC} (or V– if need)			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A = 25°C Over temp.		25 200	250 500	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ T_A = 25°C Over temp.		±5 ±50	±50 ±200	nA nA
I_{OL}	Output sink current	$V_{IN(-)}$ ≥ 1V_{DC}, V_{IN}(+) = 0, V_O ≤ 1.5V_{DC}, T_A = 25°C	6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)}$ ≥ 1V_{DC}, V_{IN}(–) = 0 V_O = 5V_{DC}, T_A = 25°C V_O = 30V_{DC}, Over temp.		0.1	 1.0	nA µA
I_{CC}	Supply current	V+ = 5V, R_L = ∞ on comparators, T_A = 25°C V+ = 30V		0.8 1.0	2.0 2.5	mA
A_V	Voltage gain	R_L ≥ 15kΩ, V+ = 15V_{DC}	25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)}$ ≥ 1V_{DC}, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4mA T_A = 25°C Over temp.		 400	 400 700	mV
t_{LSR}	Large–signal response time	V_{IN} = TTL logic swing, V_{REF} = 1.4V_{DC}, V_{RL} = 5V_{DC}, R_L = 5.1kΩ, T_A = 25°C		300		ns
t_R	Response time[5]	V_{RL} = 5V_{DC}, R_L = 5.1kΩ, T_A = 25°C		1.3		µs

NOTES:

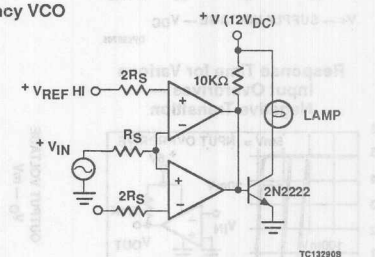
1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common–mode range, the comparator will provide a proper output state. The low input voltage state must not be less than –0.3V_{DC} (or 0.3V_{DC} below the magnitude of the negative power supply, if used).
2. At output switch point, V_O ≈ 1.4V_{DC}, R_S=0Ω with V+ from 5V_{DC} to 30V_{DC}; and over the full input common–mode range (0V_{DC} to V+ – 1.5V_{DC}).
3. The input common–mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common–mode voltage range is V+ – 1.5V, but either or both inputs can go to 30V_{DC} without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained (see Typical Performance Characteristics section).

EQUIVALENT CIRCUIT

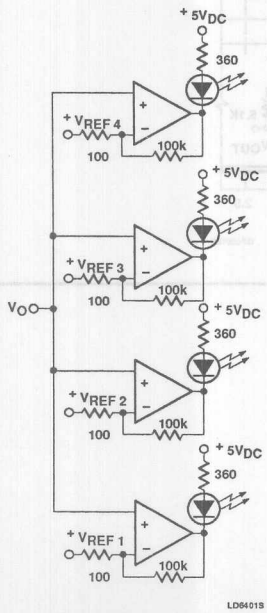


NOTES:
$V_+ = 30V_{DC}$
$+250m\ V_{DC} \le V_C = 50V_{DC}$
$700H \le f_O = 100kHz$

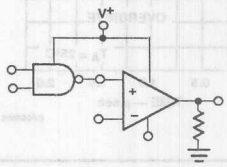
Two–Decade High–Frequency VCO



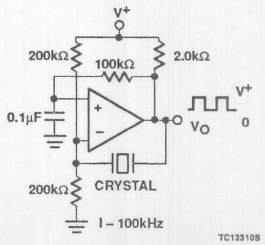
Limit Comparator



Visable Voltage Indicator



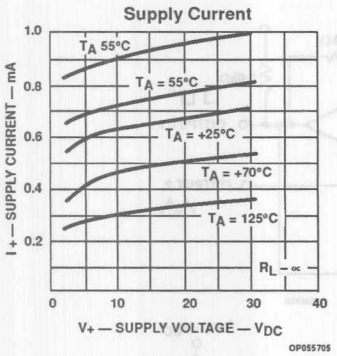
TTL–to–MOS Logic Converter

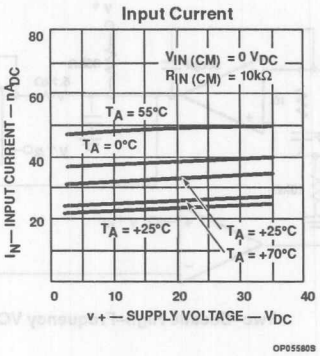


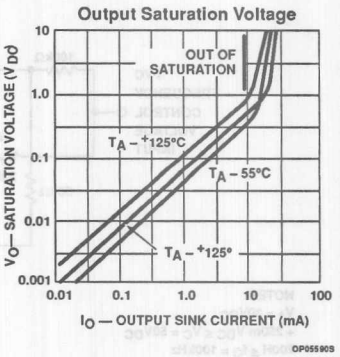
Crystal–Controlled Oscillator

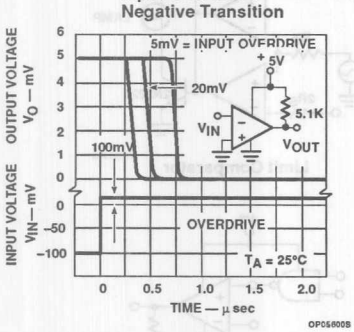
NOTE:
Input of unused comparators should be grounded.

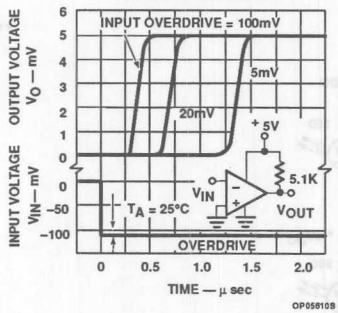
TYPICAL PERFORMANCE CHARACTERISTICS











Low power dual voltage comparator LM193/A/293/A/393/A/2903

DESCRIPTION

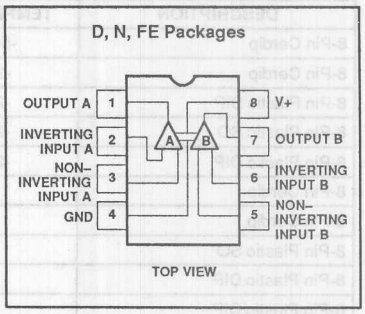
The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max. for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

FEATURES

- Wide single supply voltage range 2.0VDC to 36VDC or dual supplies ±1.0VDC, to ±18VDC
- Very low supply current drain (0.8mA) independent of supply voltage (2.0mW/comparator at 5.0VDC)
- Low input biasing current 25nA
- Low input offset current ±5nA and offset voltage ±2mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

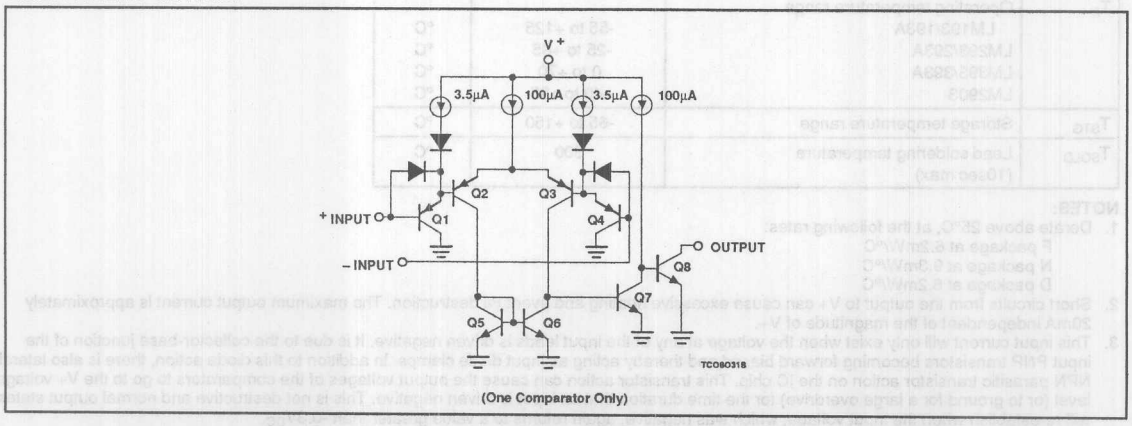
PIN CONFIGURATION



APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

EQUIVALENT CIRCUIT



Low power dual voltage comparator LM193/A/293/A/393/A/2903

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Cerdip	-55°C to +125°C	LM193FE
8-Pin Cerdip	-25°C to +85°C	LM293FE
8-Pin Plastic DIP	-25°C to +85°C	LM293N
8-Pin Plastic SO	-25°C to +85°C	LM293D
8-Pin Plastic DIP	-25°C to +85°C	LM293AN
8-Pin Cerdip	0 to +70°C	LM393AFE
8-Pin Cerdip	0 to +70°C	LM393FE
8-Pin Plastic SO	0 to +70°C	LM393D
8-Pin Plastic DIP	0 to +70°C	LM393N
8-Pin Plastic DIP	0 to +70°C	LM393AN
8-Pin Plastic DIP	-40°C to +85°C	LM2903N
8-Pin Plastic DIP	-40°C to +85°C	LM2903D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	36 or ±18	V_{DC}
	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	-0.3 to +36	V_{DC}
P_D	Maximum power dissipation, T_A=25°C (still-air)[1]		
	F package	780	mW
	N package	1160	mW
	D package	780	mW
	Output short-circuit to ground[2]	Continuous	
I_{IN}	Input current (V_{IN}<-0.3V_{DC})[3]	50	mA
T_A	Operating temperature range		
	LM193/193A	-55 to +125	°C
	LM293/293A	-25 to +85	°C
	LM393/393A	0 to +70	°C
	LM2903	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V_{DC}.

DC AND AC ELECTRICAL CHARACTERISTICS

V+=5VDC, LM193/193A: -55°C $T_A \leq +125°C$, unless otherwise specified. LM293/293A: -25°C $T_A \leq +85°C$, unless otherwise specified. LM393/393A: 0°C $T_A \leq +70°C$, unless otherwise specified. LM2903: -40°C $T_A \leq +85°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LM193A			LM293A/393A			LM2903			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	T_A=25°C Over temp.		±1.0	±2.0 ±4.0		±1.0	±2.0 ±4.0		±2.0 ±9	±7.0 ±15	mV mV
V_{CM}	Input common-mode voltage range[3, 6]	T_A=25°C Over temp.	0 0		V+-1.5 V+-2.0	0 0		V+-1.5 V+-2.0	0 0		V+-1.5 V+-2.0	V V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s ≥0V_{DC} (or V- if need)			V+			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A=25°C Over temp.		25	100 300		25	250 400		25 200	250 500	nA nA
I_{OS}	Input offset current	$I_{IN(+)}$-$I_{IN(-)}$ T_A=25°C Over temp.		±3.0	±25 ±100		±5.0	±50 ±150		±5 ±50	±50 ±200	nA nA
I_{OL}	Output sink current	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}$=0, V_O≤1.5V_{DC} T_A=25°C	6.0	16		6.0	16		6.0	16		mA
I_{OH}	Output leakage current	V_O=5V_{DC}, T_A=25°C $V_{IN(+)}$≥1V_{DC}, $V_{IN(-)}$=0 V_O=30V_{DC} Over temp.		0.1	 1.0		0.1	 1.0		0.1	 1.0	µA nA
I_{CC}	Supply current	R_L=∞ on both comparators. T_A=25°C V+=30V, over temp.		0.8 1	1 2.5		0.8 1	1 2.5		0.8 1	1 2.5	mA mA
A_V	Voltage gain	R_L≥15kΩ, V+=15V_{DC}, T_A=25°C	50	200		50	200		25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4mA T_A=25°C Over temp.		250	400 700		250	400 700		400	400 700	mV mV
t_{LSR}	Large-signal response time	V_{IN}=TTL logic swing, V_{REF}=1.4V_{DC} V_{RL}=5V_{DC}, R_L=5.1kΩ, T_A=25°C		300			300			300		ns
t_R	Response time[5]	V_{RL}=5V_{DC}, R_L=5.1kΩ T_A=25°C		1.3			1.3			1.3		µs

DC ELECTRICAL CHARACTERISTICS (Continued)

V+=5VDC, LM193/193A: -55°C $T_A \leq +125°C$, unless otherwise specified. LM293/293A: -25°C $T_A \leq +85°C$, unless otherwise specified. LM393/393A: 0°C $T_A \leq +70°C$, unless otherwise specified. LM2903: -40°C $T_A \leq +85°C$, unless otherwise specified.

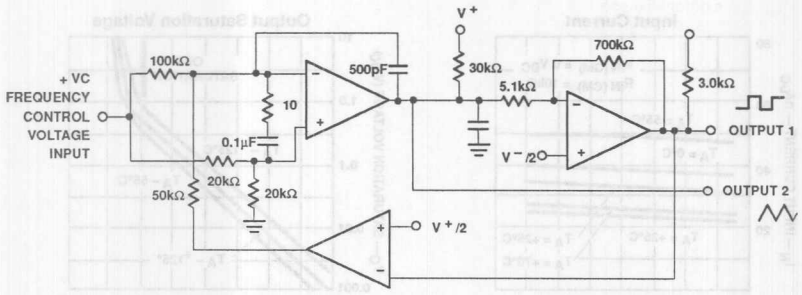
SYMBOL	PARAMETER	TEST CONDITIONS	LM193			LM293/393			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[2]	T_A=25°C Over temp.		±2.0	±5.0 ±9.0		±2.0	±5.0 ±9.0	mV mV
V_{CM}	Input common-mode voltage range[3, 6]	T_A=25°C Over temp.	0 0		V±-1.5 V±-2.0	0 0		V+-1.5 V+-2.0	V V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s ≥0V_{DC} (or V-if need)			V+			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A=25°C Over temp.		25	100 300		25	250 400	nA nA
I_{OS}	Input offset current	$I_{IN(+)}$-$I_{IN(-)}$ T_A=25°C Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}$=0, V_O≤1.5V_{DC} T_A=25°C	6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)}$≥1V_{DC}, $V_{IN(-)}$=0, V_O=5V_{DC} T_A=25°C V_O=30VDC over temp.		0.1	 1.0		0.1	 1.0	nA µA
I_{CC}	Supply current	R_L=∞ on both comparators T_A=25°C V+=30V, over temp.		0.8	1 2.5		0.8	1 2.5	mA mA
A_V	Voltage gain	R_L≥15kΩ, V+=15V_{DC}	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)}$≥1V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4mA T_A=25°C Over temp.		250	400 700		250	400 700	mV mV
t_{LSR}	Large signal response time	V_{IN}=TTL logic swing, V_{REF}=1.4V_{DC}, V_{RL}=5V_{DC} R_L=5.1kΩ, T_A=25°C		300			300		ns
t_R	Response time[5]	V_{RL}=5V_{DC}, R_L=5.1kΩ T_A=25°C		1.3			1.3		µs

NOTES:

1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3V_{DC} (V_{DC} below the magnitude of the negative power supply, if used).
2. At output switch point, $V_O \approx 1.4V_{DC}$, R_S=0Ω with V+ from 5V_{DC} to 30V_{DC} and over the full input common-mode range (0V_{DC} to V+-1.5V_{DC}).
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+-1.5V, but either or both inputs can go to 30V_{DC} without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100mV input step with a 5mV overdrive.
6. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

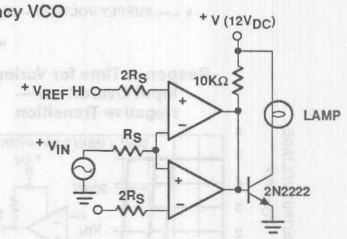
Low power dual voltage comparator LM193/A/293/A/393/A/2903

EQUIVALENT CIRCUIT

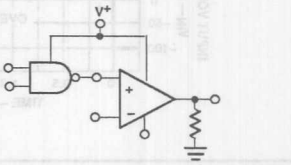


NOTES:
V+ = 30V$_{DC}$
+ 250m V$_{DC}$ ≤ V$_C$ = 50V$_{DC}$
700H ≤ f$_O$ = 100kHz

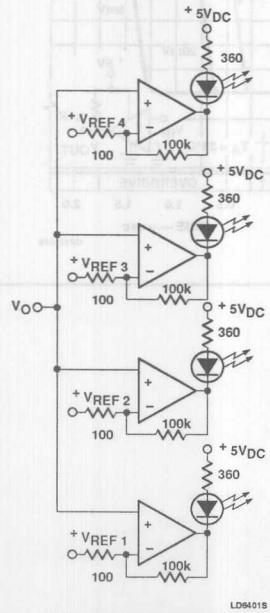
Two–Decade High–Frequency VCO



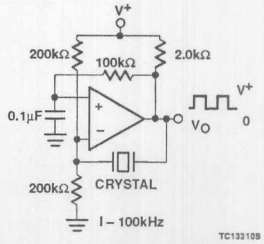
Limit Comparator



TTL–to–MOS Logic Converter



Visable Voltage Indicator

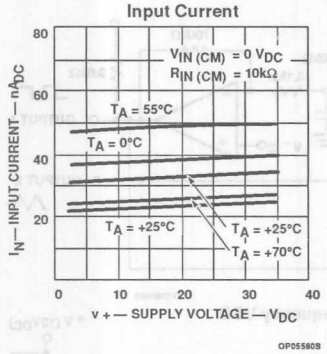


Crystal–Controlled Oscillator

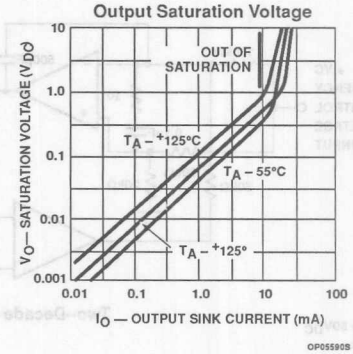
NOTE:
Input of unused comparators should be grounded.

TYPICAL PERFORMANCE CHARACTERISTICS

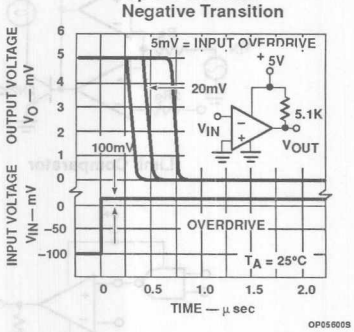
Input Current



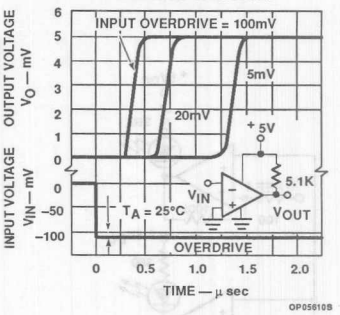
Output Saturation Voltage



Response Time for Various Input Overdrives — Negative Transition



Response Time for Various Input Overdrives — Positive Transition



Low power dual voltage comparator AU2903

DESCRIPTION

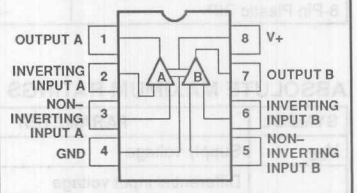
The AU2903 consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max. for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

FEATURES

- Wide single supply voltage range 2.0V_{DC} to 36V_{DC} or dual supplies ±1.0V_{DC}, to ±18V_{DC}
- Very low supply current drain (0.8mA) independent of supply voltage (2.0mW/comparator at 5.0V_{DC})
- Low input biasing current 25nA
- Low input offset current ±5nA and offset voltage ±2mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

PIN CONFIGURATION

D and N Packages

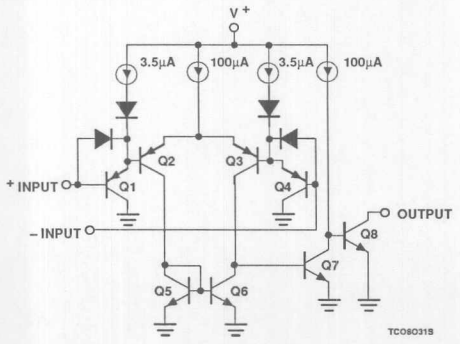


TOP VIEW

APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

EQUIVALENT CIRCUIT



(1 Comparator Only)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	-40°C to +125°C	AU2903D
8-Pin Plastic DIP	-40°C to +125°C	AU2903N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	36 or ±18	V_{DC}
	Differential input voltage	36	V_{DC}
V_{IN}	Input voltage	-0.3 to +36	V_{DC}
P_{DMAX}	Maximum power dissipation, T_A=25°C (still-air)[3]		
	N package	1160	mW
	D package	780	mW
	Output short-circuit to ground[1]	Continuous	
I_{IN}	Input current (V_{IN}<-0.3V_{DC})[2]	50	mA
T_A	Operating temperature range		
	AU2903	-40 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V_{DC}.
3. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C

DC AND AC ELECTRICAL CHARACTERISTICS

$V+=5V_{DC}$, AU2903; -40°C, $T_A \leq +125°C$, unless otherwise specified.

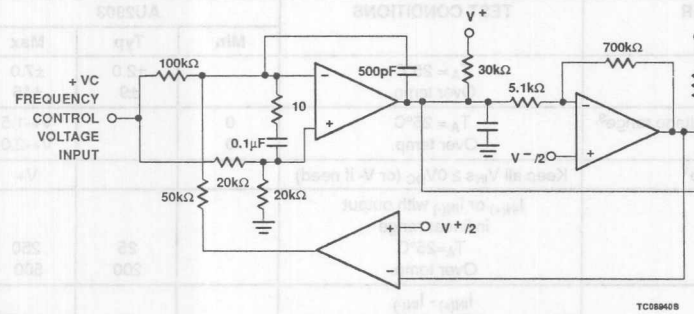
SYMBOL	PARAMETER	TEST CONDITIONS	AU2903			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage[2]	$T_A = 25°C$ Over temp.		±2.0 ±9	±7.0 ±15	mV
V_{CM}	Input common-mode voltage range[3, 6]	$T_A = 25°C$ Over temp.	0 0		V+-1.5 V+-2.0	V
V_{IDR}	Differential input voltage[1]	Keep all V_{IN}s $\geq 0V_{DC}$ (or V- if need)			V+	V
I_{BIAS}	Input bias current[4]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A=25°C Over temp.		25 200	250 500	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±5 ±50	±50 ±200	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $V_O \leq 1.5V_{DC}$ $T_A = 25°C$	6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1V_{DC}$, $V_{IN(-)} = 0$ $V_O = 5V_{DC}$, $T_A = 25°C$ $V_O = 30V_{DC}$, over temp.		0.1	 1.0	nA µA
I_{CC}	Supply current	$R_L = \infty$ on both comparators. $T_A = 25°C$ V+ = 30V, over temp.		0.8 1	1 2.5	mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15V_{DC}$, $T_A = 25°C$	25	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp.		400	400 700	mV
t_{LSR}	Large-signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4V_{DC}$ $V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300		ns
t_R	Response time[5]	$V_{RL} = 5V_{DC}$, $R_L = 5.1k\Omega$ $T_A = 25°C$		1.3		µs

NOTES:

1. Positive excursions of input voltage may exceed the power supply level by 17V. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{DC}$ (V_{DC} below the magnitude of the negative power supply, if used).
2. At output switch point, $V_O \approx 1.4V_{DC}$, $R_S = 0\Omega$ with V+ from $5V_{DC}$ to $30V_{DC}$ and over the full input common-mode range ($0V_{DC}$ to $V+-1.5V_{DC}$).
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+-1.5V, but either or both inputs can go to $30V_{DC}$ without damage.
4. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The response time specified is for a 100mV input step with a 5mV overdrive.
6. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

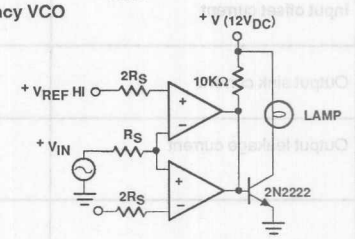
Low power dual voltage comparator AU2903

TYPICAL APPLICATIONS

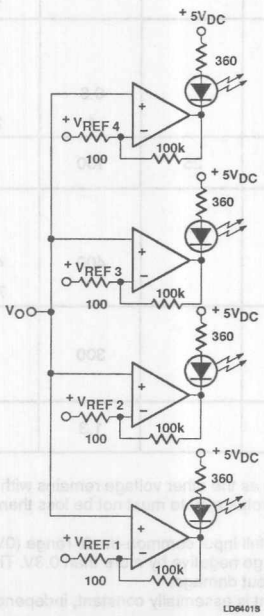


NOTES:
$V_+ = 30V_{DC}$
$+ 250m\ V_{DC} \leq V_C = 50V_{DC}$
$700H \leq f_O = 100kHz$

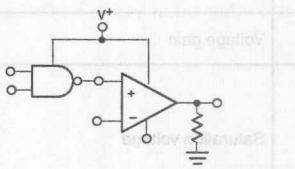
Two–Decade High–Frequency VCO



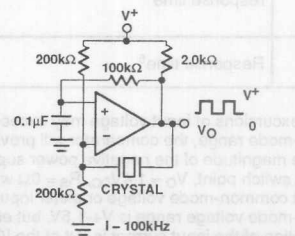
Limit Comparator



Visable Voltage Indicator



TTL–to–MOS Logic Converter

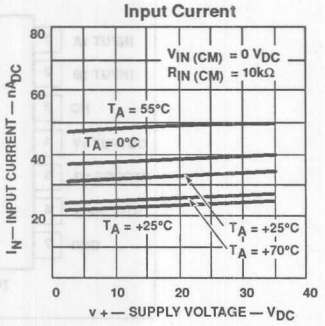


Crystal–Controlled Oscillator

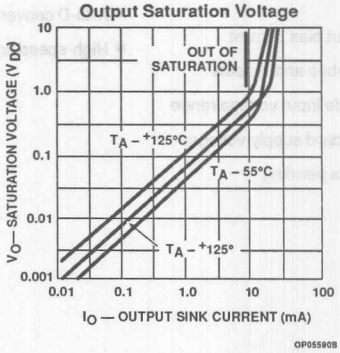
NOTE:
Input of unused comparators should be grounded.

TYPICAL PERFORMANCE CHARACTERISTICS

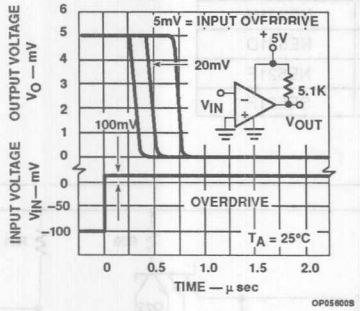
Input Current



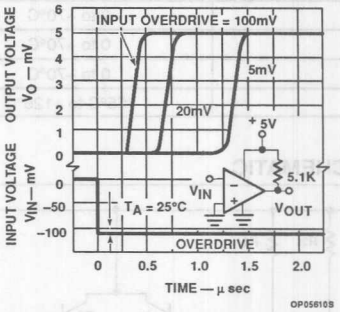
Output Saturation Voltage



Response Time for Various Input Overdrives — Negative Transition



Response Time for Various Input Overdrives — Positive Transition



High-speed dual-differential comparator/sense amp NE/SE521

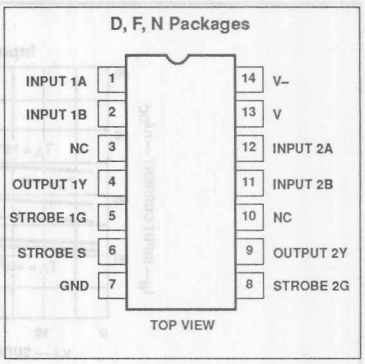
FEATURES

- 12ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- TTL compatible strobes and outputs
- Large common-mode input voltage range
- Operates from standard supply voltages
- Military qualifications pending

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High-speed line receiver

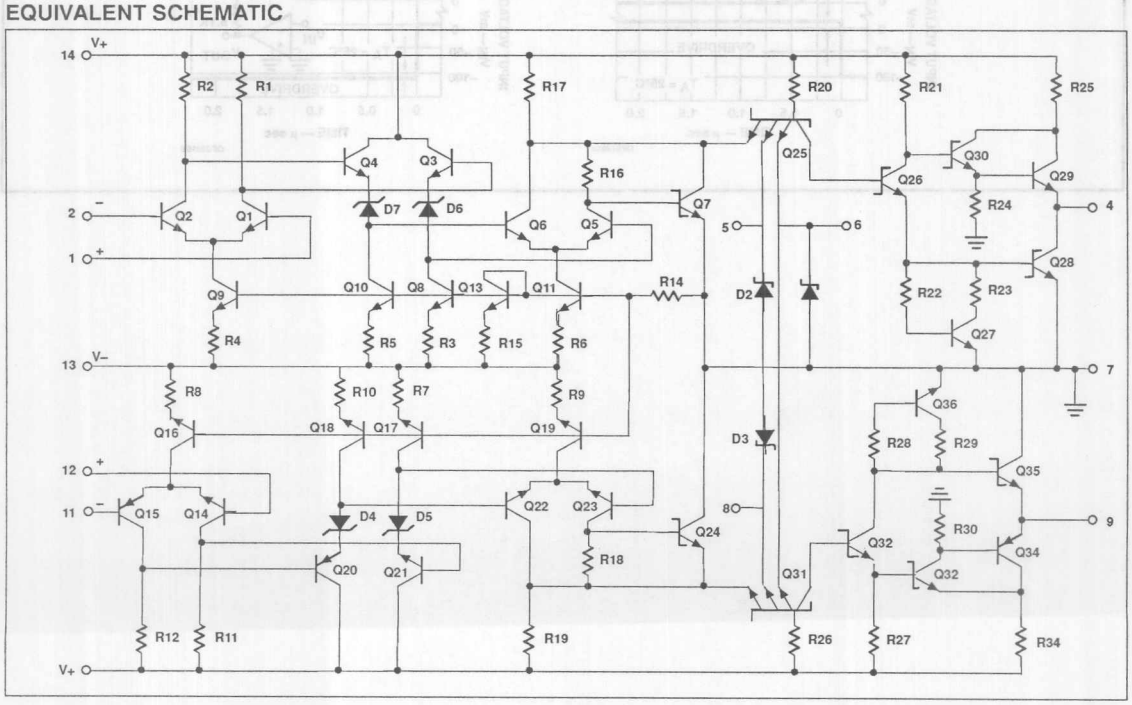
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE521N
14-Pin SO Package	0 to +70°C	NE521D
14-Pin Cerdip	0 to +70°C	NE521F
14-Pin Cerdip	-55°C to +125°C	SE521F

EQUIVALENT SCHEMATIC



LOGIC FUNCTIONS

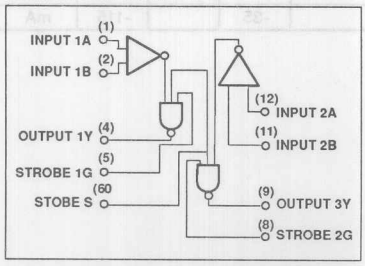
V_{ID} A^+, B^-	STROBE S	STROBE G	OUTPUT (Y)
$V_{ID} \leq -V_{OS}$	H	H	L
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined
$V_{ID} \geq V_{OS}$	H	H	H
X	L	X	H
X	X	L	H

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage		
V+	Positive	+7	V
V-	Negative	-7	V
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		
	Common mode	±5	V
	Strobe/gate	+5.25	V
P_D	Maximum power dissipation[1] T_A= 25°C (still-air)		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range		
	NE521	0 to 70	°C
	SE521	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	+300	°C

NOTES:
1. Derate above 25°C at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS (SE521)

V+=+5V, V-=-5V, TA=-55°C to +125°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+=+4.5V, V-=-4.5V				
	At 25°C			6	7.5	mV
	Over temperature range				15	
I_{BIAS}	Input bias current	V+=+5.5V, V-=-5.5V				
	At 25°C			7.5	20	µA
	Over temperature range				40	
I_{OS}	Input offset current	V+=+5.5V, V-=-5.5V				
	At 25°C			1.0	5	µA
	Over temperature range				12	
V_{CM}	Common-mode voltage range	V+=+4.5V, V-=-4.5V	–3		+3	V
V_{IL}	Low level input voltage					
	At 25°C				0.8	V
	Over temperature				0.7	
V_{IH}	High level input voltage		2.0			V
	Input current	V+=+5.5V, V-=-5.5V				
I_{IH}	High	V_{IH}=2.7V				
		1G or 2G strobe			50	µA
		Common strobe S			100	µA
	Input Current					
I_{IL}	Low	V_{IL}=0.5V				
		1G or 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage	$V_{I(S)}$=2.0V				
V_{OH}	High	V+=+4.5V, V-=-4.5V, I_{LOAD}=-1mA	2.5	3.4		V
V_{OL}	Low	V+=+4.5V, V-=-4.5V, I_{LOAD}=10mA			0.5	
		T_A=25°C, I_{LOAD}=20mA			0.5	
	Supply voltage					
V+	Positive		4.5	5.0	5.5	V
V-	Negative		-4.5	-5.0	-5.5	
	Supply current	V+=5.5V, V-=-5.5V, T_A=25°C				
I_{CC+}	Positive			27	35	mA
I_{CC-}	Negative			-15	-28	
I_{SC}	Short-circuit output current		-35		-115	mA

DC ELECTRICAL CHARACTERISTICS(NE521)

V+=+5V, V-=-5V, TA=0 to 70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+=+4.75V, V-=-4.75V				
	At 25°C			6	7.5	mV
	Over temperature range				10	
I_{BIAS}	Input bias current	V+=+5.25V, V-=-5.25V				
	At 25°C			7.5	20	µA
	Over temperature range				40	
I_{OS}	Input offset current	V+=+5.25V, V-=-5.25V				
	At 25°C			1.0	5	µA
	Over temperature range				12	
V_{CM}	Common-mode voltage range	V+=+4.75V, V-=-4.75V	–3		+3	V
	Input current	V+=+5.25V, V-=-5.25V				
I_{IH}	High	V_{IH}=2.7V				
		1G or 2G strobe			50	µA
		Common strobe S			100	µA
	Input Current					
I_{IL}	Low	V_{IL}=0.5V				
		1G or 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage	$V_{I(S)}$=2.0V				
V_{OH}	High	V+=+4.75V, V-=-4.75V, I_{LOAD}=-1mA	2.7	3.4		V
V_{OL}	Low	V+=+5.25V, V-=-5.25V, I_{LOAD}=20mA			0.5	
	Supply voltage					
V+	Positive		4.75	5.0	5.25	V
V-	Negative		-4.75	-5.0	-5.25	
	Supply current	V+=5.25V, V-=-5.25V, T_A=25°C				
I_{CC+}	Positive			27	35	mA
I_{CC-}	Negative			-15	-28	
I_{SC}	Short-circuit output current		-40		-100	mA

AC ELECTRICAL CHARACTERISTICS

T_A=25°C, R_L=280W C_L=15pF V+=5V V-=5V.

SYMBOL	PARAMETER	FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
Large-signal switching speed							
	Propagation delay						
$t_{PLH(D)}$	Low to high[1]	Amp	Output		8	12	
$t_{PHL(D)}$	High to low[1]	Amp	Output		6	9	ns
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		4.5	10	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		3.0	6	
f_{MAX}	Max. operating frequency			40	55		MHz

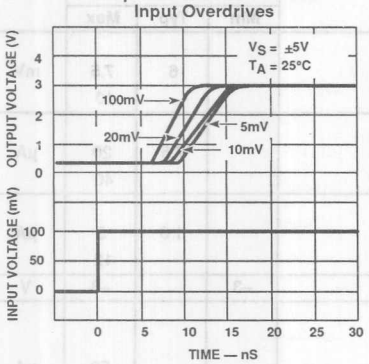
NOTES:

1. Response time measured from 0V point of ±100mV_{P-P} 10MHz square wave to the 1.5V point of the output.
2. Response time measured from 1.5V point of input to 1.5V point of the output.

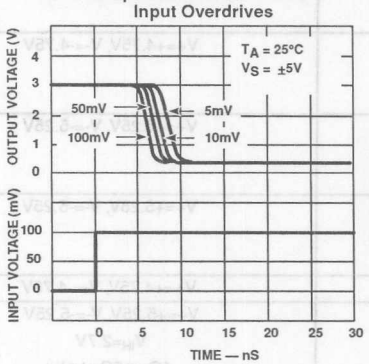
High-speed dual-differential comparator/sense amp NE/SE521

TYPICAL PERFORMANCE CHARACTERISTICS

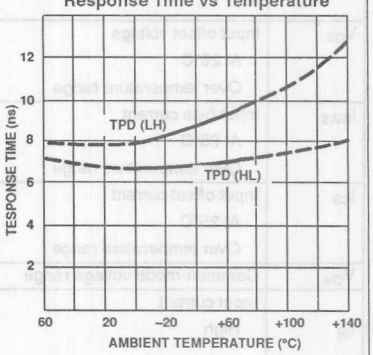
Response Time for Various Input Overdrives



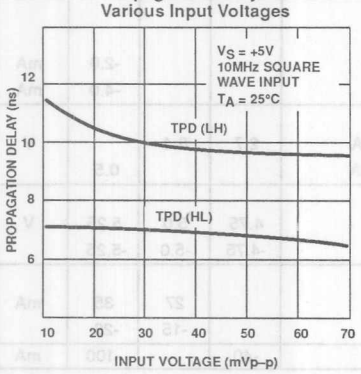
Response Time for Various Input Overdrives



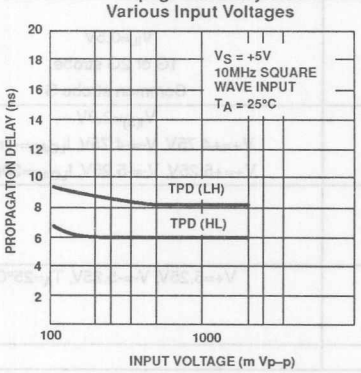
Response Time vs Temperature



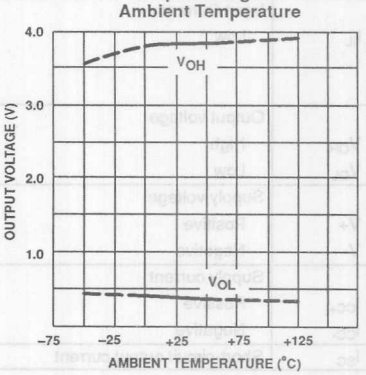
Propagation Delay for Various Input Voltages



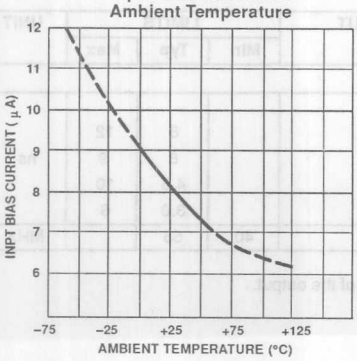
Propagation Delay for Various Input Voltages



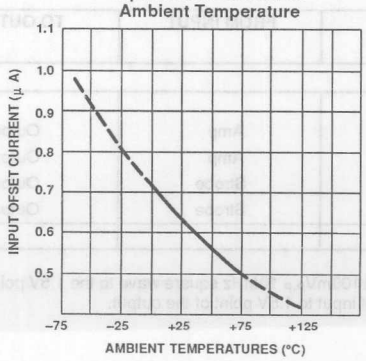
Output Voltage vs Ambient Temperature



Input Bias Current vs Ambient Temperature



Input Offset Current vs Ambient Temperature



High-speed dual-differential comparator/sense amp NE522

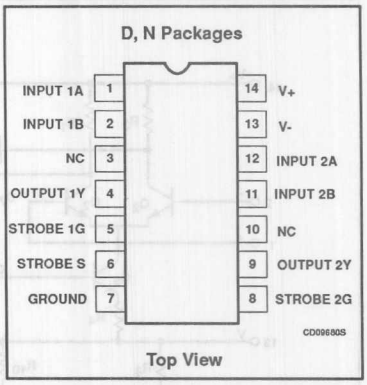
FEATURES

- 15ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- TTL-compatible strobes and outputs
- Large common-mode input voltage range
- Operates from standard supply voltages

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High-speed line receiver

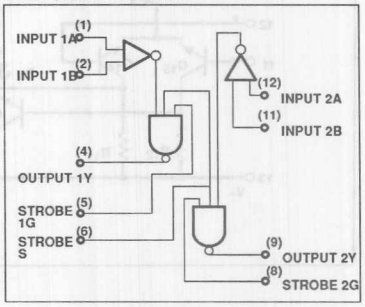
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE522N
14-Pin Plastic SO	0 to +70°C	NE522D

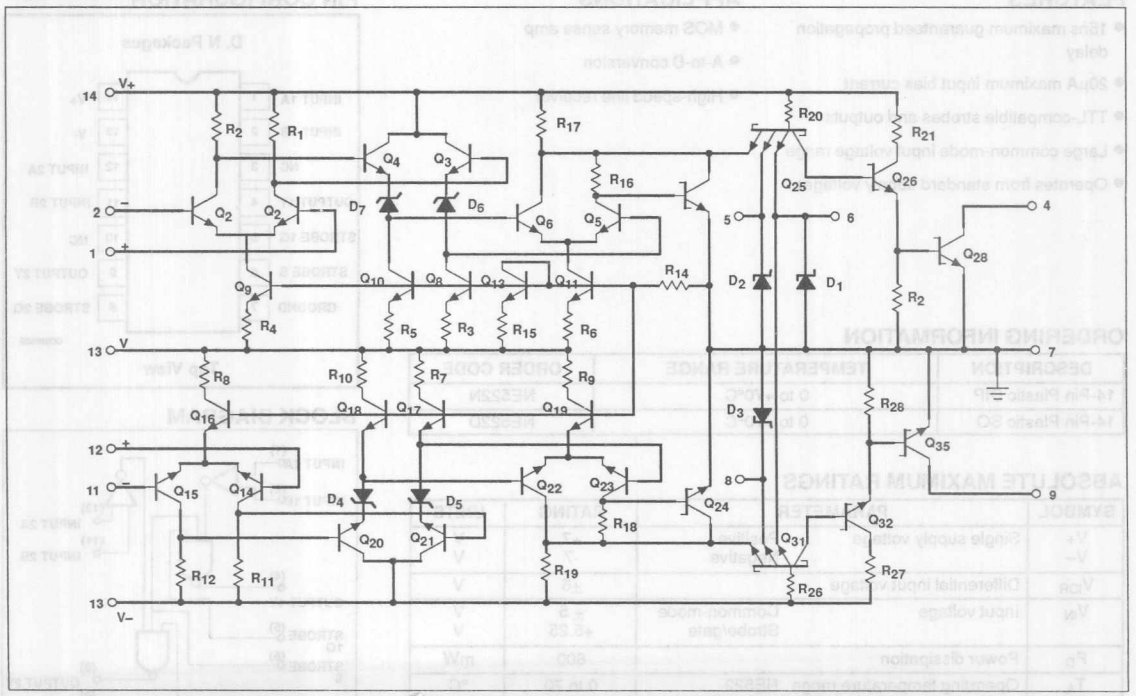
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V+ V–	Single supply voltage	Positive Negative	+7 -7	V V
V_{IDR}	Differential input voltage		±6	V
V_{IN}	Input voltage	Common-mode Strobe/gate	± 5 +5.25	V V
P_D	Power dissipation		600	mW
T_A	Operating temperature range	NE522	0 to 70	°C
T_{STG}	Storage temperature range		-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)		+300	°C

EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

(NE522) +5V ±5%, T_A = 0 to +70°C, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{OS}	Input offset voltage	V+ = +4.75V, V– = –4.75V				
	At 25°C			6	7.5	mV
	Over temperature range				10	
I_{BIAS}	Input bias current	V+ = +5.25V, V– = –5.25V				
	At 25°C			7.5	20	µA
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.25V, V– = –5.25V				
	At 25°C			1.0	5	µA
	Over temperature range				12	
V_{CM}	Common-mode voltage range	V+ = +4.75V, V– = –4.75V	–3		+3	V
V_{IL}	Low level input					
	At 25°C				0.8	V
	Over temperature range				0.7	
V_{IH}	High level temperature		2.0			V
I_{IH}	Input current	V+ = +5.25V, V– = –5.25V				
	High	V_{IH} = 2.7V			50	µA
		1G or 2G strobe			100	µA
		Common strobe S				
I_{IL}	Low input current	V_{IL} = 0.5V				
		1G or 2G strobe			–2.0	mA
		Common strobe S			–4.0	mA
V_{OL}	Output voltage Low	V+ = +5.25V, V– = –5.25V, $V_{I(S)}$ = 2.0V, I_{LOAD} = 20mA			0.5	V
I_{OH}	Output current High	V_{CC+} = +4.75V, V_{CC-} = –4.75V, V_{OH} = 5.25V			250	µA
	Supply voltage					
V+	Positive		4.75	5.0	5.25	V
V–	Negative		–4.75	–5.0	–5.25	
	Supply current	V+ = +5.25V, V– = –5.25V, T_A = 25°C				
I_{CC+}	Postiive			27	35	mA
I_{CC-}	Negative			–15	–28	

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, R_L = 280Ω, C_L = 15pF, unless otherwise stated.

SYMBOL	PARAMETER	FROM INPUT	TO OUTPUT	LIMITS			UNITS
				MIN	TYP	MAX	
I_R	Input resistance				4		kΩ
I_C	Input capacitance				3		pF
Large-signal switching speed							
	Propagation delay						
$t_{PLH(D)}$	Low to high[1]	Amp	Output		10	15	
$t_{PHL(D)}$	High to low[1]	Amp	Output		8	12	ns
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		6	13	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		5	9	
I_{MAX}	Maximum operating frequency			25	35		MHz

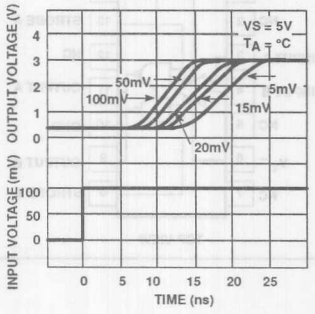
NOTES:
1. Response time measured from 0V point of +100mV_{P-P} 10MHz square wave to the 1.5V point of the output.
2. Response time measured from 1.5V point of the input to 1.5V point of the output.

LOGIC FUNCTION TABLE

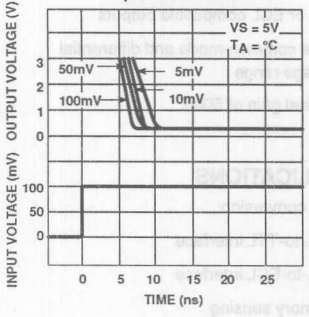
V_{ID} (A^+, B^-)	STRS	STRG	OUTPUT TRANSLATOR
$< -V_{OS}$	H	H	ON
$< -V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined
$> V_{OS}$	H	H	OFF
X	L	X	OFF
X	X	L	OFF

EQUIVALENT SCHEMATIC

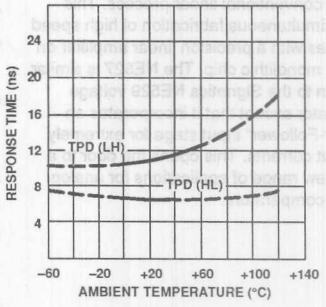
Response Time for Various Input Overdrives



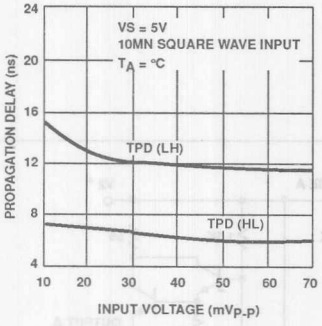
Response Time for Various Input Overdrives



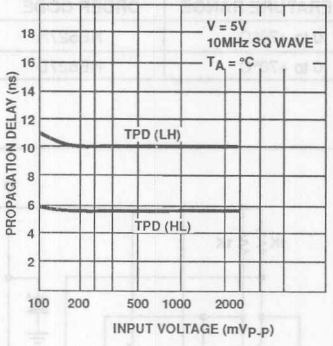
Response Time vs Temperature



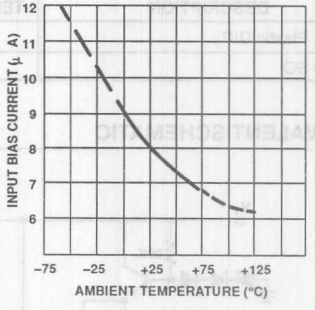
Propagation Delay for Various Input Voltages



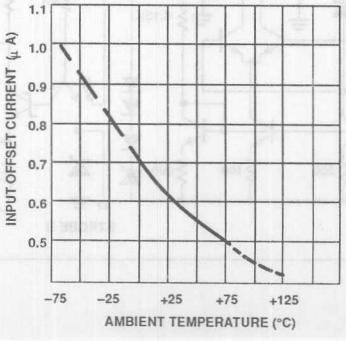
Propagation Delay for Various Input Voltages



Input Bias Current vs Ambient Temperature



Input Offset Current vs Ambient Temperature



Voltage comparator NE527

DESCRIPTION

The NE527 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed TTL gates with a precision linear amplifier on a single monolithic chip. The NE527 is similar in design to the Signetics NE529 voltage comparator except that it incorporates an "Emitter-Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

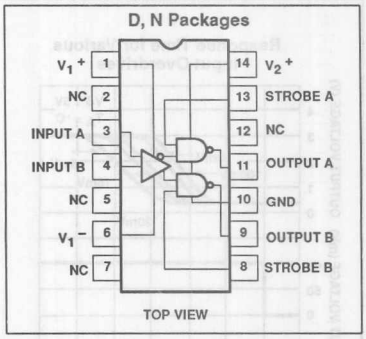
FEATURES

- 15ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common-mode and differential voltage range
- Typical gain of 5000

APPLICATIONS

- A/D conversion
- ECL-to-TTL interface
- TTL-to-ECL interface
- Memory sensing
- Optical data coupling

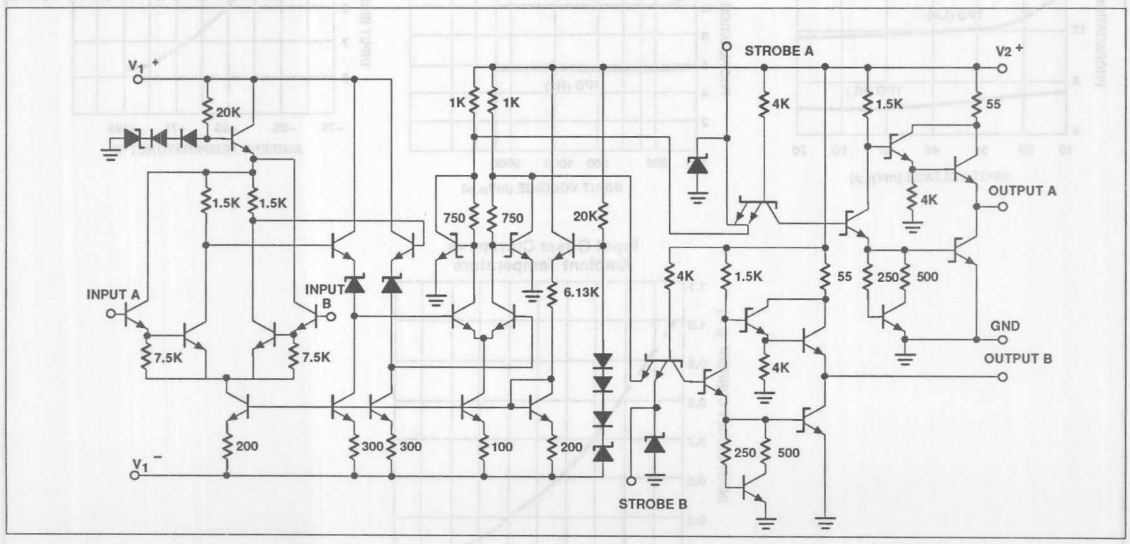
PIN CONFIGURATIONS



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE527N
14-Pin SO	0 to +70°C	NE527D

EQUIVALENT SCHEMATIC

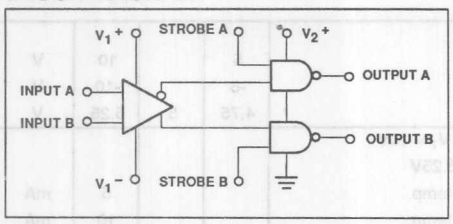


ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_1+	Positive supply voltage	+15	V
V_1-	Negative supply voltage	-15	V
V_2+	Gate supply voltage	+7	V
V_{OUT}	Output voltage	+7	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Input common mode voltage	±6	V
P_D	Max power dissipation[1] 25°C ambient (still air)		
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range		
	NE527	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:
1. Derate above 25°C, at the following rates:
   F package 9.5mW/°C
   N package 11.4mW/°C
   D package 8.3mW/°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V1+=10V, V1-=-10V, V2+=+5.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE527			UNIT
			Min	Typ	Max	
Input characteristics						
V_{OS}	Input offset voltage @ 25°C				6	mV
	over temperature range				10	mV
I_{BIAS}	Input bias current @ 25°C				2	µA
	over temperature range				4	µA
I_{OS}	Input offset current @ 25°C				0.75	µA
	over temperature range	V_{IN}=0V			1	µA
	common-mode voltage range				±5	V
Gate characteristics						
V_{OUT}	Output Voltage					
	"1" State	V_2+=4.75V, I_{SOURCE}=-1mA	2.7	3.3		V
	"0" State	V_2+=4.75V, I_{SINK}=10mA			0.5	V
	Strobe inputs					
	"0" Input current[1]	V_2+=5.25V, V_{STROBE}=0.5V			-2	mA
	"1" Input current @ 25°C[1]	V_2+=5.25V, V_{STROBE}=2.7V			100	µA
	Over temperature range	V_2+=5.25V, V_{STROBE}=2.7V			200	µA
	"0" Input voltage	V_2+=4.75V			0.8	V
	"1" Input voltage	V_2+=4.75V	2.0			V
I_{SC}	Short-circuit output current	V_2+=5.25V, V_{OUT}=0V	-18		-70	mA
Power supply requirements						
	Supply voltage					
V_1+			5		10	V
V_1-			-6		-10	V
V_2+			4.75	5	5.25	V
	Supply current	V_1+=10V, V_1-=-10V				
		V_2+=5.25V				
I_1+		Over temp.			5	mA
I_1-		Over temp.			10	mA
I_2+		Over temp.			20	mA

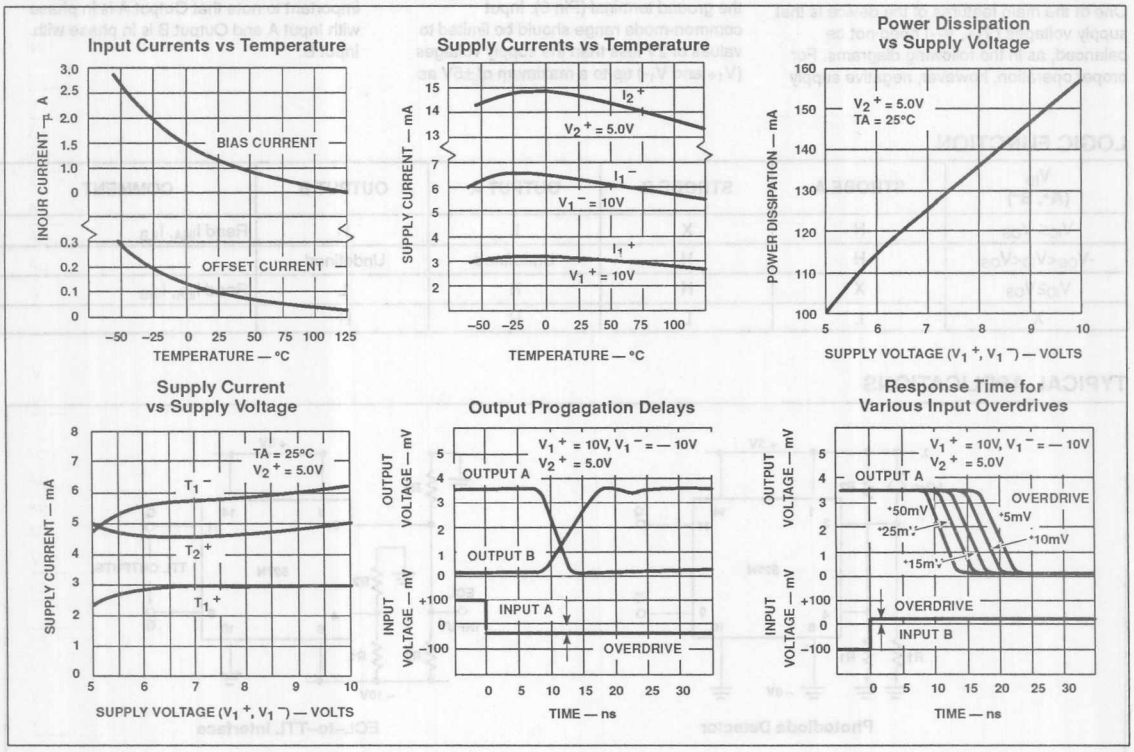
NOTES:
1. See Logic Function Table.

AC ELECTRICAL CHARACTERISTICS

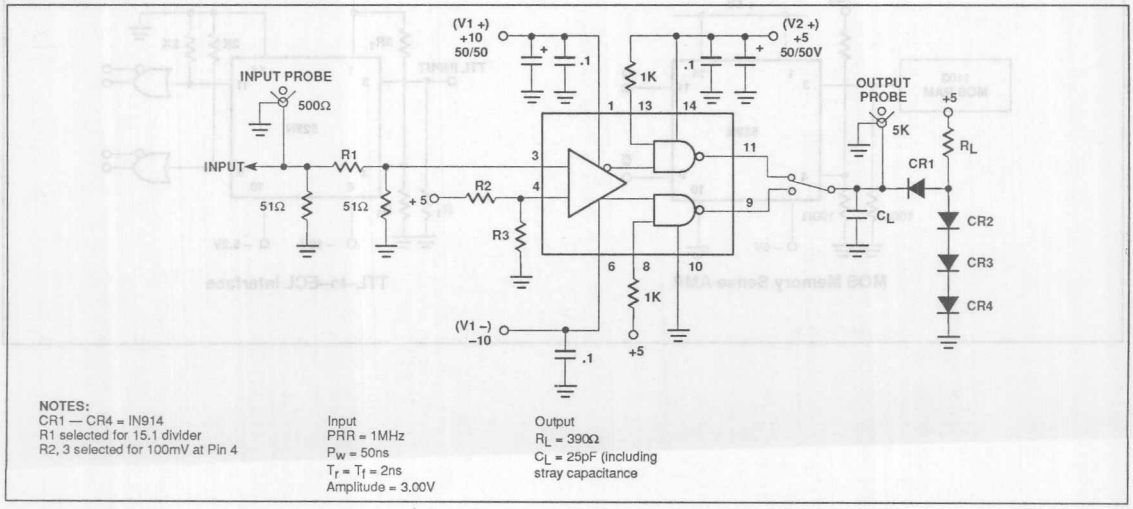
T_A=25°C, unless otherwise specified. (See AC test circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Transient response propagation delay time					
t_{PLH}	Low-to-High	V_{IN}=±100mV step		16	26	ns
t_{PHL}	High-to-Low			14	24	ns
	Delay between output A and B			2	5	ns
	Strobe delay time					
t_{ON}	Turn-on time			6		ns
t_{OFF}	Turn-off time			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS



RESPONSE TIME TEST CIRCUIT



NOTES:
CR1 — CR4 = IN914
R1 selected for 15.1 divider
R2, 3 selected for 100mV at Pin 4

Input
PRR = 1MHz
P_W = 50ns
$T_r = T_f$ = 2ns
Amplitude = 3.00V

Output
R_L = 390Ω
C_L = 25pF (including stray capacitance

Voltage comparator NE527

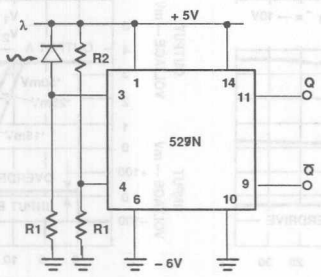
APPLICATIONS

One of the main features of the device is that supply voltages (V_1+, V_1-) need not be balanced, as in the following diagrams. For proper operation, however, negative supply (V_1-) should always be at least 6V more than the ground terminal (Pin 6). Input common-mode range should be limited to values of 2V less than the supply voltages (V_1+ and V_1-) up to a maximum of ±5V as supply voltages are increased. It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

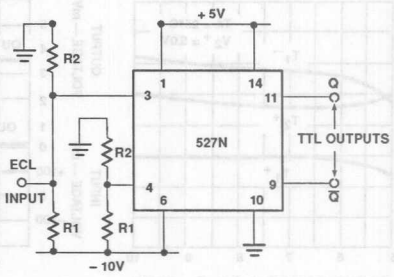
LOGIC FUNCTION

V_{ID} (A^+, B^-)	STROBE A	STROBE B	OUTPUT A	OUTPUT B	COMMENT
$V_{ID} \leq -V_{OS}$	H	X	L	H	Read I_{IHA}, I_{ILB}
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined	Undefined	
$V_{ID} \geq V_{OS}$	X	H	H	L	Read I_{ILA}, I_{IHB}
X	L	L	H	H	

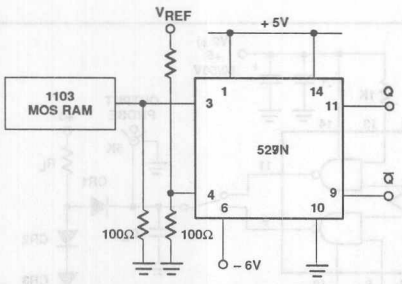
TYPICAL APPLICATIONS



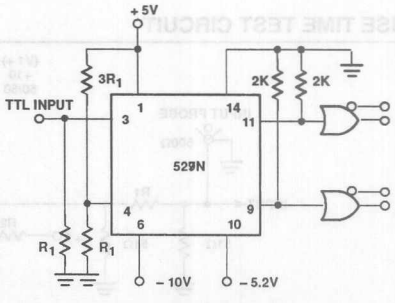
Photodiode Detector



ECL–to–TTL Interface



MOS Memory Sense AMP



TTL–to–ECL Interface

Voltage comparator — NE529

DESCRIPTION

The NE529 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high-speed TTL gates with a precision linear amplifier on a single monolithic chip.

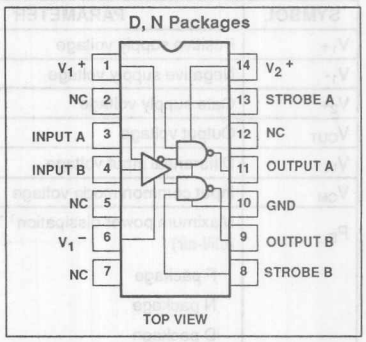
FEATURES

- 10ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common-mode and differential voltage range
- Typical gain 5000

APPLICATIONS

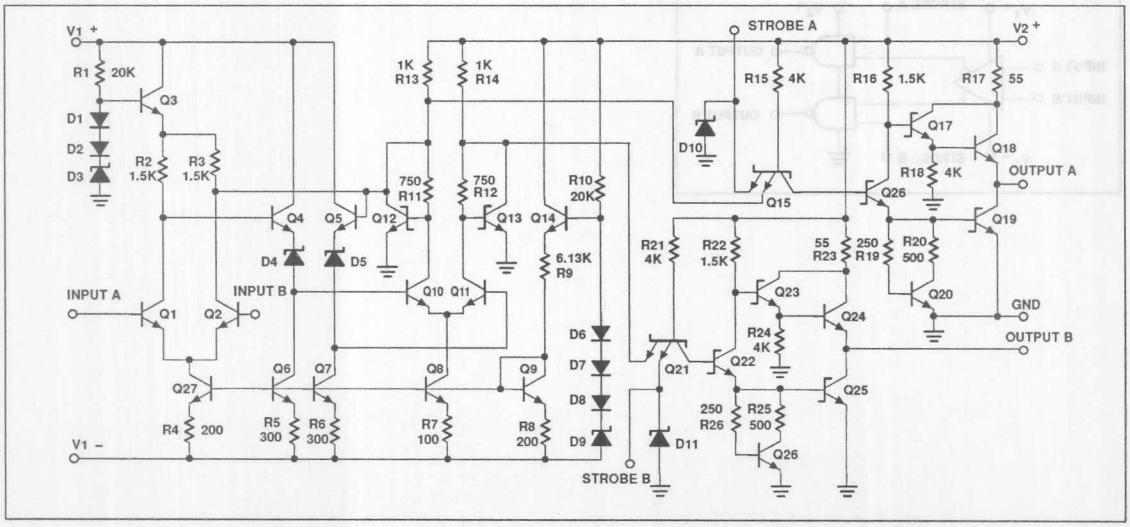
- A/D conversion
- ECL-to-TTL interface
- TTL-to-ECL interface
- Memory sensing
- Optical data coupling

PIN CONFIGURATIONS



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE529N
14-Pin SO	0 to +70°C	NE529D

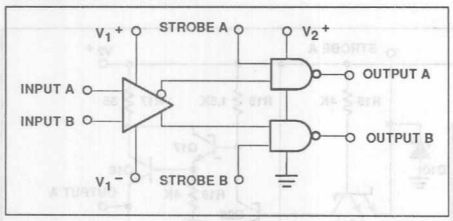


ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_1+	Positive supply voltage	+15	V
V_1-	Negative supply voltage	-15	V
V_2+	Gate supply voltage	+7	V
V_{OUT}	Output voltage	+7	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Input common mode voltage	±6	V
P_D	Maximum power dissipation[1] T_A=25°C (still-air)		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec max)	+300	°C

NOTES:
1. Derate above 25°C at the following rates:
   N package at 11.5mW/°C
   D package at 8.3mW/°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_1+=+10V, V_2+=+5.0V, V_1-=-10V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE529			UNIT
			Min	Typ	Max	
Input characteristics						
V_{OS}	Input offset voltage @ 25°C				6	mV
	Over temperature range				10	mV
I_{BIAS}	Input bias current @ 25°C			5	20	µA
	Over temperature range	V_{IN}=0V			50	µA
I_{OS}	Input offset current @ 25°C			2	5	µA
	Over temperature range	V_{IN}=0V			15	µA
	Common-mode voltage range			0	±5	V
Gate characteristics						
V_{OUT}	Output voltage					
	"1" state	V_2+=4.75V, I_{SOURCE}=-1mA	2.7	3.3		V
	"0" state	V_2+=4.75V, I_{SINK}=10mA			0.5	V
	Strobe inputs					
	"0" Input current[1]	V_2+=5.25V, V_{STROBE}=0.5V			-2	mA
	"1" Input current @ 25°C[1]	V_2+=5.25V, V_{STROBE}=2.7V			100	µA
	Over temperature range	V_2+=5.25V, V_{STROBE}=2.7V			200	µA
	"0" input voltage	V_2+=4.75V			0.8	V
	"1" input voltage	V_2+=4.75V	2.0			V
I_{SC}	Short-circuit output current	V_2+=5.25V, V_{OUT}=0V	-18		-70	mA
Power supply requirements						
	Supply voltage					
V_1+			5		10	V
V_1-			-6		-10	V
V_2+			4.75	5	5.25	V
	Supply current	V_1+=10V, V_1-=-10V				
		V_2+=5.25V				
I_1+		Over temp.			5	mA
I_1-		Over temp.			10	mA
I_2+		Over temp.			20	mA

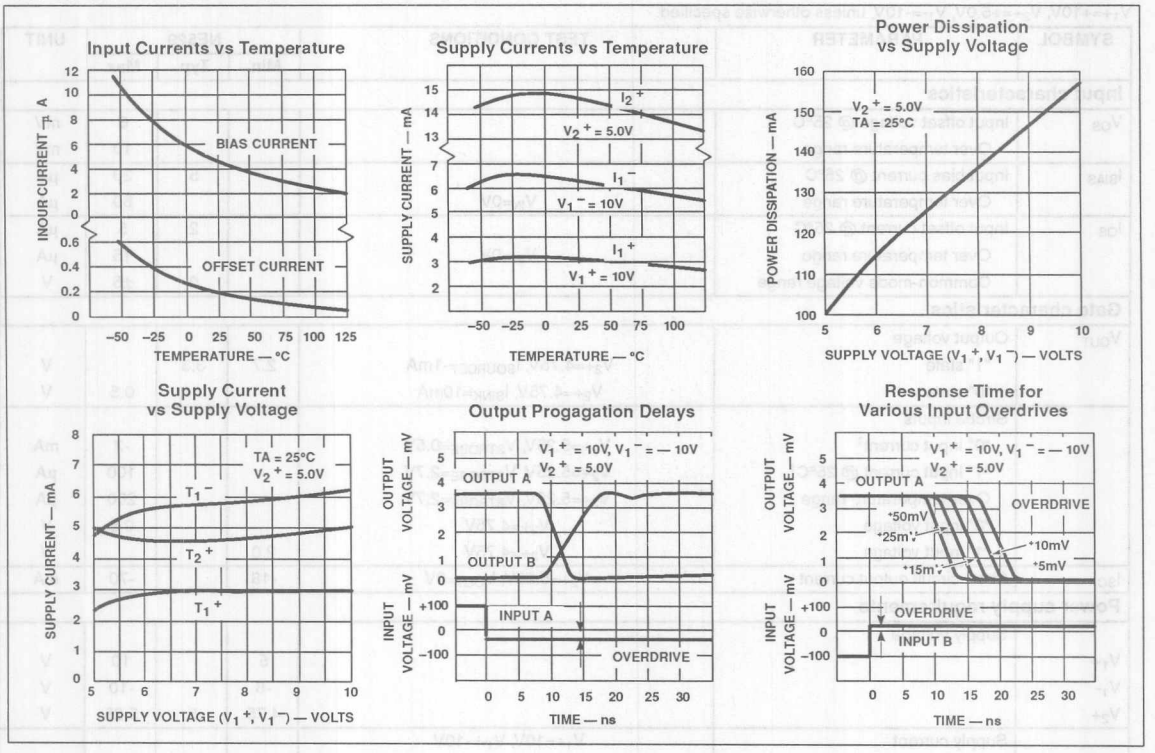
NOTES:
1. See logic function table.

AC ELECTRICAL CHARACTERISTICS

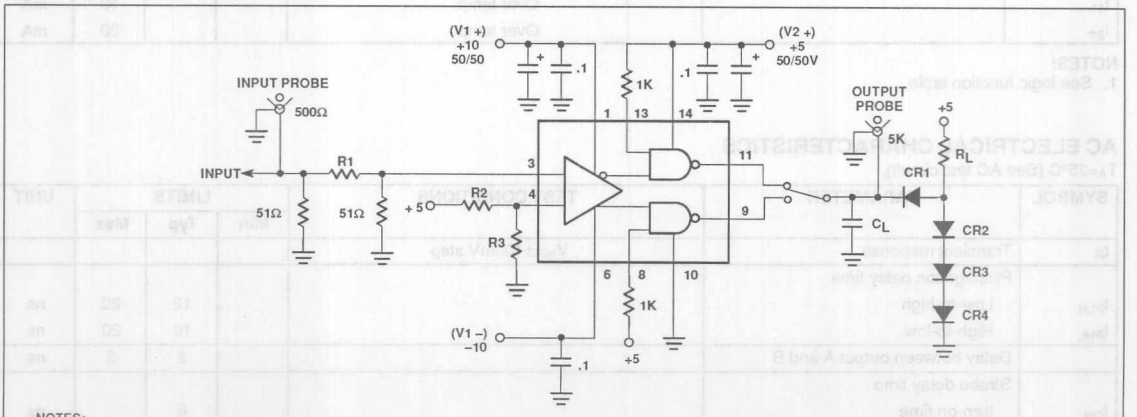
T_A=25°C (See AC test circuit).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_R	Transient response	V_{IN}=±100mV step				
	Propagation delay time					
t_{PLH}	Low-to-high			12	22	ns
t_{PHL}	High-to-low			10	20	ns
	Delay between output A and B			2	5	ns
	Strobe delay time					
t_{ON}	turn-on time			6		ns
t_{OFF}	turn-off time			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS



RESPONSE TIME TEST CIRCUIT



NOTES:
CR1 — CR4 = IN914
R1 selected for 15.1 divider
R2, 3 selected for 100mV at Pin 4

Input
PRR = 1MHz
P_W = 50ns
$T_r = T_f$ = 2ns
Amplitude = 3.00V

Output
R_L = 390Ω
C_L = 25pF (including stray capacitance

APPLICATIONS

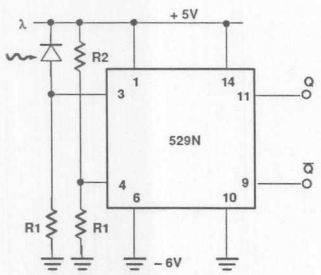
One of the main features of the device is that supply voltages (V+, V-) need not be balanced, as in the following diagrams. For proper operation, however, negative supply (V-) should always be at least 6V more than the ground terminal (pin 6). Input Common-Mode range should be limited to values of 2V less than the supply voltages (V+ and V-) up to a maximum of ±6V as supply voltages are increased.

It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

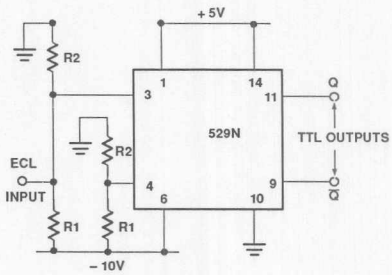
LOGIC FUNCTION

V_{ID} (A^+, B^-)	STROBE A	STROBE B	OUTPUT A	OUTPUT B
$V_{ID} \leq -V_{OS}$	H	X	L	H
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined	Undefined
$V_{ID} \geq V_{OS}$	X	H	H	L
X	L	L	H	H

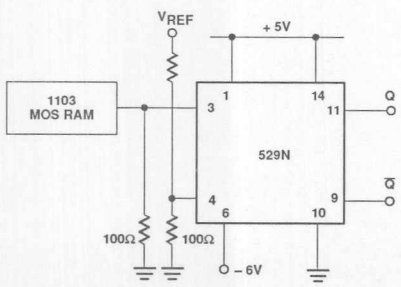
TYPICAL APPLICATIONS



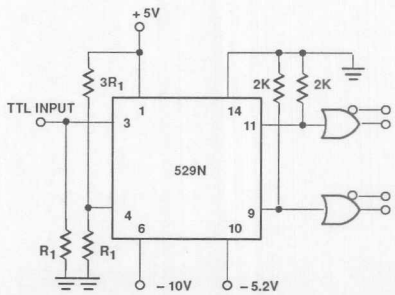
Photodiode Detector



ECL–to–TTL Interface



MOS Memory Sense AMP



TTL–to–ECL Interface

Section 4
Timers

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Philips Semiconductors-Signetics

Section 4
Timers

General Purpose/Linear ICs

General purpose CMOS timer — ICM7555

DESCRIPTION

The ICM7555 is a CMOS timer providing significantly improved performance over the standard NE/SE555 timer, while at the same time being a direct replacement for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, TRIGGER, and RESET currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

The ICM7555 is a stable controller capable of producing accurate time delays or frequencies.

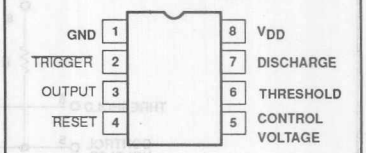
In the one-shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the bipolar 555 device, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The TRIGGER and RESET inputs are active low. The output inverter can source or sink currents large enough to drive TTL loads or provide minimal offsets to drive CMOS loads.

FEATURES

- Exact equivalent in most applications for NE/SE555
- Low supply current: 80µA (typ)
- Extremely low trigger, threshold, and reset currents: 20pA (typ)
- High-speed operation: 500kHz guaranteed
- Wide operating supply voltage range guaranteed 3 to 16V over full automotive temperatures
- Normal reset function; no crowbarring of supply during output transition
- Can be used with higher-impedance timing elements than the bipolar 555 for longer time constants
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- High output source/sink driver can drive TTL/CMOS
- Typical temperature stability of 0.005%/°C at 25°C
- Rail-to-rail outputs

PIN CONFIGURATION

D and N Packages



CD12800S

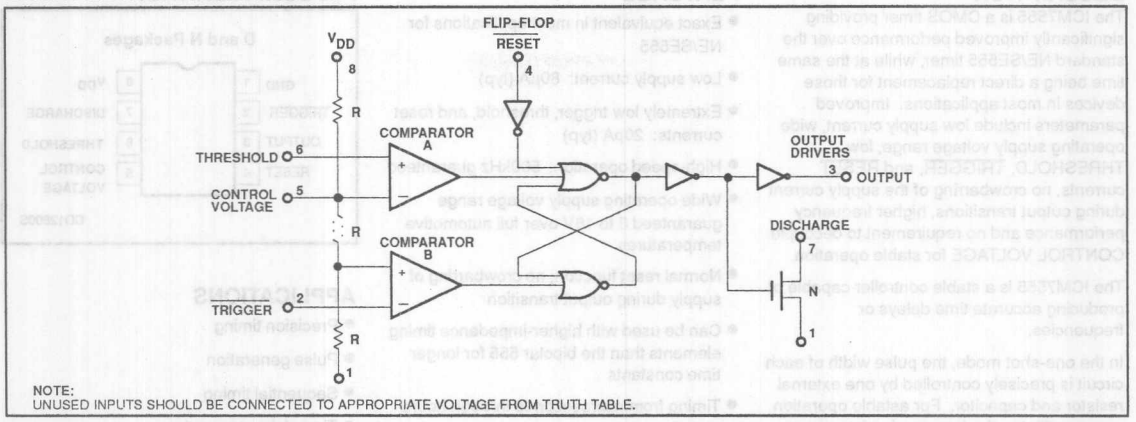
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	ICM7555CN
8-Pin Plastic SO	0 to +70°C	ICM7555CD
8-Pin Plastic DIP	-40 to +85°C	ICM7555IN
8-Pin Plastic SO	-40 to +85°C	ICM7555ID

EQUIVALENT BLOCK DIAGRAM



NOTE:
UNUSED INPUTS SHOULD BE CONNECTED TO APPROPRIATE VOLTAGE FROM TRUTH TABLE.

TRUTH TABLE

THRESHOLD VOLTAGE	TRIGGER VOLTAGE	RESET[1]	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
>2/3(V+)	> 1/3(V+)	HIGH	LOW	ON
V_{TH} < 2/3	V_{TR} > 1/3	HIGH	STABLE	STABLE
DON'T CARE	<1/3(V+)	HIGH	HIGH	OFF

NOTES:
1. RESET will dominate all other inputs: TRIGGER will dominate over THRESHOLD.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	+18	V
V_{TRIG}[1]	Trigger innput voltage		
V_{CV}	Control voltage	> -0.3 to	
V_{TH}	Threshold input voltage	<V_{DD} + 0.3	V
V_{RST}	RESET input voltage		
I_{OUT}	Output current	100	mA
P_{DMAX}	Maximum power dissipation, T_A = 25°C (still air)[2]		
	N package	1160	mW
	D package	780	mW
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead temperature (Soldering 60s)	300	°C

NOTES:
1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} + 0.3V or less than GND -0.3V may cause destructive latch-up. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555 must be turned on first.
2. Derate above 25°C, at the following rates:
   N package at 9.3mW/°C
   D package at 6.2mW/°C
3. See "Power Dissipation Considerations" section.

DC AND AC ELECTRICAL CHARACTERISTICS

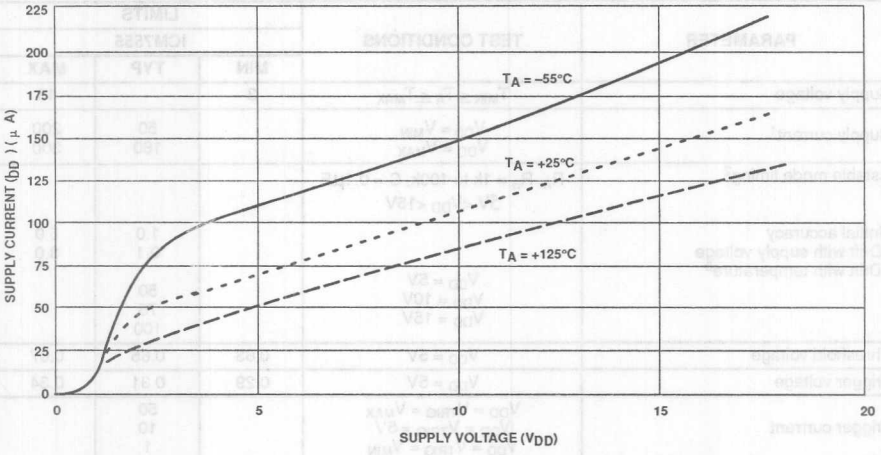
T_A = 25°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			ICM7555			
			MIN	TYP	MAX	
V_{DD}	Supply voltage	$T_{MIN} \le T_A \le T_{MAX}$	3		16	V
I_{DD}	Supply current[1]	$V_{DD} = V_{MIN}$ $V_{DD} = V_{MAX}$		50 180	200 300	µA µA
	Astable mode timing[2] 5V <V_{DD} <15V	R_A, R_B = 1k to 100k, C = 0.1µF				
	Initial accuracy			1.0	5.0	%
	Drift with supply voltage			0.1	3.0	%/V
	Drift with temperature[3]	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		50 75 100		ppm/°C ppm/°C ppm/°C
V_{TH}	Threshold voltage	V_{DD} = 5V	0.63	0.65	0.67	xV_{DD}
V_{TRIG}	Trigger voltage	V_{DD} = 5V	0.29	0.31	0.34	xV_{DD}
I_{TRIG}	Trigger currrent	$V_{DD} = V_{TRIG} = V_{MAX}$ $V_{DD} = V_{TRIG}$ = 5V $V_{DD} = V_{TRIG} = V_{MIN}$		50 10 1		pA pA pA
I_{TH}	Threshold current	$V_{DD} = V_{TH} = V_{MAX}$ $V_{DD} = V_{TH}$ = 5V $V_{DD} = V_{TH} = V_{MIN}$		50 10 1		pA pA pA
I_{RST}	Reset current	$V_{DD} = V_{RST} = V_{MAX}$ $V_{DD} = V_{RST}$ = 5V $V_{DD} = V_{RST} = V_{MIN}$		100 20 2		pA pA pA
V_{RST}	Reset voltage	$V_{DD} = V_{MIN}$ and V_{MAX}	0.4	0.7	1.0	V
V_{CV}	Control voltage	V_{DD} = 5V	0.62	0.65	0.67	xV_{DD}
V_{OL}	Output voltage (low)	$V_{DD} = V_{MAX}$, I_{SINK} = 3.2mA V_{DD} = 5V, I_{SINK} = 3.2mA		0.1 0.2	0.4 0.4	V V
V_{OH}	Output voltage (high)	$V_{DD} = V_{MAX}$, I_{SOURCE} = -1.0mA V_{DD} = 5V, I_{SOURCE} = -1.0mA	15.25 4.0	15.7 4.5		V_{DD} V_{DD}
V_{DIS}	Discharge output voltage	V_{DD} = 5V, I_{DIS} = 10.0mA		0.2	0.4	V
t_R	Rise time of output[3]	R_L = 10MΩ, C_L = 10pF, V_{DD} = 5V		45	75	ns
t_F	Fall time of output[3]	R_L = 10MΩ, C_L = 10pF, V_{DD} = 5V		20	75	ns
F_{MAX}	Maximum oscillator frequency (astable mode)		500			kHz

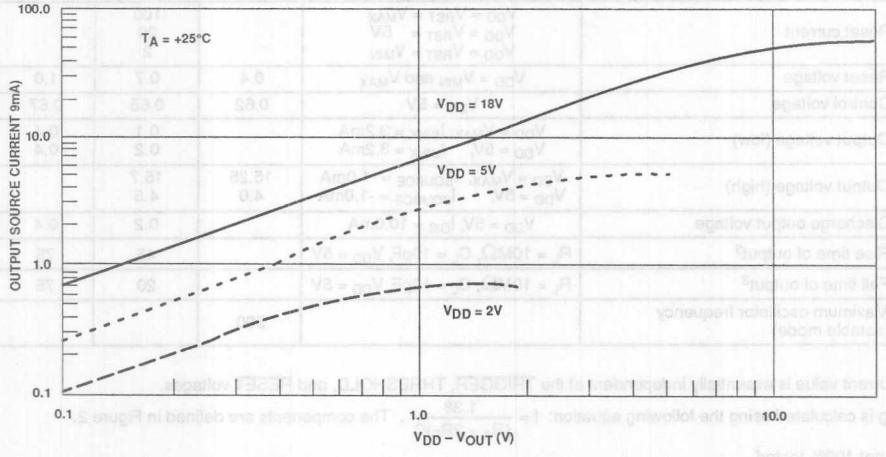
NOTES:

1. The supply current value is essentially independent of the $\overline{\text{TRIGGER}}$, THRESHOLD, and $\overline{\text{RESET}}$ voltages.
2. Astable timing is calculated using the following equation: $f = \frac{1.38}{(R_A + 2R_B)C}$. The components are defined in Figure 2.
3. Parameter is not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

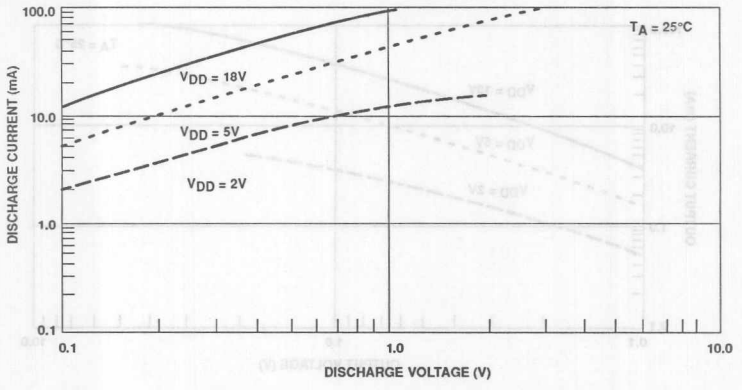


Supply Current vs Supply Voltage

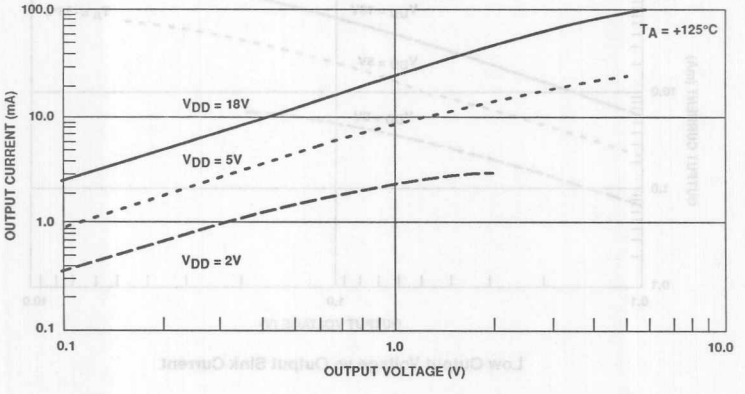


High Output Voltage Drop vs Output Source Current

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

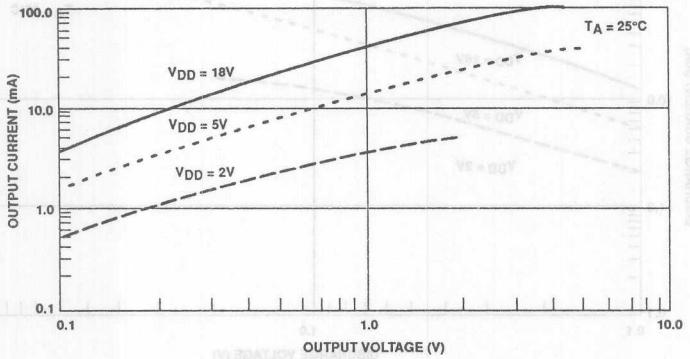


Discharge Low Output Voltage vs Discharge Sink Current

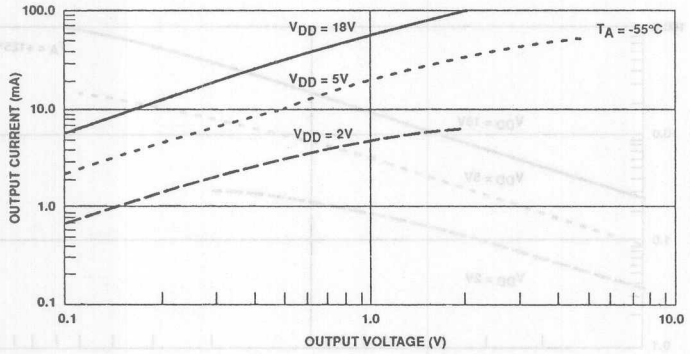


Low Output Voltage vs Output Sink Current

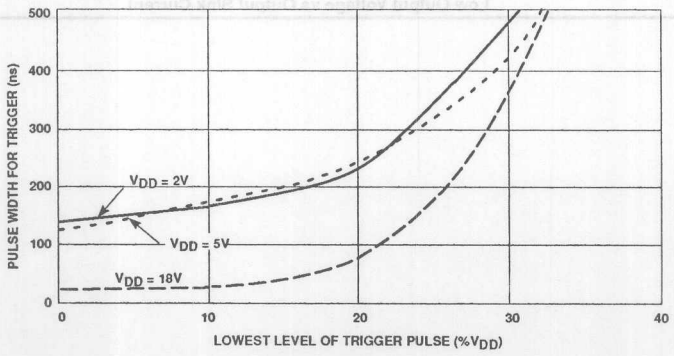
TYPICAL PERFORMANCE CHARACTERISTICS (continued)



Low Output Voltage vs Output Sink Current

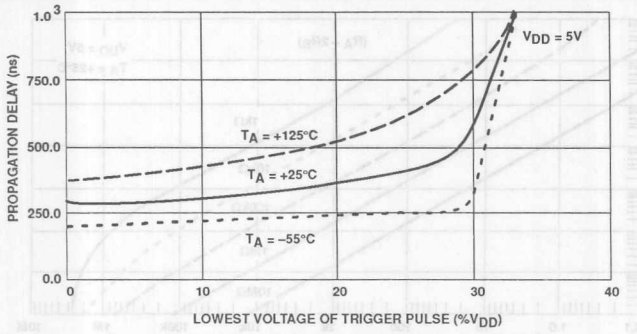


Low Output Voltage vs Output Sink Current

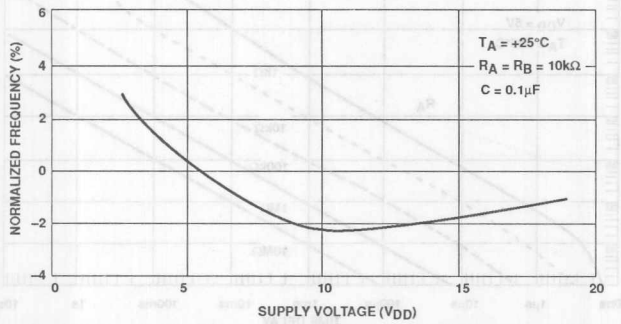


Minimum Pulse Width for Triggering

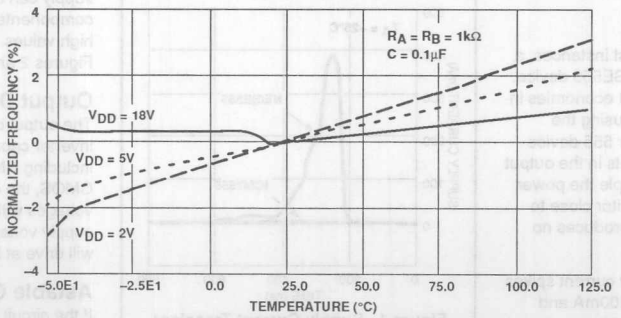
TYPICAL PERFORMANCE CHARACTERISTICS (continued)



Propagation Delay vs Voltage Level of Trigger Pulse

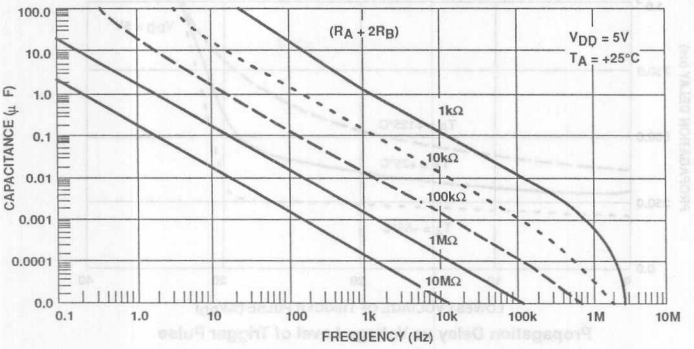


Normalized Frequency Stability as a Function of Supply Voltage (Astable Mode)

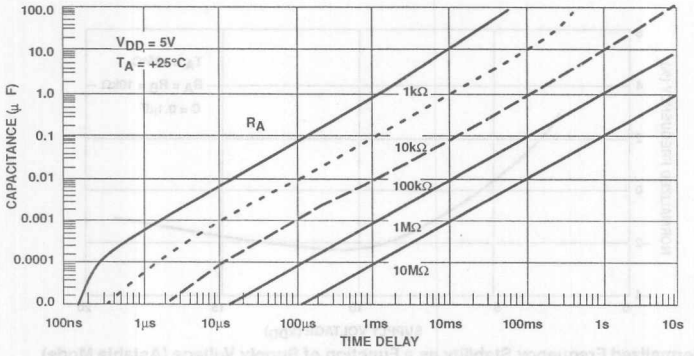


Normalized Frequency Stability as a Function of Temperature (Astable Mode)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)



Free-Running Frequency as a Function of R_A, R_B, and C



Monostable Time Delay vs R_A and C

APPLICATION NOTES

General

The ICM7555 device is, in most instances, a direct replacement for the NE/SE555 device. However, it is possible to effect economies in the external component count using the ICM7555. Because the bipolar 555 device produces large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555 device produces no such transients. See Figure 1.

The ICM7555 produces supply current spikes of only 2-3mA instead of 300-400mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications, 2 capacitors can be saved using an ICM7555.

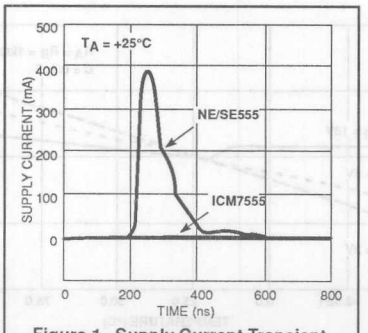


Figure 1. Supply Current Transient Compared With a Standard Bipolar 555 During an Output Transition

Power Supply Considerations

Although the supply current consumed by the ICM7555 device is very low, the total system supply can be high unless the timing components are high impedance. Therefore, high values for R and low values for C in Figures 2 and 3 are recommended.

Output Drive Capability

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5V or more, the ICM7555 will drive at least 2 standard TTL loads.

Astable Operation

If the circuit is connected as shown in Figure 2, it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus, the duty cycle (D) may be precisely set by the ratio of these two resistors. In this mode of operation, the

capacitor charges and discharges between 1/3 V_{DD} and 2/3 V_{DD}. Since the charge rate and the threshold levels are directly proportional to the supply voltage, the frequency of oscillation is independent of the supply voltage.

$$F = \frac{1.38}{(R_A + 2R_B)\,C} \qquad D = \frac{R_A + R_B}{R_A + 2R_B}$$

Monostable Operation

In this mode of operation, the timer functions as a one-shot. Initially, the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative pulse to Pin 2, $\overline{\text{TRIGGER}}$, the internal flip-flop is set which releases the low impedance on DISCHARGE; the external capacitor charges and drives the OUTPUT High. The voltage across the capacitor increases exponentially with a time constant $t = R_AC$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip-flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state.

Control Voltage

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode, or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555, i.e., 0.6 to 0.7V. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard bipolar 555 in that it controls only the internal flip-flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

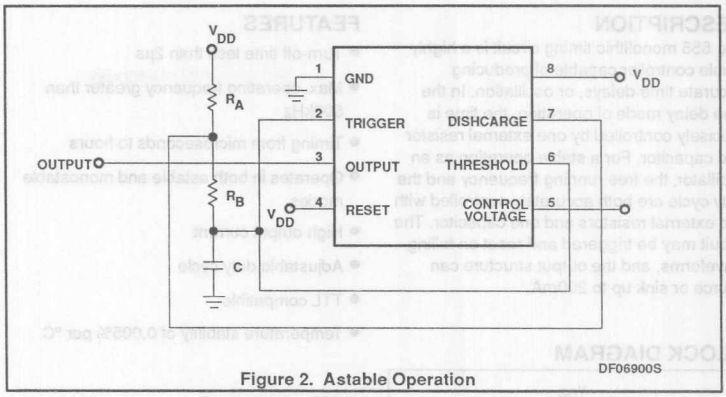


Figure 2. Astable Operation

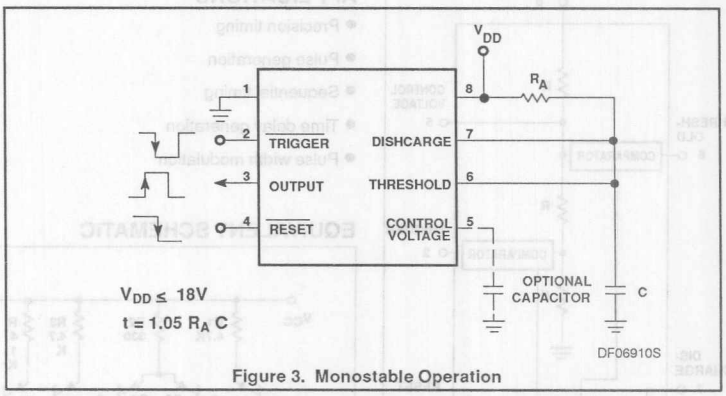


Figure 3. Monostable Operation

Timer — NE/SA/SE555/SE555C

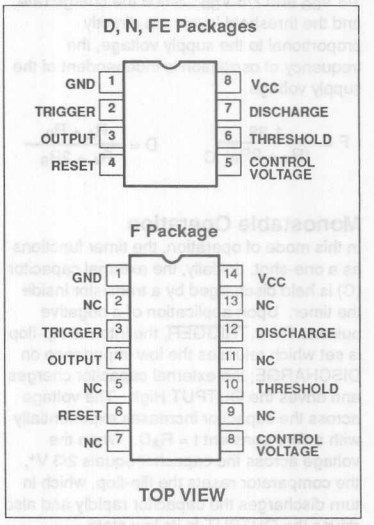
DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

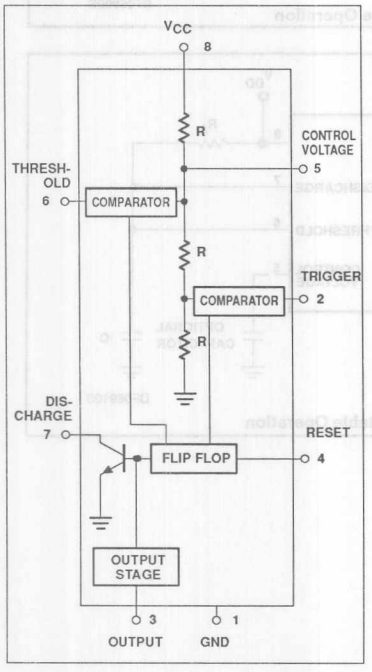
FEATURES

- Turn-off time less than 2µs
- Max. operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

PIN CONFIGURATIONS



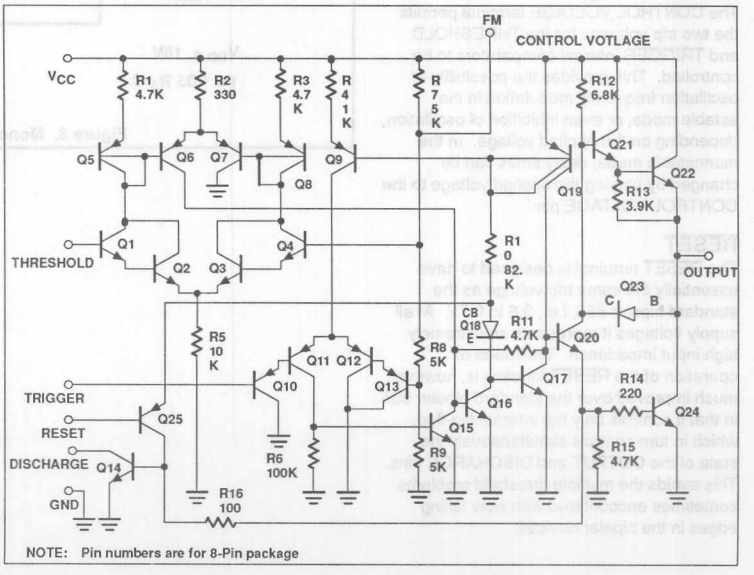
BLOCK DIAGRAM



APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE555D
8-Pin Plastic DIP	0 to +70°C	NE555N
8-Pin Plastic DIP	-40°C to +85°C	SA555N
8-Pin Plastic SO	-40°C to +85°C	SA555D
8-Pin Hermetic Cerdip	-55°C to +125°C	SE555CFE
8-Pin Plastic DIP	-55°C to +125°C	SE555CN
14-Pin Plastic DIP	-55°C to +125°C	SE555N
8-Pin Hermetic Cerdip	-55°C to +125°C	SE555FE
14-Pin Ceramic DIP	0 to +70°C	NE555F
14-Pin Ceramic DIP	-55°C to +125°C	SE555F
14-Pin Ceramic DIP	-55°C to +125°C	SE555CF

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	SE555	+18	V
	NE555, SE555C, SA555	+16	V
P_D	Maximum allowable power dissipation[1]	600	mW
T_A	Operating ambient temperature range		
	NE555	0 to +70	°C
	SA555	-40 to +85	°C
	SE555, SE555C	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

1. The junction temperature must be kept below 125°C for the D package and below 150°C for the FE, N and F packages. At ambient temperatures above 25°C, where this limit would be derated by the following factors:
   D package 160°C/W
   FE package 150°C/W
   N package 100°C/W
   F package 105°C/W

DC AND AC ELECTRICAL CHARACTERISTICS

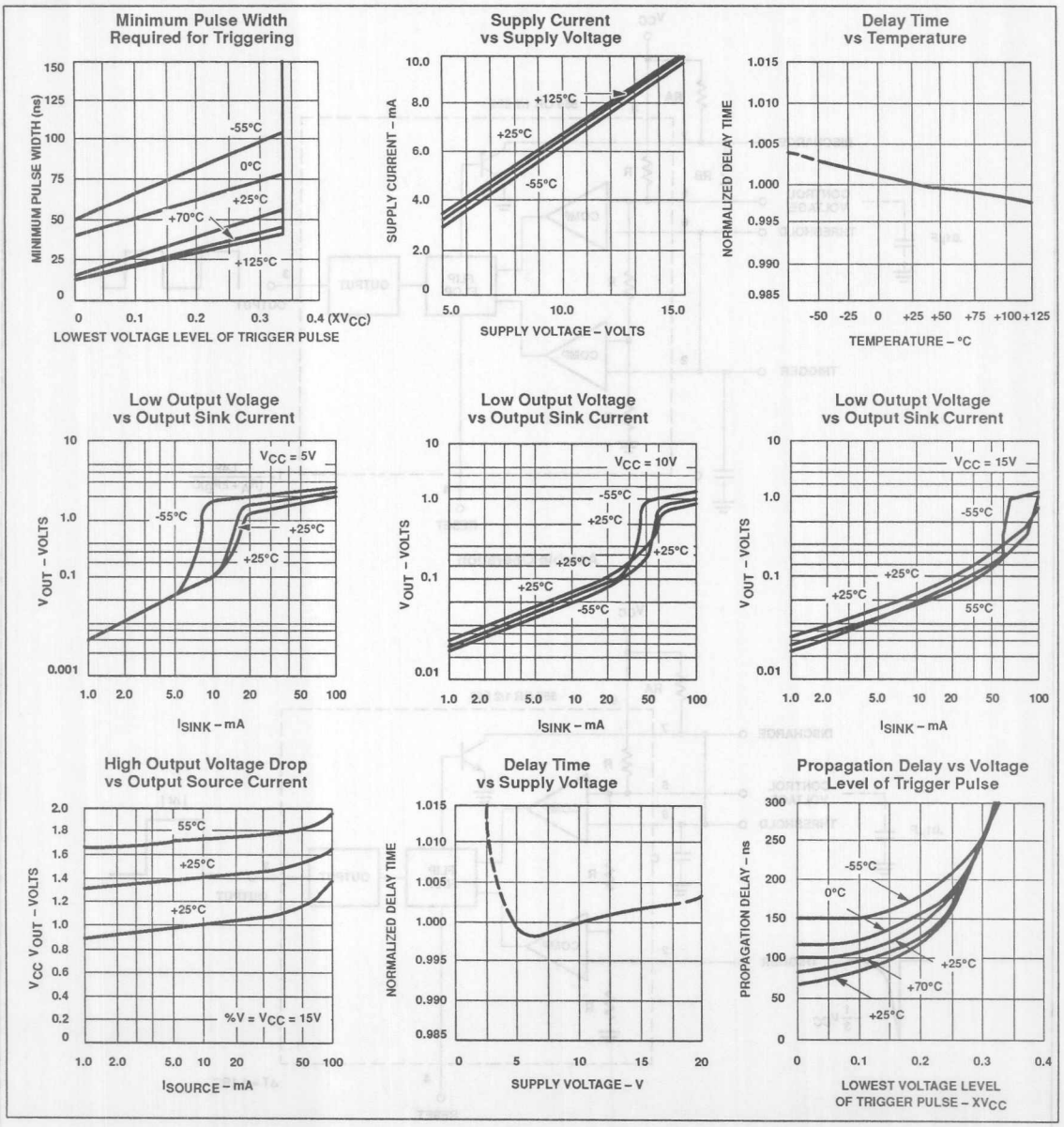
T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	V_{CC}=5V, R_L=∞		3	5		3	6	mA
		V_{CC}=15V, R_L=∞		10	12		10	15	mA
	Timing error (monostable)	R_A=2kΩ to 100kΩ							
t_M	Initial accuracy[2]	C=0.1μF		0.5	2.0		1.0	3.0	%
$\Delta t_M/\Delta T$	Drift with temperature			30	100		50	150	ppm/°C
$\Delta t_M/\Delta V_S$	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
	Timing error (astable)	R_A, R_B=1kΩ to 100kΩ							
t_A	Initial accuracy[2]	C=0.1μF		4	6		5	13	%
$\Delta t_A/\Delta T$	Drift with temperature	V_{CC}=15V			500			500	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.15	0.6		0.3	1	%/V
V_C	Control voltage level	V_{CC}=15V	9.6	10.0	10.4	9.0	10.0	11.0	V
		V_{CC}=5V	2.9	3.33	3.8	2.6	3.33	4.0	V
V_{TH}	Threshold voltage	V_{CC}=15V	9.4	10.0	10.6	8.8	10.0	11.2	V
		V_{CC}=5V	2.7	3.33	4.0	2.4	3.33	4.2	V
I_{TH}	Threshold current[3]			0.1	0.25		0.1	0.25	μA
V_{TRIG}	Trigger voltage	V_{CC}=15V	4.8	5.0	5.2	4.5	5.0	5.6	V
		V_{CC}=5V	1.45	1.67	1.9	1.1	1.67	2.2	V
I_{TRIG}	Trigger current	V_{TRIG}=0V		0.5	0.9		0.5	2.0	μA
V_{RESET}	Reset voltage[4]	V_{CC}=15V, V_{TH} =10.5V	0.3		1.0	0.3		1.0	V
I_{RESET}	Reset current	V_{RESET}=0.4V		0.1	0.4		0.1	0.4	mA
	Reset current	V_{RESET}=0V		0.4	1.0		0.4	1.5	mA
V_{OL}	Output voltage (low)	V_{CC}=15V							
		I_{SINK}=10mA		0.1	0.15		0.1	0.25	V
		I_{SINK}=50mA		0.4	0.5		0.4	0.75	V
		I_{SINK}=100mA		2.0	2.2		2.0	2.5	V
		I_{SINK}=200mA		2.5			2.5		V
		V_{CC}=5V							
		I_{SINK}=8mA		0.1	0.25		0.3	0.4	V
		I_{SINK}=5mA		0.05	0.2		0.25	0.35	V
V_{OH}	Output voltage (high)	V_{CC}=15V							
		I_{SOURCE}=200mA		12.5			12.5		V
		I_{SOURCE}=100mA	13.0	13.3		12.75	13.3		V
		V_{CC}=5V							
		I_{SOURCE}=100mA	3.0	3.3		2.75	3.3		V
t_{OFF}	Turn-off time[5]	V_{RESET}=V_{CC}		0.5	2.0		0.5	2.0	μs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

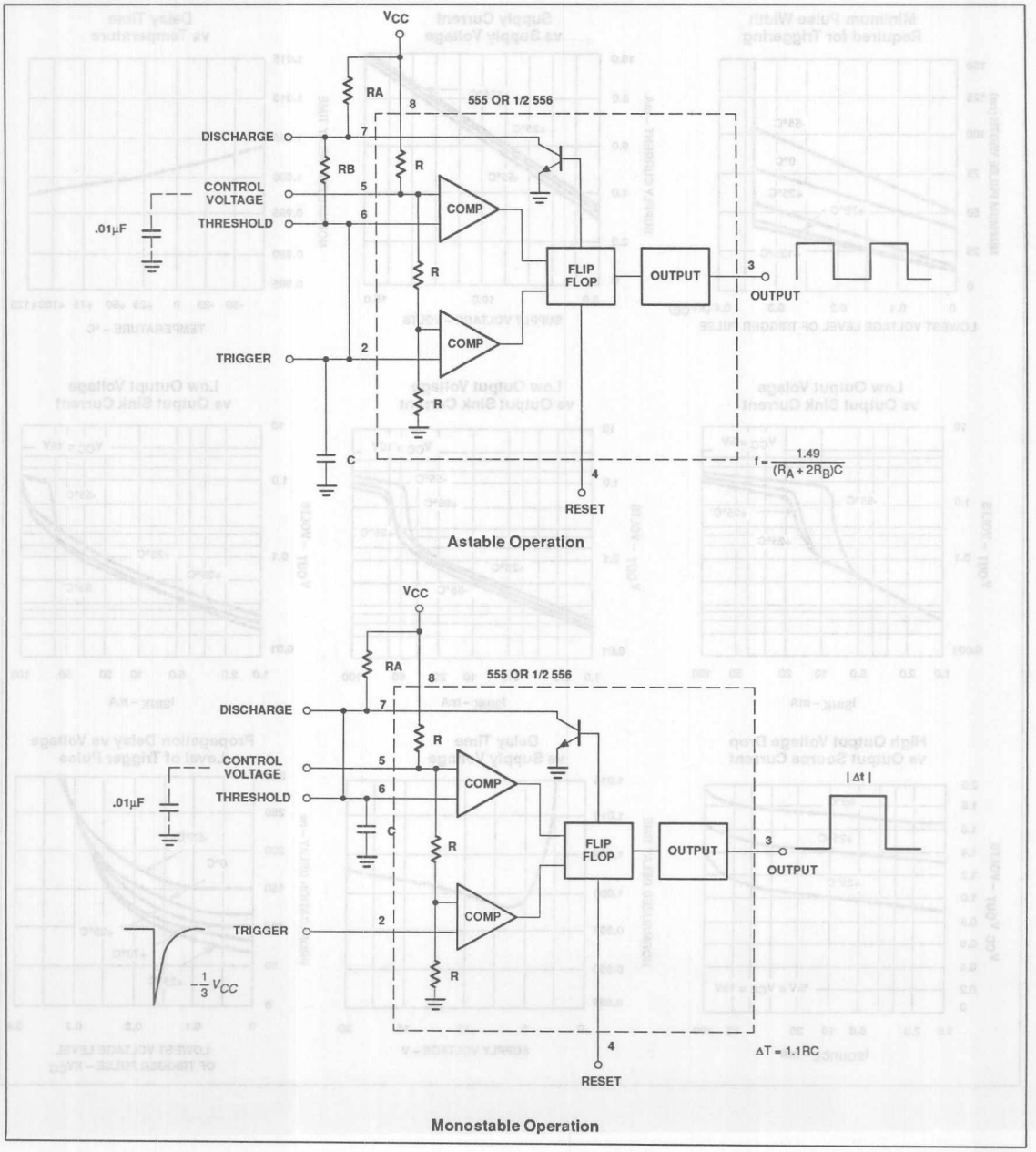
NOTES:

1. Supply current when output high typically 1mA less.
2. Tested at V_{CC}=5V and V_{CC}=15V.
3. This will determine the max value of R_A+R_B, for 15V operation, the max total R=10MΩ, and for 5V operation, the max. total R=3.4MΩ.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to 0.8×V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL APPLICATIONS

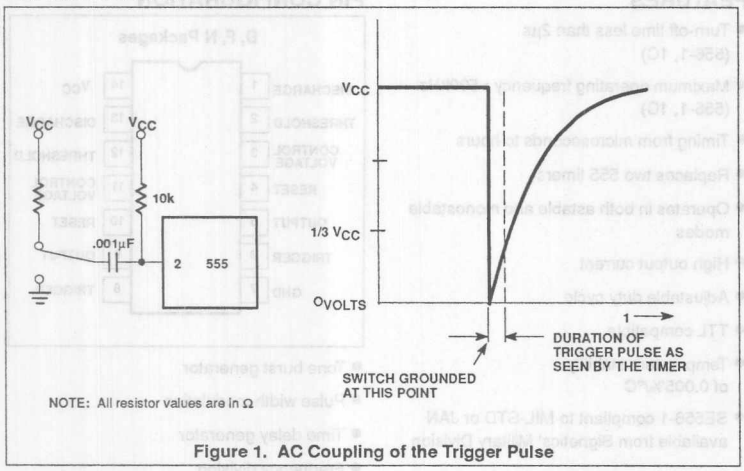


Figure 1. AC Coupling of the Trigger Pulse

Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 1, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bistable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the "turn-off time". This is the measurement of the amount of time required after the threshold reaches 2/3 V_{CC} to turn the output low. To explain further, Q_1 at the threshold input turns on after reaching 2/3 V_{CC}, which then turns on Q_5, which turns on Q_6. Current from Q_6 turns on Q_{16} which turns Q_{17} off. This allows current from Q_{19} to turn on Q_{20} and Q_{24} to given an output low. These steps cause the 2µs max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low, Q_{10} is on and turns on Q_{11} which turns on Q_{15}. Q_{15} turns off Q_{16} and allows Q_{17} to turn on. This turns off current to Q_{20} and Q_{24}, which results in output high. When the trigger is released, Q_{10} and Q_{11} shut off, Q_{15} turns off, Q_{16} turns on and the circuit then follows the same path and time delay explained as "turn off time". This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.

Dual timer

NE/SA/SE556/NE556-1

DESCRIPTION

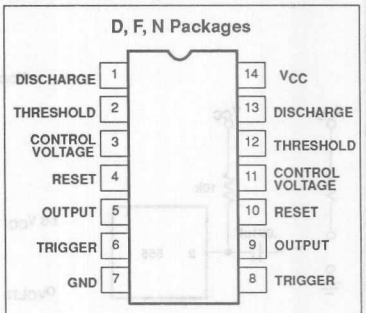
Both the 556 and 556-1 Dual Monolithic timing circuits are highly stable controllers capable of producing accurate time delays or oscillation. The 556 and 556-1 are a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other, sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

FEATURES

- Turn-off time less than 2µs (556-1, 1C)
- Maximum operating frequency >500kHz (556-1, 1C)
- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005%/°C
- SE556-1 compliant to MIL-STD or JAN available from Signetics' Military Division

PIN CONFIGURATION

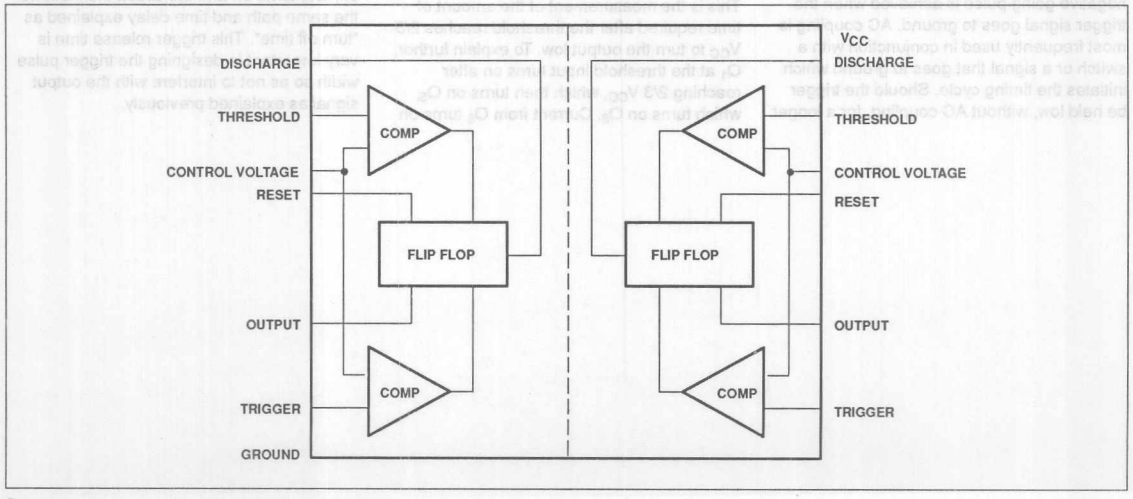
D, F, N Packages



APPLICATIONS

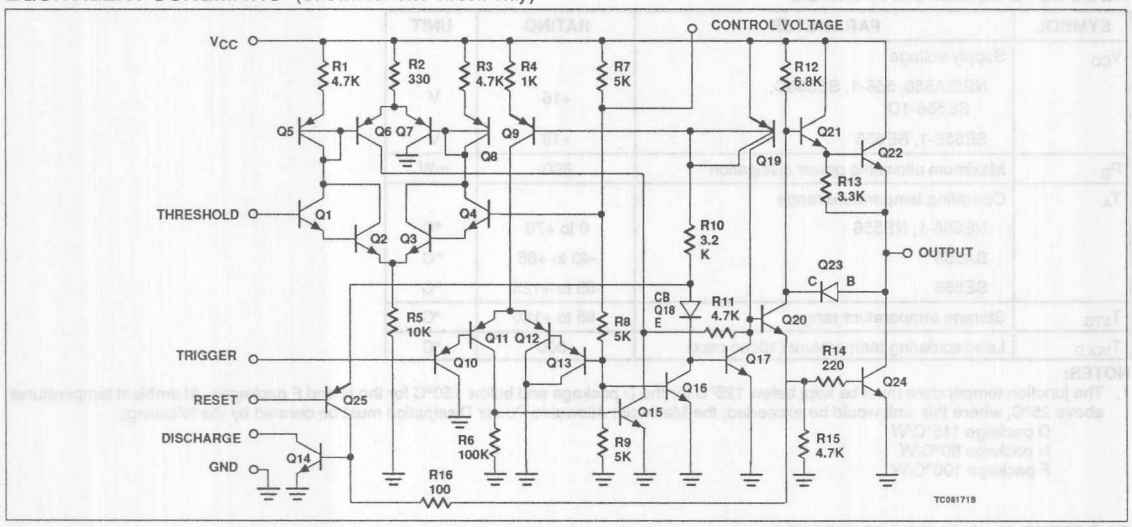
- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Touch-Tone®encoder
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control

BLOCK DIAGRAM



®Touch-Tone is a registered trademark of AT&T

EQUIVALENT SCHEMATIC (Shown for one circuit only)



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE556D
14-Pin Cerdip	0 to +70°C	NE556F
14-Pin Plastic DIP	0 to +70°C	NE556N
14-Pin Cerdip	0 to +70°C	NE556-1F
14-Pin Plastic DIP	0 to +70°C	NE556-1N
14-Pin Plastic DIP	-40°C to +85°C	SA556N
14-Pin Cerdip	-55°C to +125°C	SE556F
14-Pin Plastic DIP	-55°C to +125°C	SE556N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	NE/SA556, 556-1, SE556C, SE556-1C	+16	V
	SE556-1, SE556	+18	V
P_D	Maximum allowable power dissipation[1]	800	mW
T_A	Operating temperature range		
	NE556-1, NE556	0 to +70	°C
	SA556	-40 to +85	°C
	SE556	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

1. The junction temperature must be kept below 125°C for the D package and below 150°C for the N and F packages. At ambient temperatures above 25°C, where this limit would be exceeded, the Maximum Allowable Power Dissipation must be derated by the following:
   D package 115°C/W
   N package 80°C/W
   F package 100°C/W

ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC}=+5V to +15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE556/556-1			NE/SA556/SE556C NE556-1/SE556-1C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	V_{CC}=5V, R_L=∞		6	10		6	12	mA
		V_{CC}=15V, R_L=∞		20	24		20	30	mA
	Timing error (monostable)	R_A=2kΩ to 100kΩ							
t_M	Initial accuracy[2]	C=0.1μF		0.5	2.0		0.75	3.0	%
$\Delta t_M/\Delta T$	Drift with temperature	T=1.1 RC		30	100		50	150	ppm/°C
$\Delta t_M/\Delta V_S$	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
	Timing error (astable)	R_A, R_B=1kΩ to 100kΩ							
t_A	Initial accuracy[2]	C=0.μF		4	6		5	13	%
$\Delta t_A/\Delta T$	Drift with temperature	V_{CC}=15V		400	500		400	500	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.15	0.6		0.3	1	%/V
V_C	Control voltage level	V_{CC}=15V	9.6	10.0	10.4	9.0	10.0	11.0	V
		V_{CC}=5V	2.9	3.33	3.8	2.6	3.33	4.0	V
V_{TH}	Threshold voltage	V_{CC}=15V	9.4	10.0	10.6	8.8	10.0	11.2	V
		V_{CC}=5V	2.7	3.33	4.0	2.4	3.33	4.2	V
I_{TH}	Threshold current[3]	V_{CC} = 15V, V_{TH} = 10.5V		30	250		30	250	nA
V_{TRIG}	Trigger voltage	V_{CC}=15V	4.8	5.0	5.2	4.5	5.0	5.6	V
		V_{CC}=5V	1.45	1.67	1.9	1.1	1.67	2.2	V
I_{TRIG}	Trigger current	V_{TRIG}=0V		0.5	0.9		0.5	2.0	μA
V_{RESET}	Reset voltage[5]		0.4	0.7	1.0	0.4	0.7	1.0	V
	Reset current	V_{RESET}=0.4V	0.4	0.1	0.4	0.4	0.1	0.6	mA

ELECTRICAL CHARACTERISTICS (Continued)

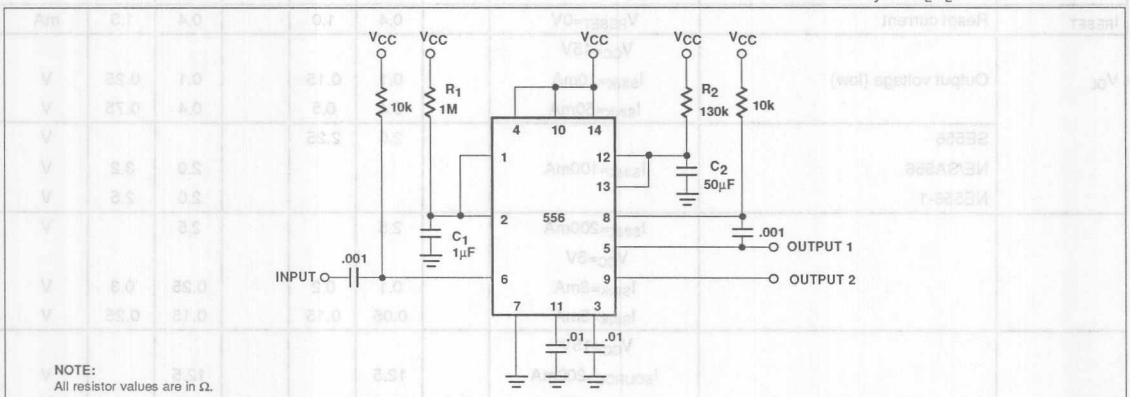
SYMBOL	PARAMETER	TEST CONDITIONS	SE556/556-1			NE/SA556/SE556C NE556-1/SE556-1C			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{RESET}	Reset current	V_{RESET}=0V		0.4	1.0		0.4	1.5	mA
V_{OL}	Output voltage (low)	V_{CC}=15V							
		I_{SINK}=10mA		0.1	0.15		0.1	0.25	V
		I_{SINK}=50mA		0.4	0.5		0.4	0.75	V
	SE556			2.0	2.25				V
	NE/SA556	I_{SINK}=100mA					2.0	3.2	V
	NE556-1						2.0	2.5	V
		I_{SINK}=200mA		2.5			2.5		V
		V_{CC}=5V							
		I_{SINK}=8mA		0.1	0.2		0.25	0.3	V
		I_{SINK}=5mA		0.05	0.15		0.15	0.25	V
V_{OH}	Output voltage (high)	V_{CC}=15V							
		I_{SOURCE}=200mA		12.5			12.5		V
		I_{SOURCE}=100mA	13.0	13.3		12.75	13.3		V
		V_{CC}=5V							
		I_{SOURCE}=100mA	3.0	3.3		2.75	3.3		V
t_{OFF}	Turn-off time[6] NE556-1	V_{RESET}=V_{CC}		0.5	2.0		0.5		µs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA
	Matching characteristics[4]								
	Initial accuracy[2]			0.5	1.0		1.0	2.0	%
	Drift with temperature			10			±10		ppm/°C
	Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

NOTES:
1. Supply current when output is high is typically 1.0mA less.
2. Tested at V_{CC}=5V and V_{CC}=15V.
3. This will determine maximum value of R_A+R_B. For 15V operation, the max total R=10MΩ, and for 5V operation, the maximum total R=3.4MΩ.
4. Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high. In order to guarantee reset the voltage at reset pin must be less than or equal to 0.4V. To disable reset function, the voltage at reset pin has to be greater than 1V.
6. Time measured from a positive-going input pulse from 0 to 0.4 V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL APPLICATIONS

One feature of the dual timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a 0.001µF coupling capacitor sequential timing may be obtained. Delay t_1 is determined by the first half and t_2 by the second half delay.

The first half of the timer is started by momentarily connecting Pin 6 to ground. When it is timed out (determined by $1.1R_1C_1$) the second half begins. Its duration is determined by $1.1R_2C_2$.

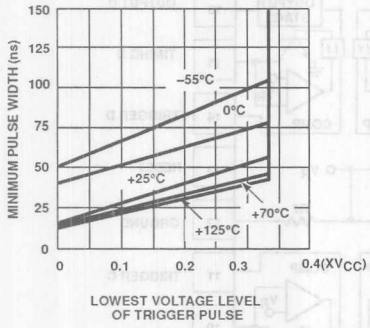


NOTE:
All resistor values are in Ω.

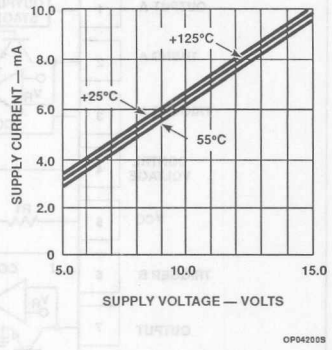
Sequential Timer

TYPICAL PERFORMANCE CHARACTERISTICS

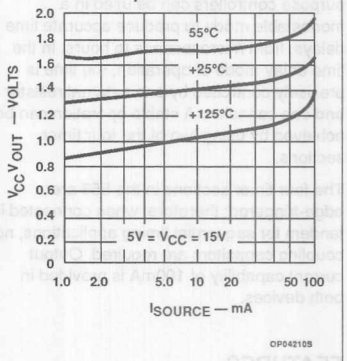
Minimum Pulse Width Required for Triggering



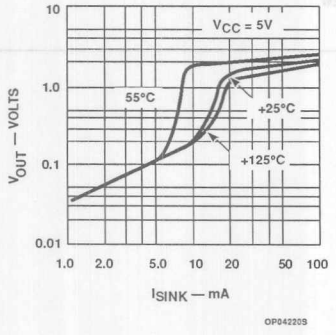
Supply Current VS Supply Voltage



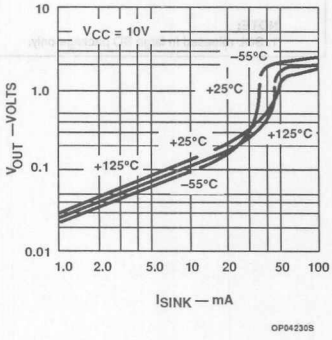
High Output Voltage Drop vs Output Source Current



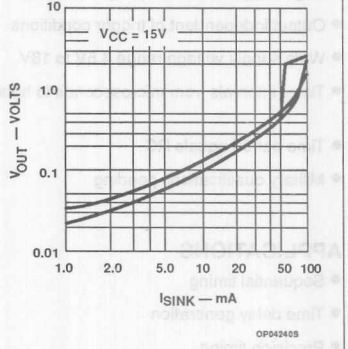
Low Output Voltage vs Output Sink Current



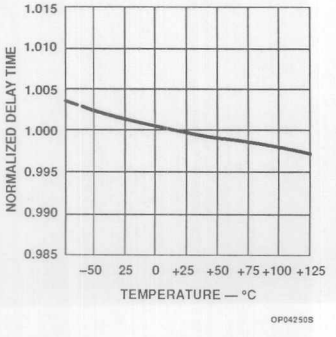
Low Output vs Output Sink Current



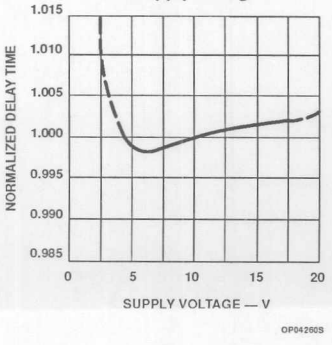
Low Output Voltae vs Output Sink Current



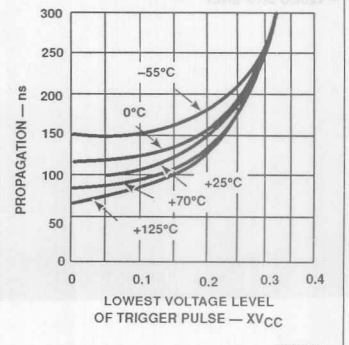
Delay Time vs Temperature



Delay Time vs Supply Voltage



Propagation Delay vs Voltage Level of Trigger Pulse



Quad timer

NE558

DESCRIPTION

The 558 Quad Timers are monolithic timing devices which can be used to produce four independent timing functions. The 558 output sinks current. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays; from microseconds to hours. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. A stable operation can be achieved by using two of the four timer sections.

The four timer sections in the 558 are edge-triggered; therefore, when connected in tandem for sequential timing applications, no coupling capacitors are required. Output current capability of 100mA is provided in both devices.

FEATURES

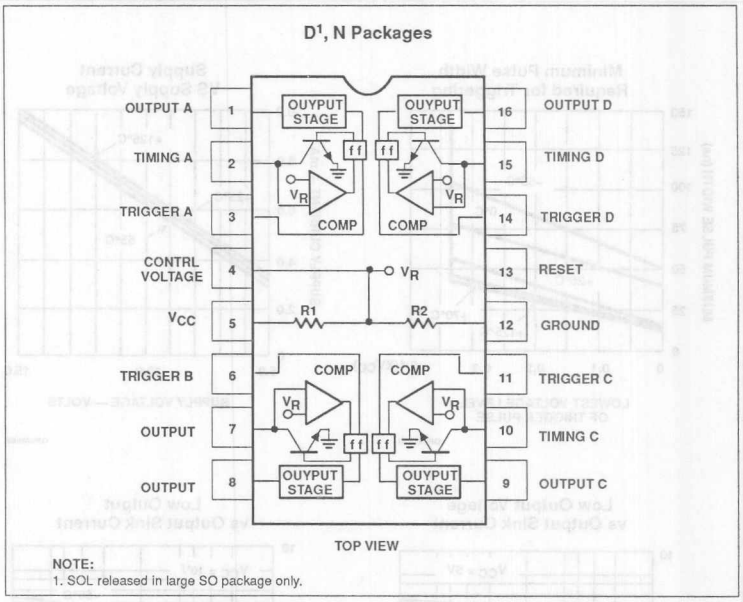
- 100mA output current per section
- Edge-triggered (no coupling capacitor)
- Output independent of trigger conditions
- Wide supply voltage range 4.5V to 18V
- Timer intervals from microseconds to hours
- Time period equals RC
- Military qualifications pending

APPLICATIONS

- Sequential timing
- Time delay generation
- Precision timing
- Industrial controls
- Quad one-shot

PIN CONFIGURATION

D[1], N Packages



NOTE:
1. SOL released in large SO package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SOL	0 to +70°C	NE558D
16-Pin Plastic DIP	0 to +70°C	NE558N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	NE/SA558	+16	V
	SE558	+18	V
P_D	Maximum power dissipation T_A=25°C ambient (still-air)[1]		
	N package	1450	mW
	D package	1090	mW
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:
1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.6mW/°C
   D package at 8.7mW/°C

T_A= 25°C V_{CC}=+5V to +15V, unless otherwise specified.

DC AND AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE558			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5		16	V
I_{CC}	Supply current	V_{CC}=Reset=15V		16	36	mA
	Timing accuracy (t=RC)	R=2kΩ to 100kΩ, C=1μF				
t_A	Initial accuracy			±2	5	%
$\Delta t_A/\Delta T$	Drift with temperature			30	150	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.1	0.9	%/V
V_{TRIG}	Trigger voltage[1]	V_{CC}=15V	0.8		2.4	V
I_{TRIG}	Trigger current	Trigger=0V		5	100	μA
V_{RESET}	Reset voltage[2]		0.8		2.4	V
I_{RESET}	Reset current	Reset		50	500	μA
V_{TH}	Threshold voltage			0.63		xV_{CC}
	Threshold leakage			15		nA
V_{OUT}	Output voltage[3]	I_L=10mA		0.1	0.4	V
		I_L=100mA		1.0	2.0	V
	Output leakage			10	500	nA
t_{PD}	Propagation delay			1.0		μs
t_R	Rise time of output	I_L=100mA		100		ns
t_F	Fall time of output	I_L=100mA		100		ns

NOTES:
1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset, the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8V, outputs set low and trigger inhibited. For reset above 2.4V, trigger enabled.
3. The 558 output structure is open-collector which requires a pull-up resistor to V_{CC} to sink current. The output is normally low sinking current.

558 EQUIVALENT CIRCUIT

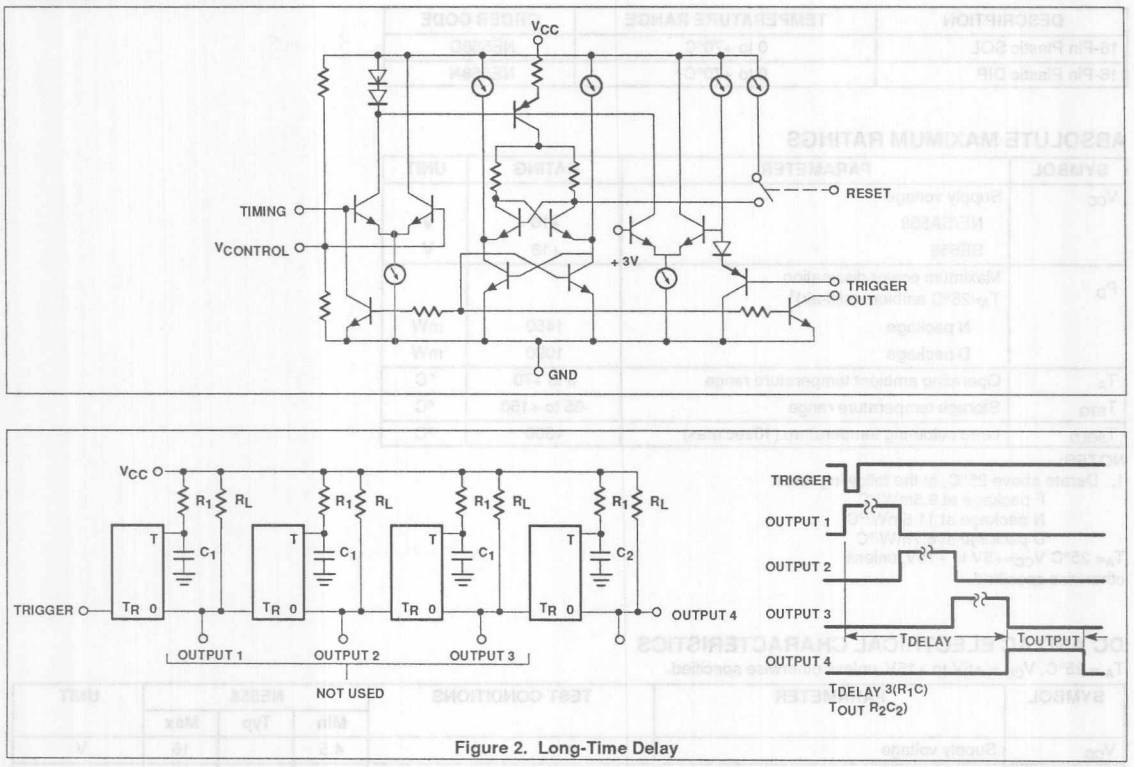
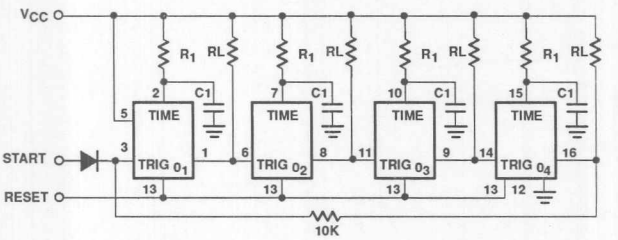
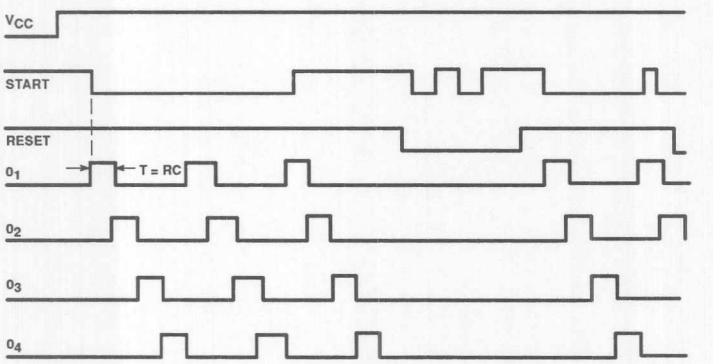


Figure 2. Long-Time Delay



a. Ring Counter



b. Expected Waveforms

Figure 3.

a. Ring Counter

b. Expected Waveforms

Figure 3.

Section 5
High Frequency Phase-Locked Loops / Function Generators

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Section 5
High Frequency Phase-Locked Loops \ Function Generators

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Phase-locked loop

NE/SE564

DESCRIPTION

The NE/SE564 is a versatile, high guaranteed frequency phase-locked loop designed for operation up to 50MHz. As shown in the Block Diagram, the NE/SE564 consists of a VCO, limiter, phase comparator, and post detection processor.

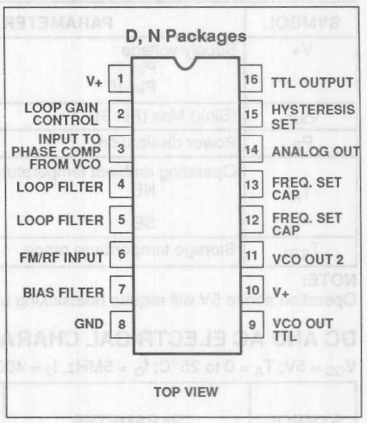
FEATURES

- Operation with single 5V supply
- TTL-compatible inputs and outputs
- Guaranteed operation to 50MHz
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications
- Can be used as a modulator
- Variable loop gain (externally controlled)

APPLICATIONS

- High speed modems
- FSK receivers and transmitters
- Frequency Synthesizers
- Signal generators
- Various satcom/TV systems
- pin configuration

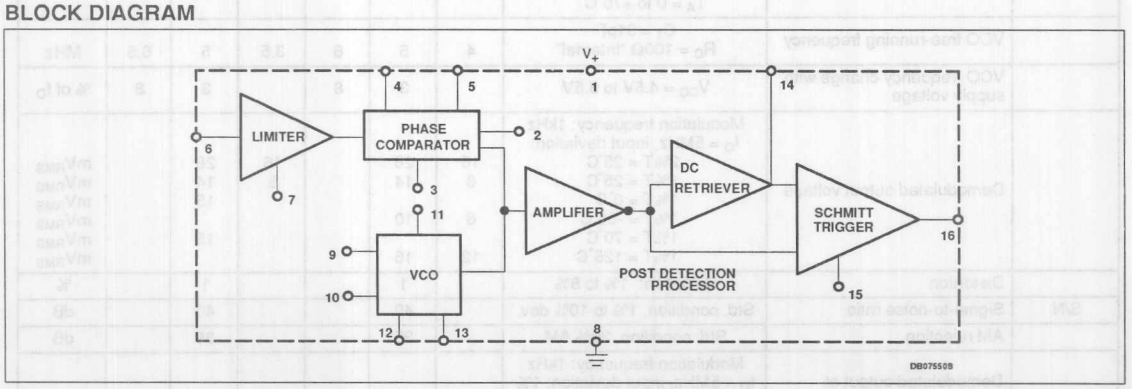
PIN CONFIGURATIONS



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE564D
16-Pin Plastic DIP	0 to +70°C	NE564N
16-Pin Plastic DIP	-55 to +125°C	SE564N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V+	Supply voltage Pin 1 Pin 10	 14 6	 V V
I_{OUT}	(Sink) Max (Pin 9)	10	mA
P_D	Power dissipation	600	mW
T_A	Operating ambient temperature NE SE	 0 to +70 -55 to +125	 °C °C
T_{STG}	Storage temperature range	-65 to +150	°C

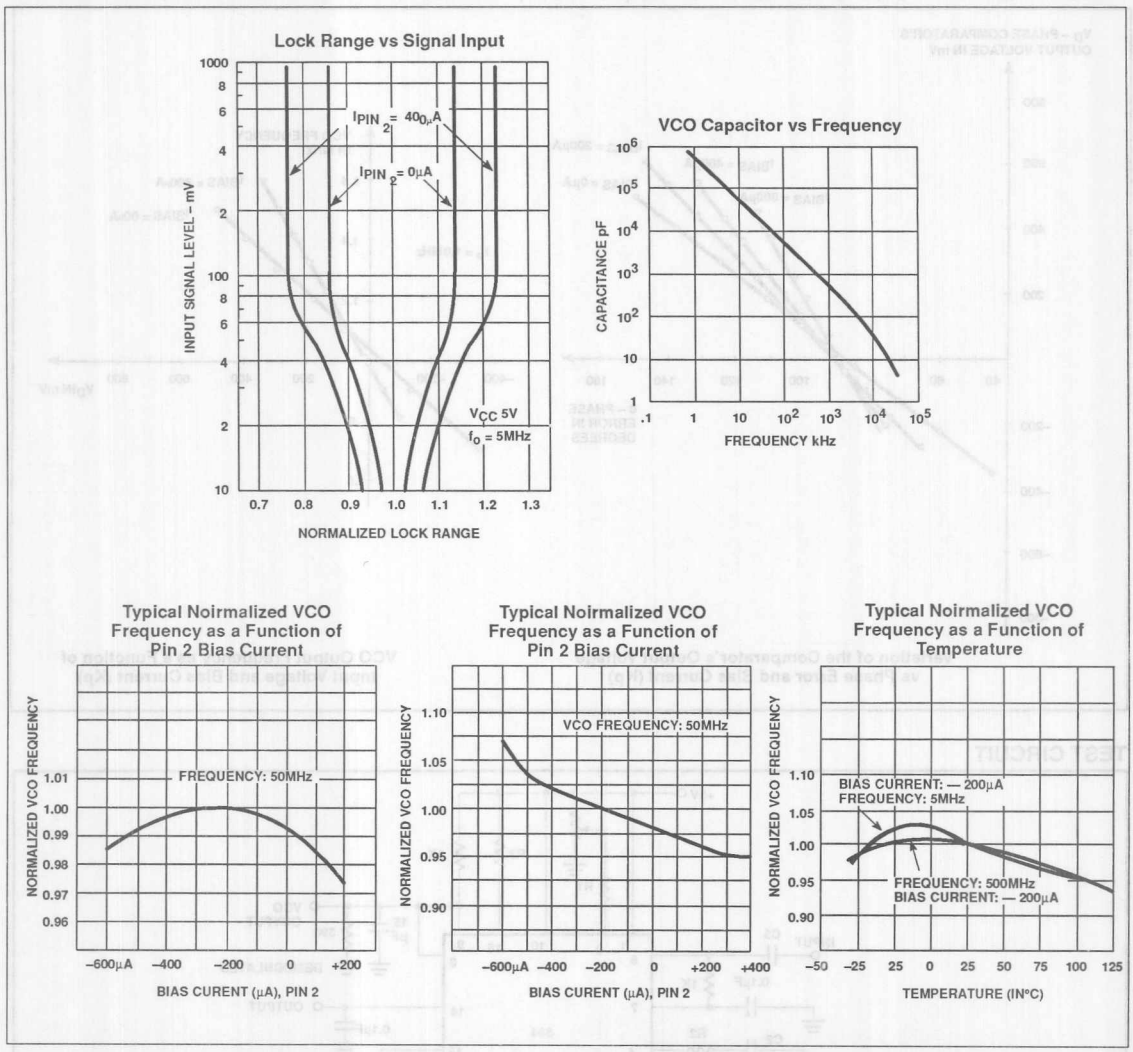
NOTE:
Operation above 5V will require heatsinking of the case.

DC AND AC ELECTRICAL CHARACTERISTICS

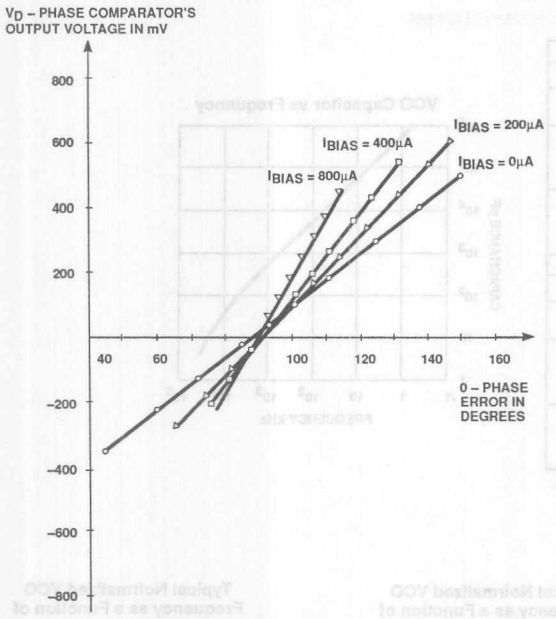
V_{CC} = 5V; T_A = 0 to 25°C; f_O = 5MHz, I_2 = 400µA; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SE564			LIMITS NE564			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Maximum VCO frequency	C_1 = 0 (stray)	45	60		45	60		MHz
	Lock range	Input ≥ 200mV$_{RMS}$ T_A = 25°C T_A = 125°C T_A = -55°C T_A = 0°C T_A = 70°C	 40 20 50	 70 30 80		 40	 70 70 40		% of f_O
	Capture range	Input ≥ 200mV$_{RMS}$, R_2 = 27Ω	20	30		20	30		% of f_O
	VCO frequency drift with temperature	f_O = 5MHz, T_A = -55°C to +125°C T_A = 0 to +70°C = 0 to +70°C f_O = 5MHz, T_A = -55°C to +125°C T_A = 0 to +70°C		500 300	1500 800		 600 500		PPM/°C
	VCO free-running frequency	C_1 = 91pF R_C = 100Ω "Internal"	4	5	6	3.5	5	6.5	MHz
	VCO frequency change with supply voltage	V_{CC} = 4.5V to 5.5V		3	8		3	8	% of f_O
	Demodulated output voltage	Modulation frequency: 1kHz f_O = 5MHz, input deviation: 2%T = 25°C 1%T = 25°C 1%T = 0°C 1%T = -55°C 1%T = 70°C 1%T = 125°C	 16 8 6 12	 28 14 10 16		 16 8	 28 14 13 15		 mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$
	Distortion	Deviation: 1% to 8%		1			1		%
S/N	Signal-to-noise ratio	Std. condition, 1% to 10% dev.		40			40		dB
	AM rejection	Std. condition, 30% AM		35			35		dB
	Demodulated output at operating voltage	Modulation frequency: 1kHz f_O = 5MHz, input deviation: 1% V_{CC} = 4.5V V_{CC} = 5.5V	 7 8	 12 14		 7 8	 12 14		 mV$_{RMS}$ mV$_{RMS}$
I_{CC}	Supply current	V_{CC} = 5V I_1, I_{10}		45	60		45	60	mA
	Output "1" output leakage current "0" output voltage	V_{OUT} = 5V, Pins 16, 9 I_{OUT} = 2mA, Pins 16, 9 I_{OUT} = 6mA, Pins 16, 9		 1 0.3 0.4	 20 0.6 0.8		 1 0.3 0.4	 20 0.6 0.8	 µA V V

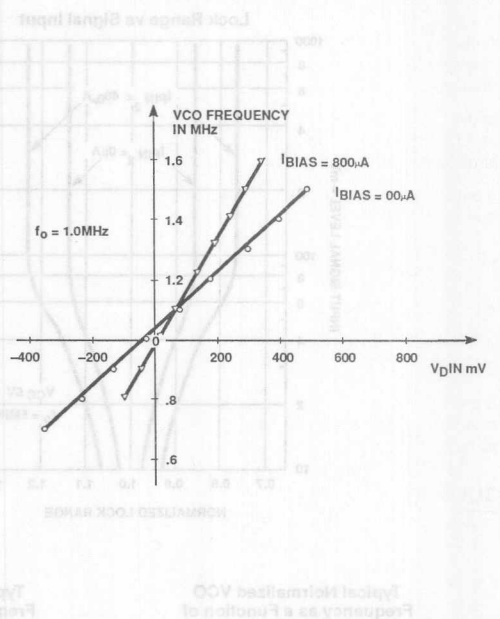
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

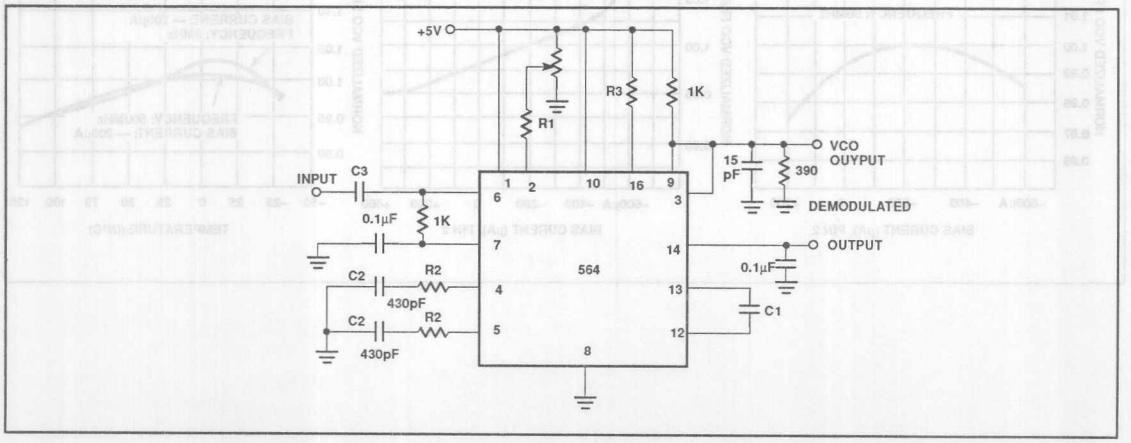


Variation of the Comparator's Output Voltage vs Phase Error and Bias Current (Kp)



VCO Output Frequency as a Function of Input Voltage and Bias Current (Kp)

TEST CIRCUIT



FUNCTIONAL DESCRIPTION

(Figure 1)

The NE564 is a monolithic phase-locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz.

In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{IN} - f_O)}{K_{VCO}} \quad (1)$$

K_{VCO} = conversion gain of the VCO

f_{IN} = frequency of the input signal

f_O = free-running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{IN} from f_O. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at Pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free-running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the DC levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrowband signals where the deviation in f_{IN} itself may be less than the change in f_O due to temperature. This effect can be eliminated if the DC or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the DC levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high-frequency performance, an emitter-coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q21 and Q23 with current sources Q25 - Q26 form the basic oscillator. The approximate free-running frequency of the oscillator is shown in the following equation:

$$f_O \cong \frac{1}{22\, R_C\, (C_1 + C_S)} \quad (2)$$

EQUIVALENT SCHEMATIC

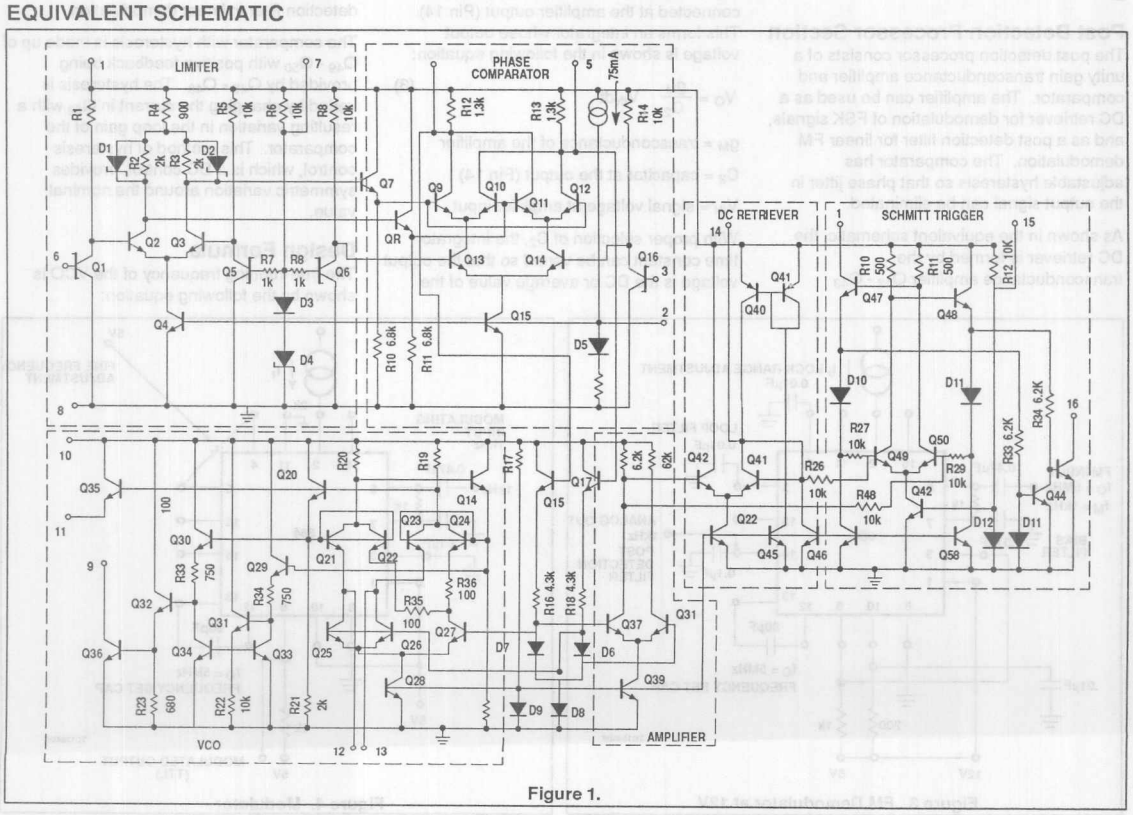


Figure 1.

$R_C = R_{19} = R_{20} = 100\Omega$ (INTERNAL)

C_1 = external frequency setting capacitor

C_S = stray capacitance

Variation of V_D (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase detection processor consists of a doubled-balanced modulator with a limiter amplifier to improve AM rejection. Schottky-clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at Pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a DC retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the DC retriever is formed by the transconductance amplifier Q_{42} - Q_{43} together with an external capacitor which is connected at the amplifier output (Pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_O = \frac{g_M}{C_2} \int V_{IN} dt \qquad (3)$$

g_M = transconductance of the amplifier

C_2 = capacitor at the output (Pin 14)

V_{IN} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied so that the output voltage is the DC or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of Q_{49} - Q_{50} with positive feedback being provided by Q_{47} - Q_{48}. The hysteresis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a DC control, provides symmetric variation around the nominal value.

Design Formula

The free-running frequency of the VCO is shown by the following equation:

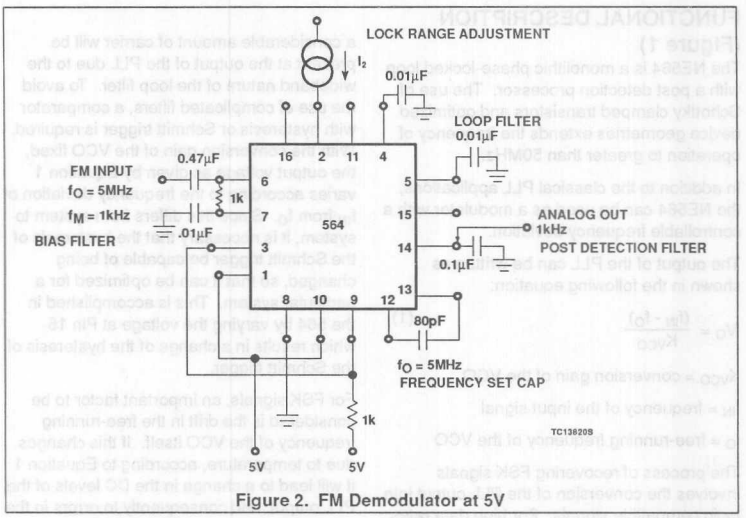


Figure 2. FM Demodulator at 5V

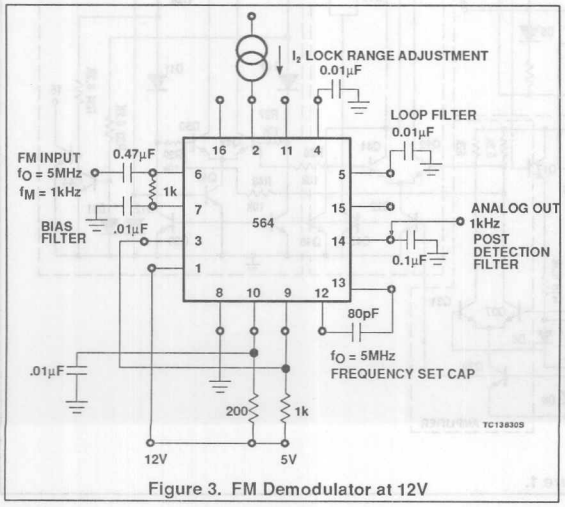


Figure 3. FM Demodulator at 12V

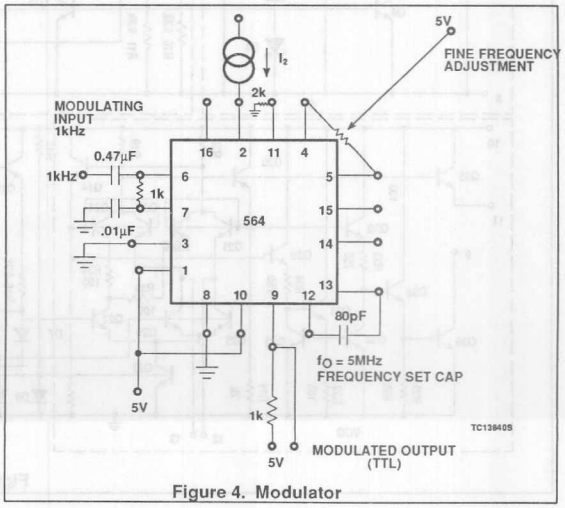


Figure 4. Modulator

$$f_O \cong \frac{1}{22\,R_C\,(C_1 + C_S)} \quad (4)$$

$R_C = 100\Omega$

C_1 = external cap in farads

C_S = stray capacitance

The loop filter diagram shown is explained by the following equation:

$$f_S = \frac{1}{1 + sRC_3} \text{ (First Order)} \quad (5)$$

$R = R_{12} = R_{13} = 1.3k\Omega$ (Internal)*

By adding capacitors to Pins 4 and 5, a pole is added to the loop transfer at

$$\omega = \frac{1}{RC_3}$$

NOTE:
*Refer to Figure 1.

APPLICATIONS

FM Demodulator

The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in Figures 2 and 3, respectively. The input signal is AC coupled with the output signal being extracted at Pin 14. Loop filtering is provided by the capacitors at Pins 4 and 5 with additional filtering being provided by the capacitor at Pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be 1% or higher.

Modulation Techniques

The NE564 phase-locked loop can be modulated at either the loop filter ports (Pins 4 and 5) or the input port (Pin 6) as shown in Figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in Figure 5. This curve will be appropriate for signals injected into Pins 4 and 5 as shown in Figure 4.

FSK Demodulation

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5V power supply. Demodulated DC voltages associated with the mark and space frequencies are recovered with a single external capacitor in a DC retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high-frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 5 shows a high-frequency FSK decoder designed for input frequency deviations of ±1.0MHz centered around a free-running frequency of 10.8MHz. the value of the timing capacitance required was estimated from Figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune f_O' 10.8MHz.

The lock range graph indicates that the +1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero Pin 2 bias current. (While strictly this figure is appropriate only for 50MHz, it can be used as a guide for lock range estimates at other f_O' frequencies).

The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in Figure 7 for 20k, 500k, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators' output voltages with respect to each other and to the FSK output. The high-frequency sum components of the input and VCO frequency also are viable as noise on the phase comparator's outputs.

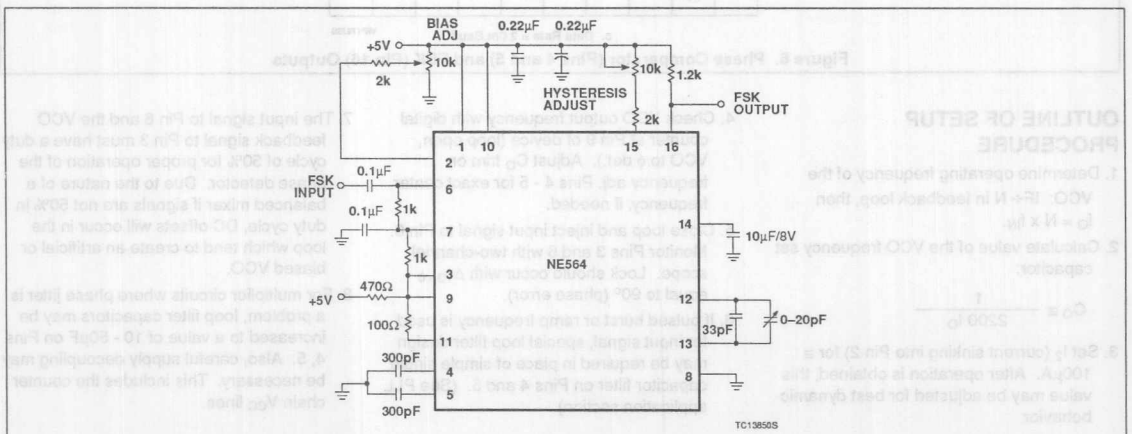


Figure 5. 10.8MHz FSK Decoder Using the 564

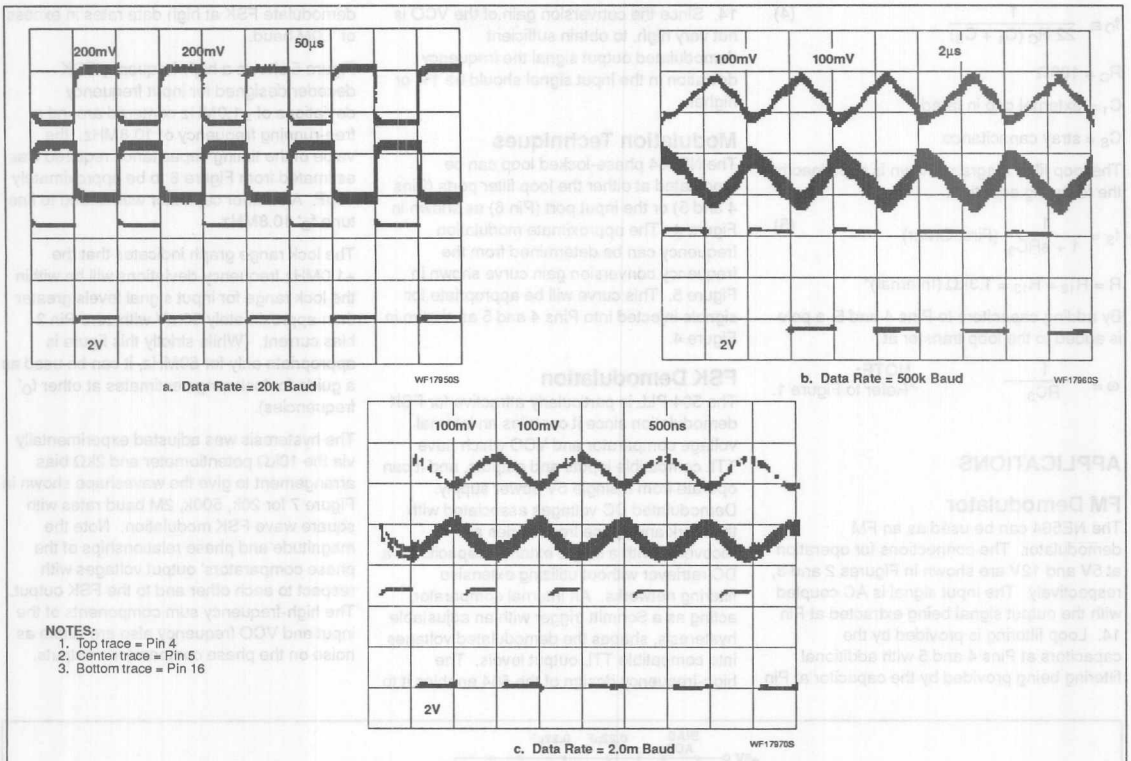


Figure 6. Phase Comparator (Pins 4 and 5) and FSK (Pin 16) Outputs

OUTLINE OF SETUP PROCEDURE

1. Determine operating frequency of the VCO: IF÷ N in feedback loop, then $f_O = N \times f_{IN}$.
2. Calculate value of the VCO frequency set capacitor:

$$C_O \cong \frac{1}{2200\ f_O}$$

3. Set I_2 (current sinking into Pin 2) for ≅ 100µA. After operation is obtained, this value may be adjusted for best dynamic behavior.
4. Check VCO output frequency with digital counter at Pin 9 of device (loop open, VCO to ϕ det.). Adjust C_O trim or frequency adj. Pins 4 - 5 for exact center frequency, if needed.
5. Close loop and inject input signal to Pin 6. Monitor Pins 3 and 6 with two-channel scope. Lock should occur with $\Delta\phi_{3-6}$ equal to 90° (phase error).
6. If pulsed burst or ramp frequency is used for input signal, special loop filter design may be required in place of simple single capacitor filter on Pins 4 and 5. (See PLL application section)
7. The input signal to Pin 6 and the VCO feedback signal to Pin 3 must have a duty cycle of 50% for proper operation of the phase detector. Due to the nature of a balanced mixer if signals are not 50% in duty cycle, DC offsets will occur in the loop which tend to create an artificial or biased VCO.
8. For multiplier circuits where phase jitter is a problem, loop filter capacitors may be increased to a value of 10 - 50µF on Pins 4, 5. Also, careful supply decoupling may be necessary. This includes the counter chain V_{CC} lines.

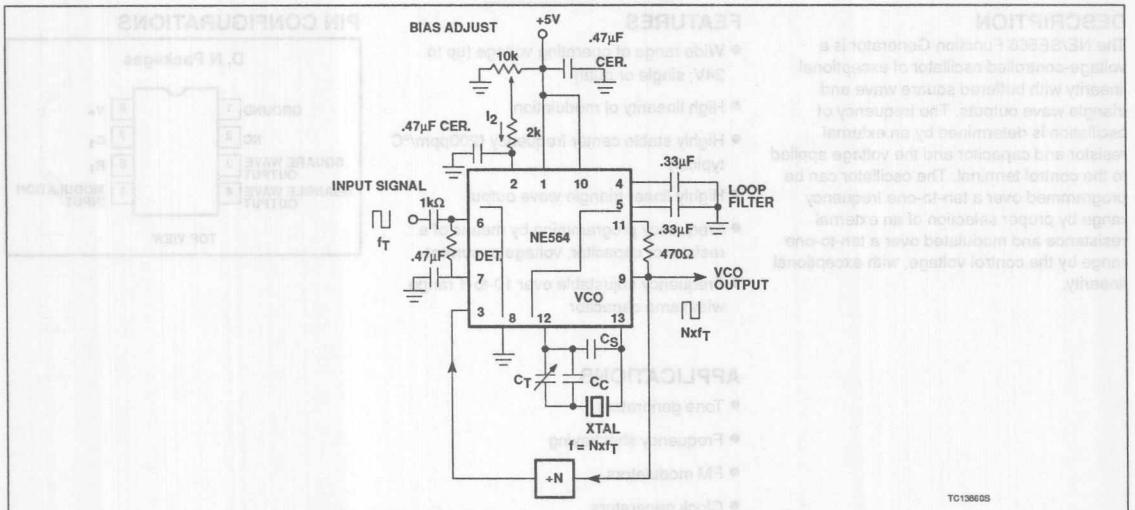


Figure 7. NE564 Phase-Locked Frequency Multiplier with VCXO

Function generator — NE/SE566

DESCRIPTION

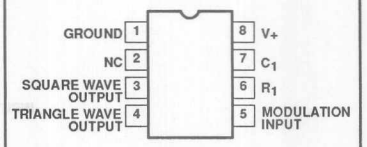
The NE/SE566 Function Generator is a voltage-controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten-to-one frequency range by proper selection of an external resistance and modulated over a ten-to-one range by the control voltage, with exceptional linearity.

FEATURES

- Wide range of operating voltage (up to 24V; single or dual)
- High linearity of modulation
- Highly stable center frequency (200ppm/°C typical)
- Highly linear triangle wave output
- Frequency programming by means of a resistor or capacitor, voltage or current
- Frequency adjustable over 10-to-1 range with same capacitor

PIN CONFIGURATIONS

D, N Packages



TOP VIEW

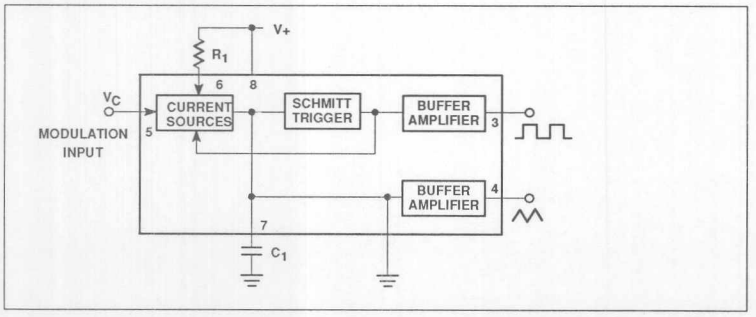
APPLICATIONS

- Tone generators
- Frequency shift keying
- FM modulators
- Clock generators
- Signal generators
- Function generators

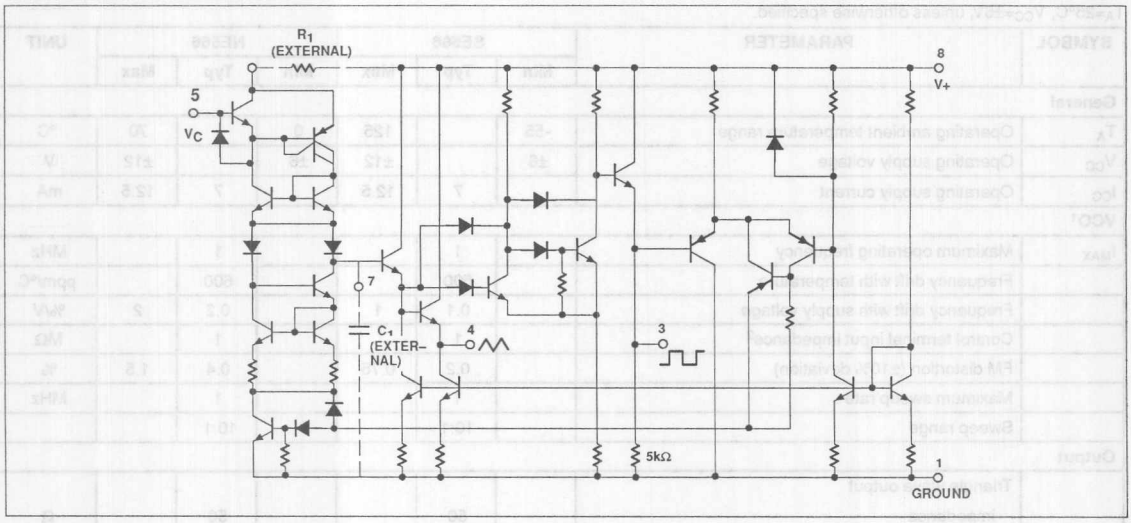
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE566D
14-Pin Cerdip	0 to +70°C	NE566F
8-Pin Plastic DIP	0 to +70°C	NE566N
8-Pin Plastic DIP	-55°C to +125°C	SE566N

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_+	Maximum operating voltage	26	V
V_{IN}	Input voltage	3	V_{P-P}
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range		
	NE566	0 to +70	°C
	SE566	-55 to +125	°C
P_D	Power dissipation	300	mW

DC ELECTRICAL CHARACTERISTICS

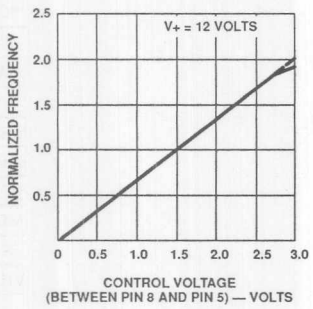
T_A=25°C, V_{CC}=±6V, unless otherwise specified.

SYMBOL	PARAMETER	SE566			NE566			UNIT
		Min	Typ	Max	Min	Typ	Max	
General								
T_A	Operating ambient temperature range	-55		125	0		70	°C
V_{CC}	Operating supply voltage	±6		±12	±6		±12	V
I_{CC}	Operating supply current		7	12.5		7	12.5	mA
VCO[1]								
f_{MAX}	Maximum operating frequency		1			1		MHz
	Frequency drift with temperature		500			600		ppm/°C
	Frequency drift with supply voltage		0.1	1		0.2	2	%/V
	Control terminal input impedance[2]		1			1		MΩ
	FM distortion (±10% deviation)		0.2	0.75		0.4	1.5	%
	Maximum sweep rate		1			1		MHz
	Sweep range		10:1			10:1		
Output								
	Triangle wave output							
	impedance		50			50		Ω
	voltage	1.9	2.4		1.9	2.4		V_{P-P}
	linearity		0.2			0.5		%
	Square wave input							
	impedance		50			50		Ω
	voltage	5	5.4		5	5.4		V_{P-P}
	duty Cycle	45	50	55	40	50	60	%
t_R	Rise time		20			20		ns
t_F	Fall Time		50			50		ns

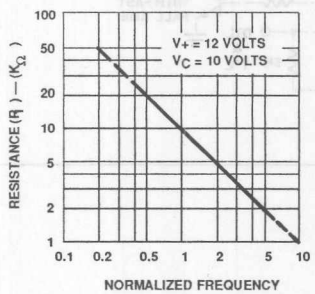
NOTES:
1. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20kΩ.
2. The bias voltage (V_C) applied to the control terminal (Pin 5) should be in the range $V+ \leq V_C \leq V+$.

TYPICAL PERFORMANCE CHARACTERISTICS

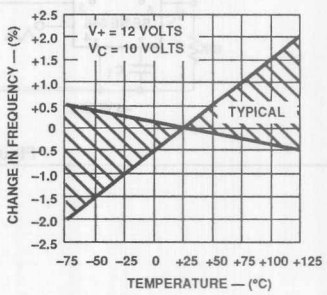
Normalized Frequency as a Function of Control Voltage



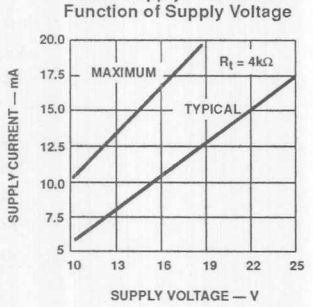
Normalized Frequency as a Function of Resistance (R1)



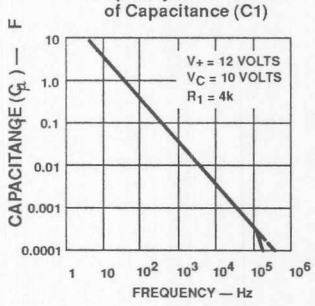
Change in Frequency as a Function of Temperature



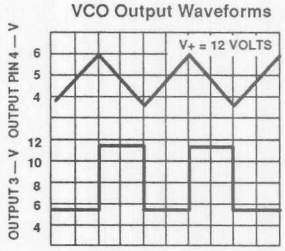
Power Supply Current as a Function of Supply Voltage



Frequency as a Function of Capacitance (C1)



VCO Output Waveforms



OPERATING INSTRUCTIONS

The NE/SE566 Function Generator is a general purpose voltage-controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1MHz. A typical connection diagram is shown in Figure 1. The control terminal (Pin 5) must be biased externally with a voltage (V_C) in the range

$$V+ \leq V_C \leq V+$$

where V_{CC} is the total supply voltage. In Figure 1, the control voltage is set by the voltage divider formed with R_2 and R_3. The modulating signal is then AC coupled with the capacitor C_2. The modulating signal can be direct coupled as well, if the appropriate DC bias voltage is applied to the control terminal. The frequency is given approximately by

$$f_O = \frac{2\,[(V+) - (V_C)]}{R_1\ C_1\ V+}$$

and R_1 should be in the range $2k\Omega < R_1 < 20k\Omega$.

A small capacitor (typically 0.001μF) should be connected between Pins 5 and 6 to eliminate possible oscillation in the control current source.

If the VCO is to be used to drive standard logic circuitry, it may be desirable to use a dual supply as shown in Figure 2. In this case the square wave output has the proper DC levels for logic circuitry. RTL can be driven directly from Pin 3. For DTL or TTL gates, which require a current sink of more than 1mA, it is usually necessary to connect a 5kΩ resistor between Pin 3 and negative supply. This increases the current sinking capability to 2mA. The third type of interface shown uses a saturated transistor between the 566 and the logic circuitry. This scheme is used primarily for TTL circuitry which requires a fast fall time (<50ns) and a large current sinking capability.

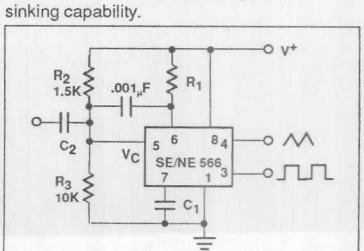


Figure 4.

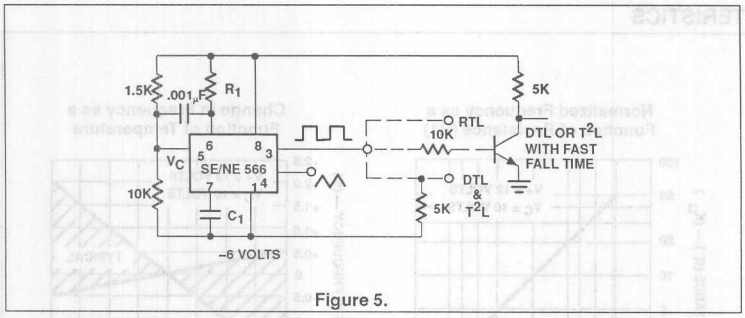

1.5K
.001μF
R1
5K
RTL
10K
DTL OR T2L
WITH FAST
FALL TIME
VC
SE/NE 566
DTL
&
T2L
10K
5K
C1
–6 VOLTS

Figure 5.

Tone decoder/phase-locked loop NE/SE567

DESCRIPTION

The NE/SE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency and output delay are independently determined by means of four external components.

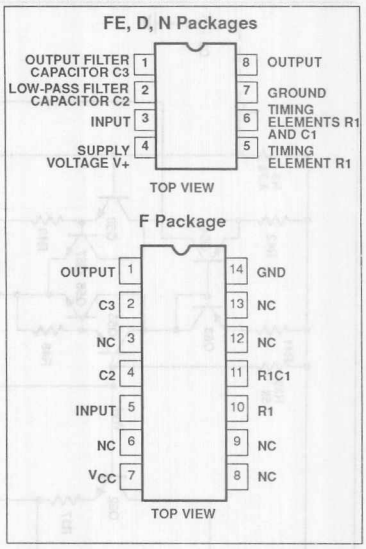
FEATURES

- Wide frequency range (.01Hz to 500kHz)
- High stability of center frequency
- Independently controllable bandwidth (up to 14%)
- High out-band signal and noise rejection
- Logic-compatible output with 100mA current sinking capability
- Inherent immunity to false signals
- Frequency adjustment over a 20-to-1 range with an external resistor
- Military processing available

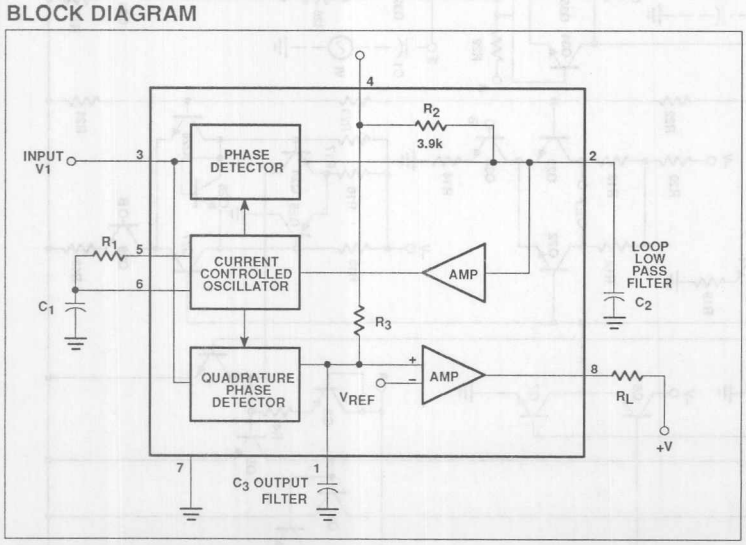
APPLICATIONS

- Touch-Tone® decoding
- Carrier current remote controls
- Ultrasonic controls (remote TV, etc.)
- Communications paging
- Frequency monitoring and control
- Wireless intercom
- Precision oscillator

PIN CONFIGURATIONS

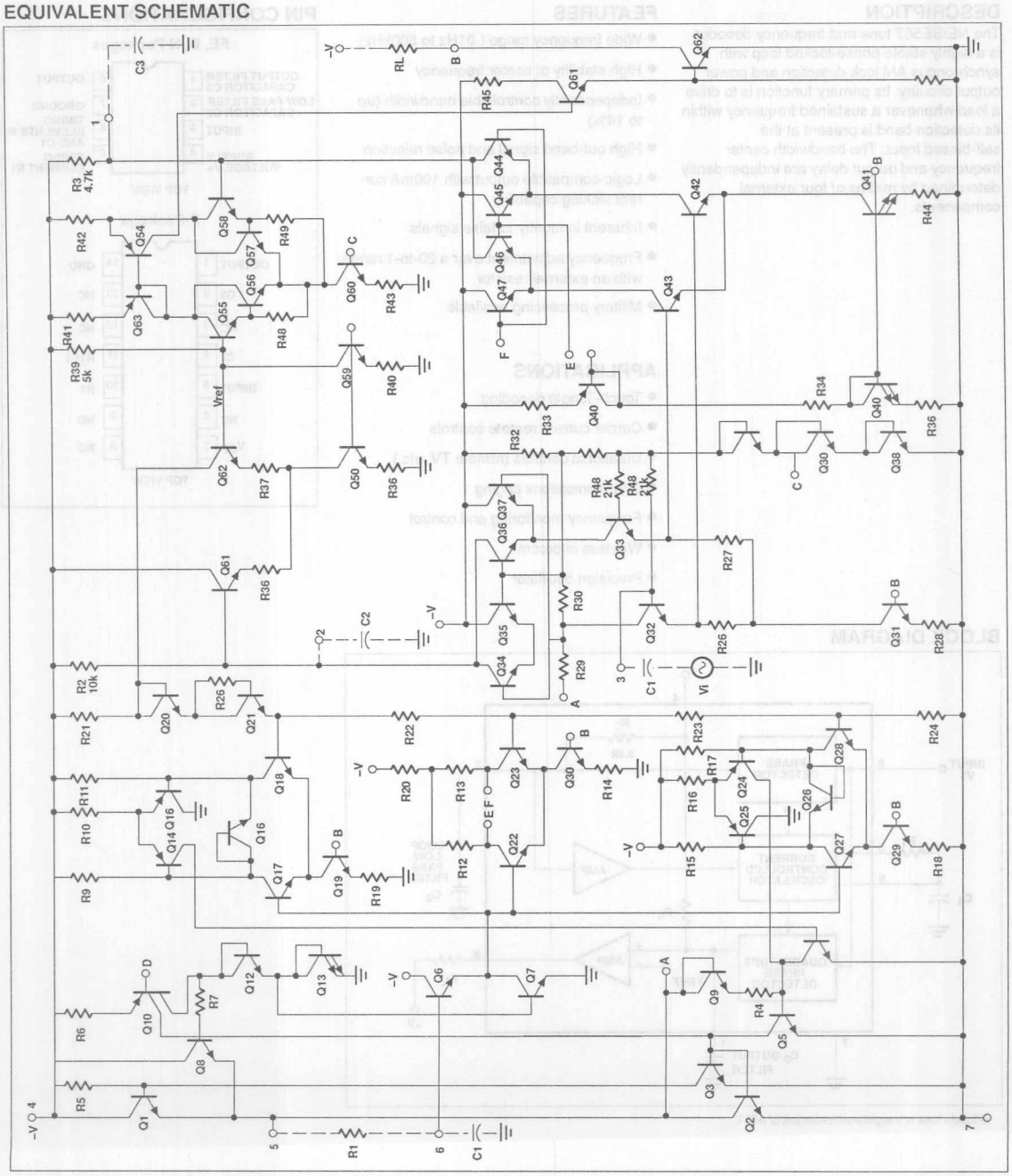


BLOCK DIAGRAM



®Touch-Tone is a registered trademark of AT&T.

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE567D
14-Pin Cerdip	0 to +70°C	NE567F
8-Pin Plastic DIP	0 to +70°C	NE567N
8-Pin Plastic SO	-55°C to +125°C	SE567D
8-Pin Cerdip	-55°C to +125°C	SE567FE
8-Pin Plastic DIP	-55°C to +125°C	SE567N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating temperature		
	NE567	0 to +70	°C
	SE567	-55 to +125	°C
V_{CC}	Operating voltage	10	V
V+	Positive voltage at input	0.5 +V_S	V
V-	Negative voltage at input	-10	V_{DC}
V_{OUT}	80Output voltage (collector of output transistor)	15	V_{DC}
T_{STG}	Storage temperature range	-65 to +150	°C
P_D	Power dissipation	300	mW

DC ELECTRICAL CHARACTERISTICS

V +=5.0V; T_A=25°C, unless otherwise specified.

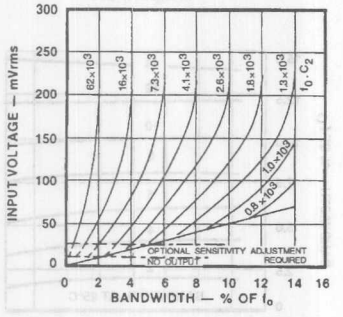
SYMBOL	PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
			Min	Typ	Max	Min	Typ	Max	
Center frequency[1]									
f_O	Highest center frequency			500			500		kHz
f_O	Center frequency stability[2]	-55 to +125°C		35 ±140			35 ±140		ppm/°C
		0 to +70°C		35 ±60			35 ±60		ppm/°C
f_O	Center frequency distribution	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$	-10	0	+10	-10	0	+10	%
f_O	Center frequency shift with supply voltage	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$		0.5	1		0.7	2	%/V
Detection bandwidth									
BW	Largest detection bandwidth	$f_O = 100kHz = \frac{1}{1.1R_1C_1}$	12	14	16	10	14	18	% of f_O
BW	Largest detection bandwidth skew			2	4		3	6	% of f_O
BW	Largest detection bandwidth—variation with temperature	V_I=300mV_{RMS}		±0.1			±0.1		%/°C
BW	Largest detectionbandwidth—variation with supply voltage	V_I=300mV_{RMS}		±2			±2		%/V
Input									
R_{IN}	Input resistance		15	20	25	15	20	25	kΩ
V_I	Smallest detectable input voltage[4]	I_L=100mA, f_I=f_O		20	25		20	25	mV_{RMS}
	Largest no-output input voltage[4]	I_L=100mA, f_I=f_O	10	15		10	15		mV_{RMS}
	Greatest simultaneous out-band signal-to-in-band signal ratio			+6			+6		dB
	Minimum input signal to wide-band noise ratio	B_n=140kHz		-6			-6		dB
Output									
	Fastest on-off cycling rate			f_O/20			f_O/20		
	"1" output leakage current	V_R=15V		0.01	25		0.01	25	µA
	"0" output voltage	I_L=30mA		0.2	0.4		0.2	0.4	V
		I_L=100mA		0.6	1.0		0.6	1.0	V
t_F	Output fall time[3]	R_L=50Ω		30			30		ns
t_R	Output rise time[3]	R_L=50Ω		150			150		ns
General									
V_{CC}	Operating voltage range		4.75		9.0	4.75		9.0	V
	Supply current quiescent			6	8		7	10	mA
	Supply current—activated	R_L=20kΩ		11	13		12	15	mA
t_{PD}	Quiescent power dissipation			30			35		mW

NOTES:

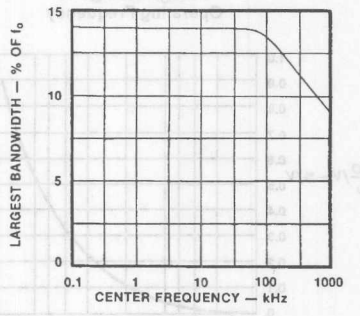
1. Frequency determining resistor R_1 should be between 2 and 20kΩ
2. Applicable over 4.75V to 5.75V. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.
4. With R_2=130kΩ from Pin 1 to V+. See Figure 1.

TYPICAL PERFORMANCE CHARACTERISTICS

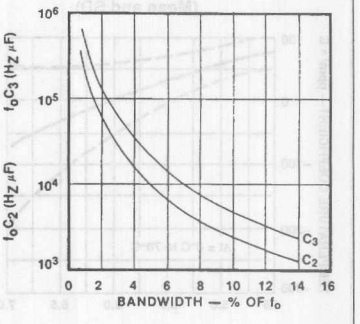
Bandwidth vs Input Signal Amplitude



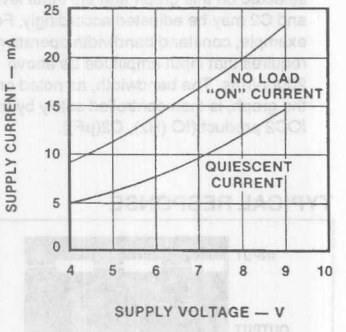
Largest Detection bandwidth vs Operating Frequency



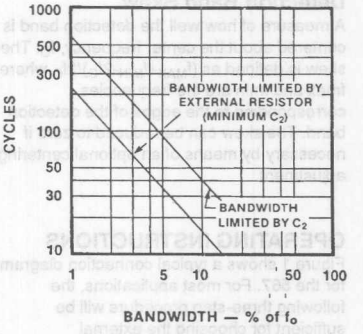
Detection bandwidth as a Function of C_2 and C_3



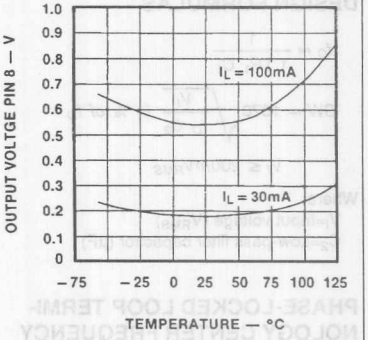
Typical Supply Current vs Supply Voltage



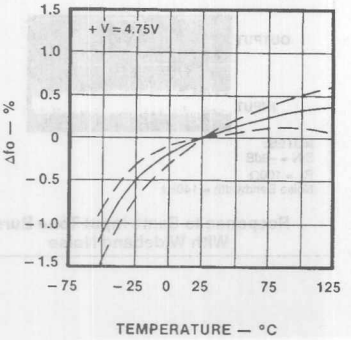
Greatest Number of Cycles Before Output



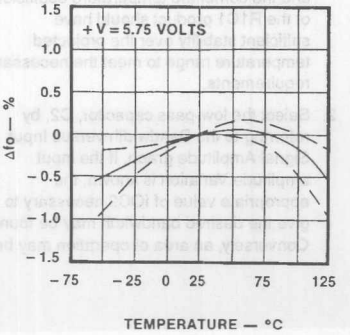
Typical Output Voltage vs Temperature



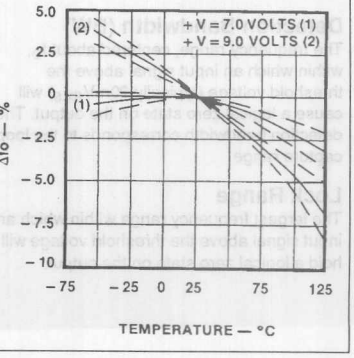
Typical Frequency Drift With Temperature (Mean and SD)



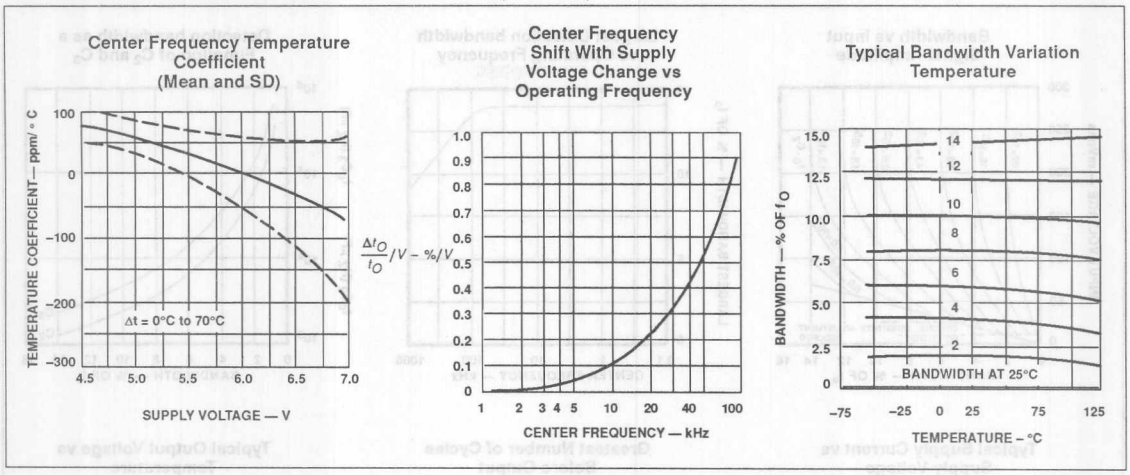
Typical Frequency Drift With Temperature (Mean and SD)



Typical Frequency Drift With Temperature (Mean and SD)



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



DESIGN FORMULAS

$$f_O \approx \frac{1}{1.1 R_1 C_1}$$

$$BW \approx 1070 \sqrt{\frac{V_I}{f_O C_2}} \text{ in \% of } f_O$$

$$V_I \leq 200 mV_{RMS}$$

Where
V_I=Input voltage (V_{RMS})
C_2=Low-pass filter capacitor (μF)

PHASE-LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (f_O)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_O, within which an input signal above the threshold voltage (typically 20mV_{RMS}) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

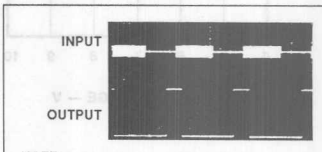
A measure of how well the detection band is centered about the center frequency, f_O. The skew is defined as $(f_{MAX}+f_{MIN}-2f_O)/2f_O$ where fmax and fmin are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

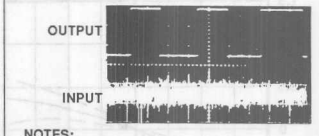
1. Select R1 and C1 for the desired center frequency. For best temperature stability, R1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R1C1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.
2. Select the low-pass capacitor, C2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude Variation is known, the appropriate value of fOC2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C2 may be adjusted accordingly. For example, constand bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the fOC2 product (fO (Hz), C2(μF)).

TYPICAL RESPONSE



NOTE:
R_L = 100Ω

Response to 100mV_{RMS} Tone Burst



NOTES:
S/N = −6dB
R_L = 100Ω
Noise Bandwidth = 140Hz

Response to Same Input Tone Burst With Wideband Noise

3. The value of C3 is generally non-critical. C3 sets the band edge of a low-pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

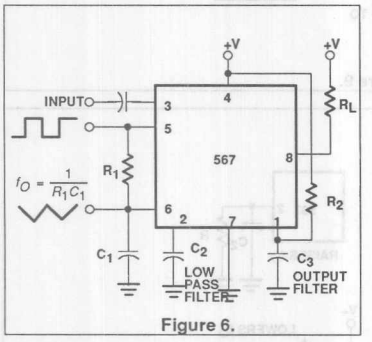


Figure 6.

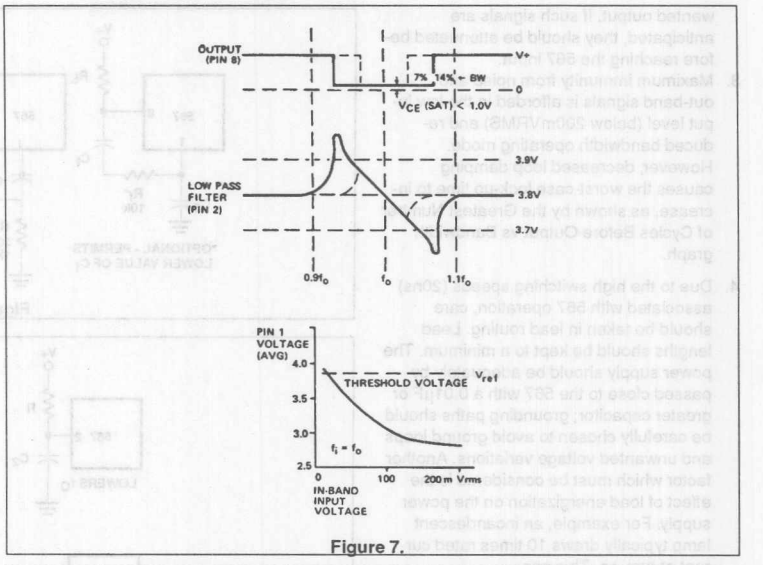


Figure 7.

4. Optional resistor R2 sets the threshold for the largest "no output" input voltage. A value of 130kΩ is used to assure the tested limit of 10mVRMS min. This resistor can be referenced to ground for increased sensitivity. The explanation can be found in the "optional controls" section which follows.

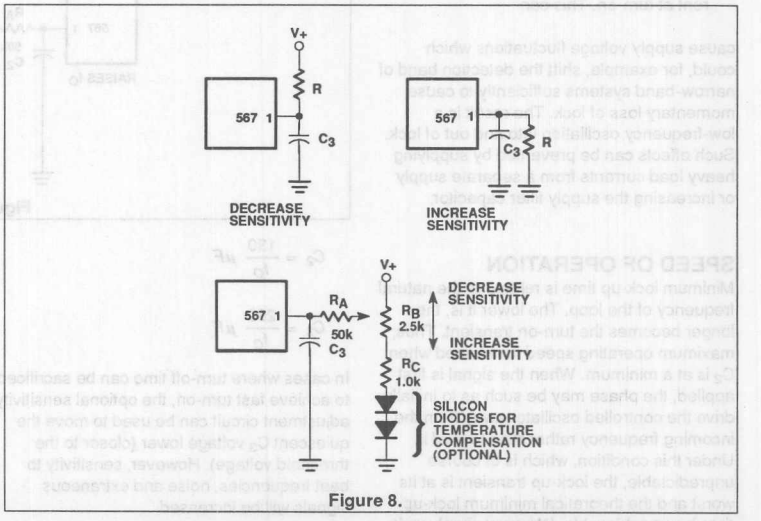


Figure 8.

AVAILABLE OUTPUTS

(Figure 2)

The primary output is the uncommitted output transistor collector, Pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at Pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_O with a slope of about 20mV per percent of frequency deviation. The average voltage at Pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{BE}) \cong (+V - 1.4V)$ having a DC average of +V/2. A 1kΩ load may be driven from pin 5. Pin 6 is an exponential triangle of $1V_{P\text{-}P}$ with an average DC level of +V/2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the inband signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at fO/3, fO/5, etc.
2. The 567 will lock onto signals near (2n+1) fO, and will give an output for signals near (4n+1) fO where n=0, 1, 2, etc. Thus, signals at 5fO and 9fO can cause an un-

wanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.

3. Maximum immunity from noise and out-band signals is afforded in the low input level (below 200mVRMS) and reduced bandwidth operating mode. However, decreased loop damping causes the worst-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can

cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

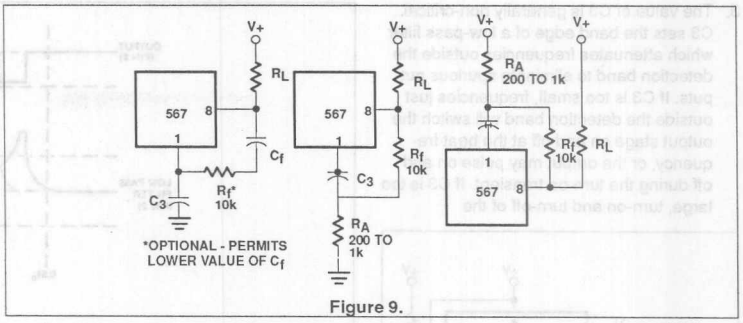


Figure 9.

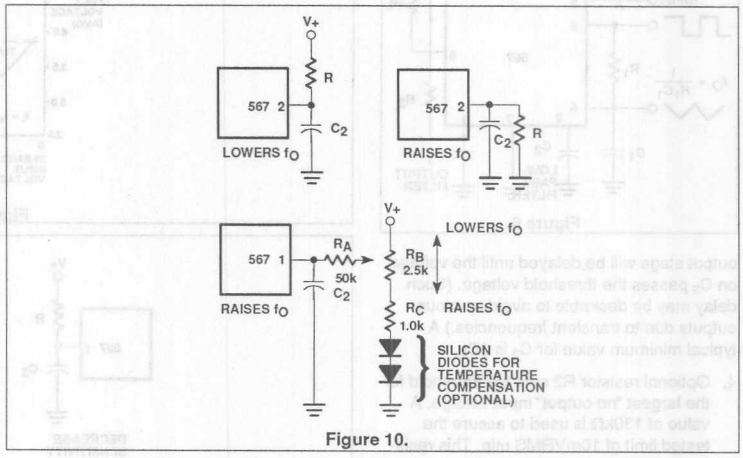


Figure 10.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_O/10$ baud.

$$C_2 = \frac{130}{f_O}\ \mu F$$

$$C_3 = \frac{260}{f_O}\ \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emmitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

SENSITIVITY ADJUSTMENT

(Figure 3)

When operated as a very narrow-band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and out-band signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

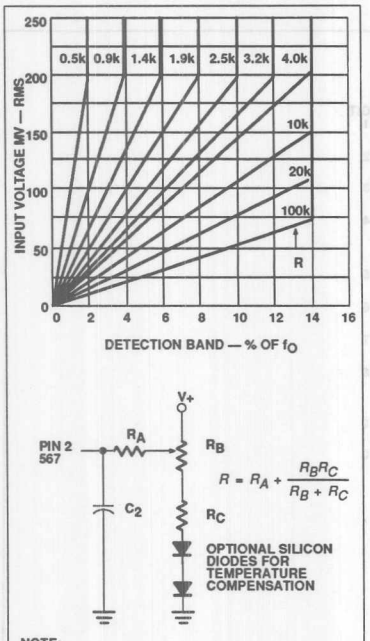


Figure 11.

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the out-band beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

CHATTER PREVENTION

(Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (Pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT

(Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION

(Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between Pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

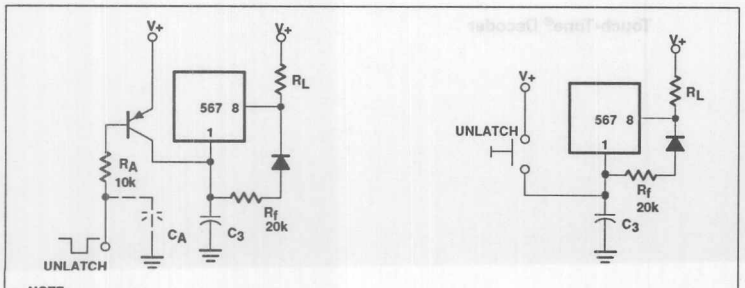
REDUCTION OF C1 VALUE

(Figure 8)

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage-follower between the R_1 C_1 junction and Pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

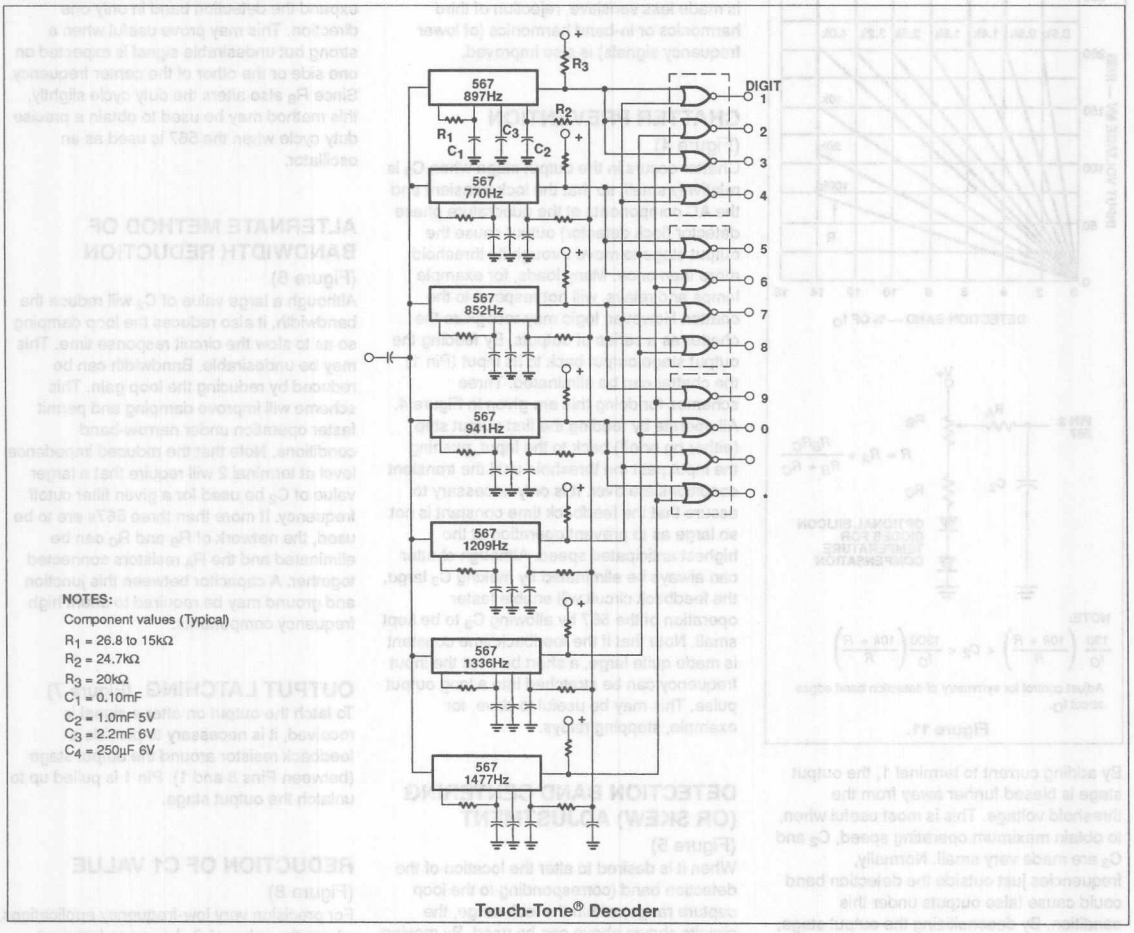
To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating NPN transistors.



NOTE:
C_A prevents latch-up when power supply is turned on.

Figure 12. Output Latching

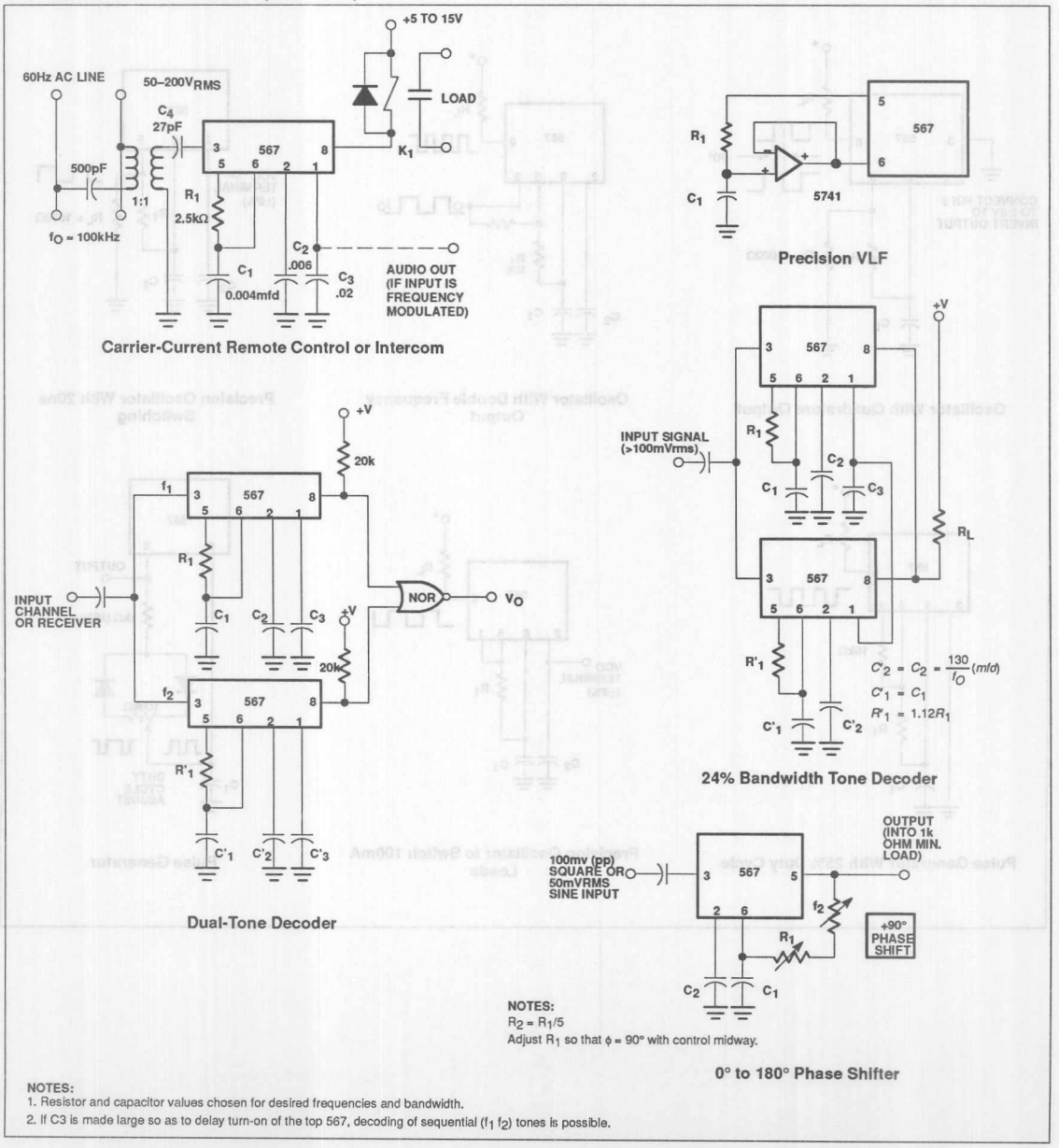
TYPICAL APPLICATIONS



Touch-Tone® Decoder

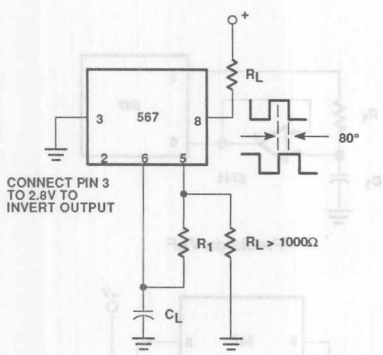
Touch-Tone® Decoder

TYPICAL APPLICATIONS (Continued)

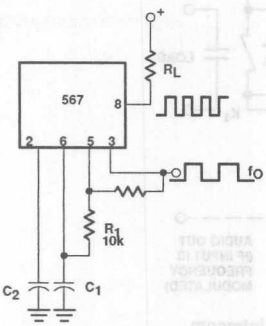


NOTES:
1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1 f_2) tones is possible.

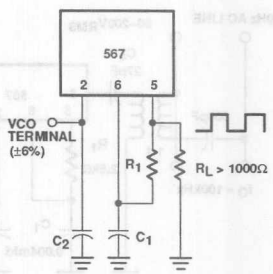
TYPICAL APPLICATIONS (Continued)



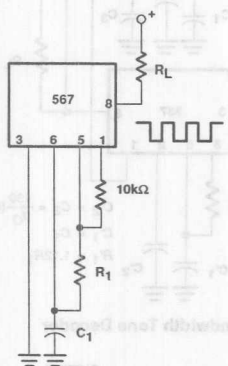
Oscillator With Quadrature Output



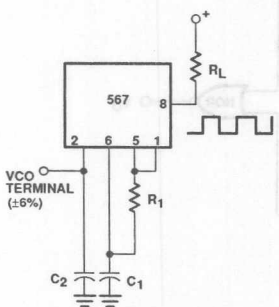
Oscillator With Double Frequency Output



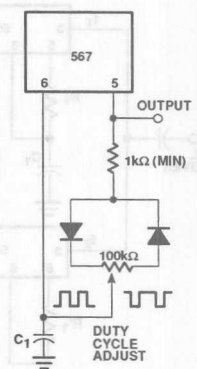
Precision Oscillator With 20ns Switching



Pulse Generator With 25% Duty Cycle



Precision Oscillator to Switch 100mA Loads



Pulse Generator

150MHz phase-locked loop

NE/SA568A

DESCRIPTION

The NE568A is a monolithic phase-locked loop (PLL) which operates from 1Hz to frequencies in excess of 150MHz and features an extended supply voltage range and a lower temperature coefficient of the V_{CO} center frequency in comparison with its predecessor, the NE 568. The NE568A is function and pin-compatible with the NE568, requiring only minor changes in peripheral circuitry (see Figure 1). Temperature compensation network is different, no resistor on Pin 12, needs to be grounded and Pin 13 has a 3.9kΩ resistor to ground. Timing cap, C_2, is different and for 70MHz operation with temperature compensation network should be 16pF, not 34pF as was used in the NE568. The NE568A has the following improvements: ESD protected; extended V_{CC} range from 4.5V to 5.5V; operating temperature range -55 to 125°C (see Signetics Military 568A data sheet); less layout sensitivity; and lower T_C of VCO (center frequency). The integrated circuit consists of a limiting amplifier, a current-controlled oscillator (ICO), a phase detector, a level shift circuit, V/I and I/V converters, an output buffer, and bias circuitry with temperature and frequency compensating characteristics. The design of the NE568A is particularly well-suited for demodulation of FM signals with extremely large deviation in systems which require a highly linear output. In satellite receiver applications with a 70MHz IF, the NE568A will demodulate ±20% deviations with less than 1.0% typical non-linearity. In addition to high linearity, the circuit has a loop filter which can be configured with series or shunt elements to optimize loop dynamic performance. The NE568A is available in 20-pin dual in-line and 20-pin SO (surface mounted) plastic packages.

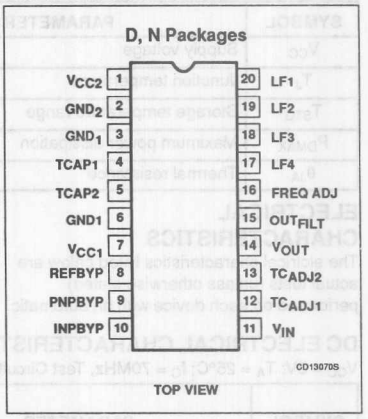
FEATURES

- Operation to 150MHz
- High linearity buffered output
- Series or shunt loop filter component capability
- External loop gain control
- Temperature compensated
- ESD protected[1]

APPLICATIONS

- Satellite receivers
- Fiber optic video links
- VHF FSK demodulators
- Clock Recovery

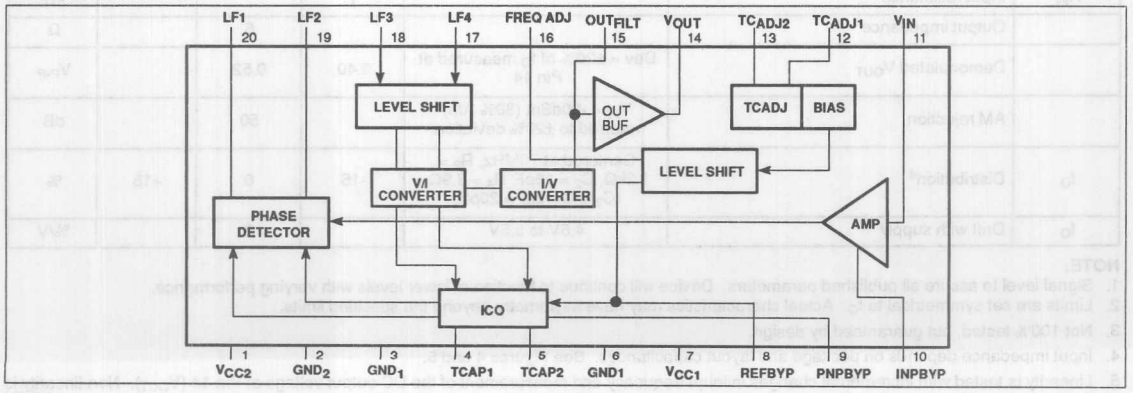
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL	0 to +70°C	NE568AD
20-Pin Plastic DIP	0 to +70°C	NE568AN
20-Pin Plastic SOL	-40 to +85°C	SA568AD
20-Pin Plastic DIP	-40 to +85°C	SA568AN

BLOCK DIAGRAM



NOTE:

1. Pins 4 and 5 can tolerate 1000V only, and all other pins, greater than 2000V for ESD (human body model).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	6	V
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
P_{DMAX}	Maximum power dissipation	400	mW
θ_{JA}	Thermal resistance	80	°C/W

ELECTRICAL CHARACTERISTICS

The elctrical characteristics listed below are actual tests (unless otherwise stated) performed on each device with an automatic IC tester prior to shipment. Performance of the device in automated test set-up is not necessarily optimum. The NE568A is layout-sensitive. Evaluation of performance for correlation to the data sheet should be done with the circuit and layout of Figures 1-3 with the evaluation unit soldered in place. (Do not use a socket!)

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V; T_A = 25°C; f_O = 70MHz, Test Circuit Figure 1, f_{IN} = -20dBm, R_4 = 3.9kΩ, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA568A			
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
I_{CC}	Supply current			54	70	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA568A			
			MIN	TYP	MAX	
f_{OSC}	Maximum oscillator operating frequency[3]		150			MHz
	Input signal level		50 −20[1]		2000 +10	mV_{P-P} dBm
BW	Demodulated bandwidth			$f_O/7$		MHz
	Non-linearity[5]	Dev = ±20%, Input = -20dBm		1.0	4.0	%
	Lock range[2]	Input = -20dBm	±25	±35		% of f_O
	Capture range[2]	Input = -20dBm	±20	±30		% of f_O
	TC of f_O	Figure 1		100		ppm/°C
R_{IN}	Input resistance[4]		1			kΩ
	Output impedance			6		Ω
	Demodulated V_{OUT}	Dev = ±20% of f_O measured at Pin 14	0.40	0.52		V_{P-P}
	AM rejection	V_{IN} = -20dBm (30% AM) referred to ±20% deviation		50		dB
f_O	Distribution[6]	Centered at 70MHz, R_2 = 1.2kΩ, C_2 = 16pF, R_4 = 3.9Ω (C_2 + C_{STRAY} = 20pF)	-15	0	+15	%
f_O	Drift with supply	4.5V to 5.5V		2		%/V

NOTE:

1. Signal level to assure all published parameters. Device will continue to function at lower levels with varying performance.
2. Limits are set symmetrical to f_O. Actual characteristics may have asymmetry beyond the specified limits.
3. Not 100% tested, but guaranteed by design.
4. Input impedance depends on package and layout capacitances. See Figures 4 and 5.
5. Linearity is tested with incremental changes in inupt frequency and measurement of the DC output voltage at Pin 14 (V_{OUT}). Non-linearity is then calculated from a straight line over the deviation range specified.
6. Free-running frequency is measured as feedthrough to Pin 14 (V_{OUT}) with no input signal applied.

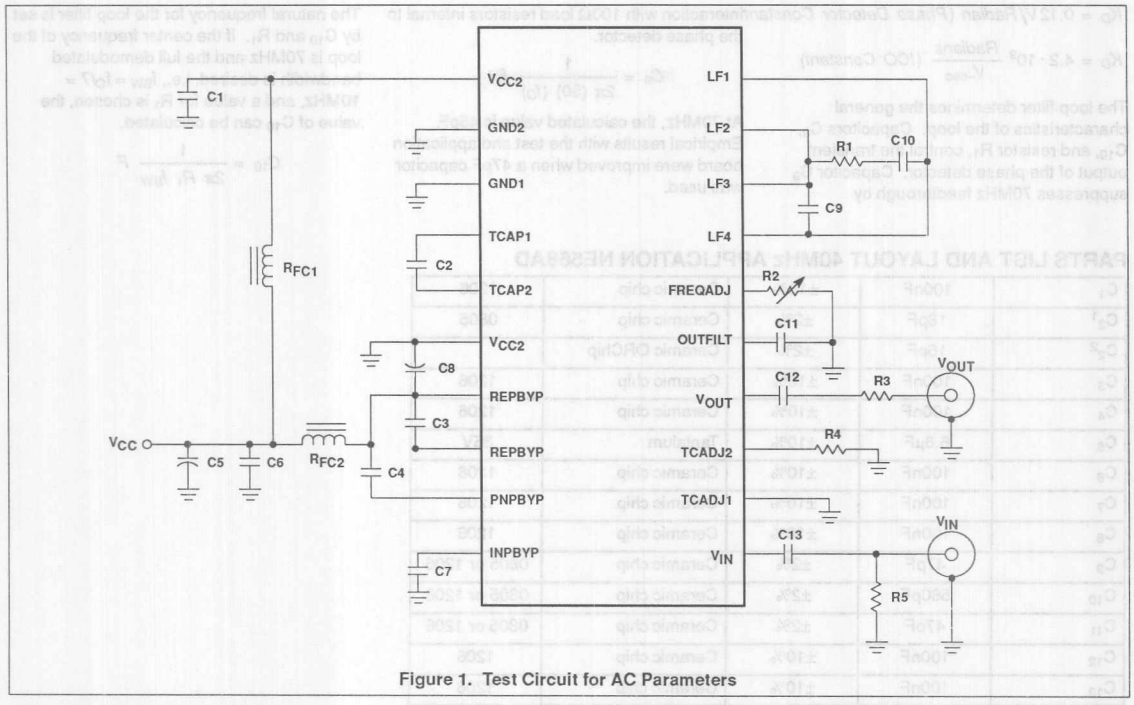


Figure 1. Test Circuit for AC Parameters

FUNCTIONAL DESCRIPTION

The NE568A is a high-performance phase-locked loop (PLL). The circuit consists of conventional PLL elements, with special circuitry for linearized demodulated output, and high-frequency performance. The process used has NPN transistors with f_T > 6GHz. The high gain and bandwidth of these transistors make careful attention to layout and bypass critical for optimum performance. The performance of the PLL cannot be evaluated independent of the layout. The use of the application layout in this data sheet and surface-mount capacitors are high recommended as a starting point.

The input to the PLL is through a limiting amplifier with a gain of 200. The input of this amplifier is differential (Pins 10 and 11). For single-ended applications, the input must be coupled through a DC-blocking capacitor with low impedance at the frequency of interest. The single-ended input is normally applied to Pin 11 with Pin 10 AC-bypassed with a low-impedance capacitor. The input impedance is characteristically slightly above 500Ω. Impedance match is not necessary, but loading the signal source should be avoided. When the source is 50 or 75Ω, a DC-blocking capacitor is usually all that is needed.

Input amplification is low enough to assure reasonable response time in the case of large signals, but high enough for good AM rejection. After amplification, the input signal drives one port of a multiplier-cell phase detector. The other port is driven by the current-controlled oscillator (ICO). The output of the phase comparator is a voltage proportional to the phase difference of the input and ICO signals. The error signal is filtered with a low-pass filter to provide a DC-correction voltage, and this voltage is converted to a current which is applied to the ICO, shifting the frequency in the direction which causes the input and ICO to have a 90° phase relationship.

The oscillator is a current-controlled multivibrator. The current control affects the charge/discharge rate of the timing capacitor. It is common for this type of oscillator to be referred to as a voltage-controlled oscillator (VCO), because the output of the phase comparator and the loop filter is a voltage. To control the frequency of an integrated ICO multivibrator, the control signal must be conditioned by a voltage-to-current converter. In the NE568A, special circuitry predistorts the control signal to make the change in frequency a linear function over a large control-voltage range.

The free-running frequency of the oscillator depend on the value of the timing capacitor connected between Pins 4 and 5. The value of the timing capacitor depends on internal resistive components and current sources. When R_2 = 1.2kΩ and R_4 = 0Ω, a very close approximation of the correct capacitor value is:

$$C^* = \frac{0.0014}{f_O} F$$

where

$$C^* = C_2 + C_{STRAY}$$

The temperature-compensation resistor, R_4, affects the actual value of capacitance. This equation is normalized to 70MHz. See 8 for correction factors.

The loop filter determines the dynamic characteristics of the loop. In most PLLs, the phase detector outputs are internally connected to the ICO inputs. The NE568A was designed with filter output to input connections from Pins 20 (ϕ DET) to 17 (ICO), and Pins 19 (ϕ DET) to 18 (ICO) external. This allows the use of both series and shunt loop-filter elements. The loop constratints are:

$K_D = 0.12 V/Radian$ (*Phase Detector Constant*

$K_D = 4.2 \cdot 10^9 \frac{Radians}{V\text{-}sec}$ (*ICO Constant*)

The loop filter determines the general characteristics of the loop. Capacitors C_9, C_{10}, and resistor R_1, control the transient output of the phase detector. Capacitor C_9 suppresses 70MHz feedthrough by interaction with 100Ω load resistors internal to the phase detector.

$$C_9 = \frac{1}{2\pi\ (50)\ (f_O)}\ F$$

At 70MHz, the calculated value is 45pF. Empirical results with the test and application board were improved when a 47pF capacitor was used.

The natural frequency for the loop filter is set by C_{10} and R_1. If the center frequency of the loop is 70MHz and the full demodulated bandwidth is desired, i.e., $f_{BW} = f_O/7 =$ 10MHz, and a value for R_1 is chosen, the value of C_{10} can be calculated.

$$C_{10} = \frac{1}{2\pi\ R_1\ f_{BW}}\ F$$

PARTS LIST AND LAYOUT 40MHz APPLICATION NE568AD

C_1	100nF	±10%	Ceramic chip	1206
C_2[1]	18pF	±2%	Ceramic chip	0805
C_2[2]	16pF	±2%	Ceramic ORChip	
C_3	100nF	±10%	Ceramic chip	1206
C_4	100nF	±10%	Ceramic chip	1206
C_5	6.8µF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic chip	1206
C_7	100nF	±10%	Ceramic chip	1206
C_8	100nF	±10%	Ceramic chip	1206
C_9	47pF	±2%	Ceramic chip	0805 or 1206
C_{10}	560pF	±2%	Ceramic chip	0805 or 1206
C_{11}	47pF	±2%	Ceramic chip	0805 or 1206
C_{12}	100nF	±10%	Ceramic chip	1206
C_{13}	100nF	±10%	Ceramic chip	1206
R_1	27Ω	±10%	Chip CR32	1/4W
R_2	1.2kΩ		Trim pot	
R_3[3]	43Ω	±10%	Chip CR32	1/4W
R_4[4]	3.9kΩ	±10%	Chip CR32	1/4W
R_5[3]	50Ω	±10%	Chip CR32	1/4W
RFC_1[5]	10µH	±10%	Surface mount	
RFC_2[5]	10µH	±10%	Surface mount	

NOTES:
1. 18pF with Pin 12 ground and Pin 13 no connect (open).
2. $C_2 + C_{STRAY} = 16pF$ for temperature-compensated configuration with $R_4 = 3.9k\Omega$.
3. For 50Ω setup. $R_1 = 62\Omega$, $R_3 = 75\Omega$ for 75Ω application.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 18pF$.
5. 0Ω chip resistors (jumpers) may be substituted with minor degradation of performance.

PARTS LIST AND LAYOUT 70MHz APPLICATION NE568AN

C_1	100nF	±10%	Ceramic chip	50V
C_2[1]	18pF	±2%	Ceramic chip	50V
C_2[2]	16pF	±2%	Ceramic chip	0805
C_3	100nF	±10%	Ceramic chip	50V
C_4	100nF	±10%	Ceramic chip	50V
C_5	6.8µF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic chip	50V
C_7	100nF	±10%	Ceramic chip	50V
C_8	100nF	±10%	Ceramic chip	50V
C_9	47pF	±2%	Ceramic chip	50V
C_{10}	560pF	±2%	Ceramic chip	50V
C_{11}	47pF	±2%	Ceramic chip	50V
C_{12}	100nF	±10%	Ceramic chip	50V
C_{13}	100nF	±10%	Ceramic chip	50V
R_1	27Ω	±10%	Ceramic chip CR32	1/4W
R_2	1.2kΩ		Trim pot	
R_3[3]	43Ω	±10%	Ceramic chip CR32	1/4W
R_4[4]	3.9kΩ	±10%	Ceramic chip CR32	1/4W
R_5[3]	50Ω	±10%	Ceramic chip CR32	1/4W
RFC_1	10µH	±10%	Surface mount	
RFC_2	10µH	±10%	Surface mount	

NOTES:
1. 18pF with Pin 12 ground and Pin 13 no connect (open).
2. $C_2 + C_{STRAY} = 16pF$ for temperature-compensated configuration with $R_4 = 3.9k\Omega$.
3. For 50Ω setup. $R_1 = 62\Omega$, $R_3 = 75\Omega$ for 75Ω application.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 18pF$.

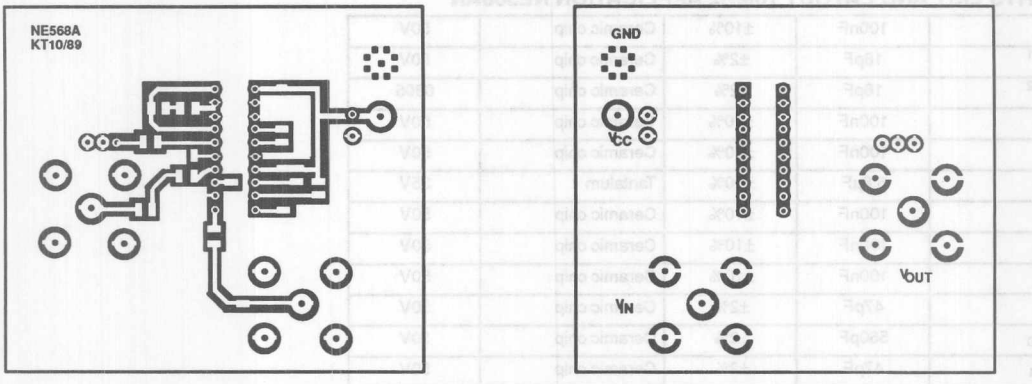


Figure 2. N Package Layout (Not Actual Size)

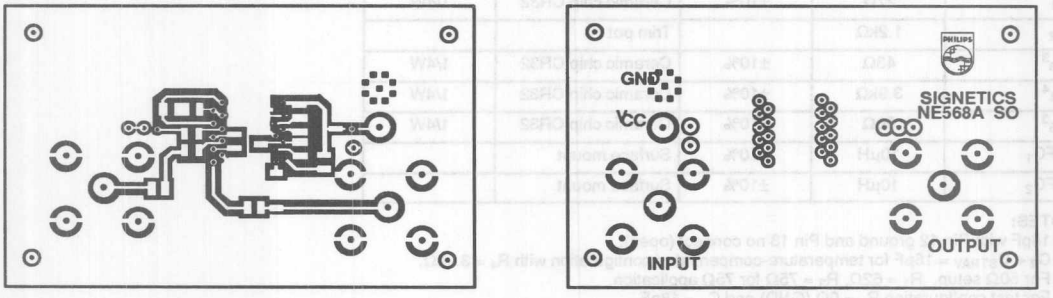


Figure 3. D Package Layout (Not Actual Size)

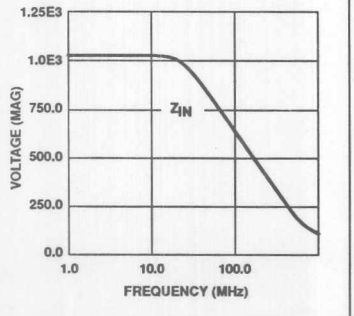


Figure 4. NE568A Input Impedance With CP = 0.5pF 20-Pin SO Package

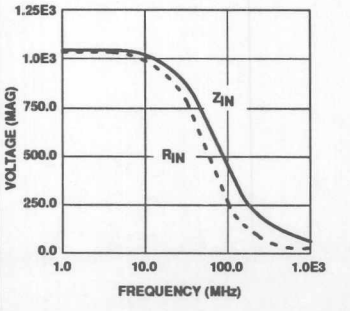


Figure 5. NE568A Input Impedance With CP = 1.49pF 20-Pin Dual In-Line Plastic Package

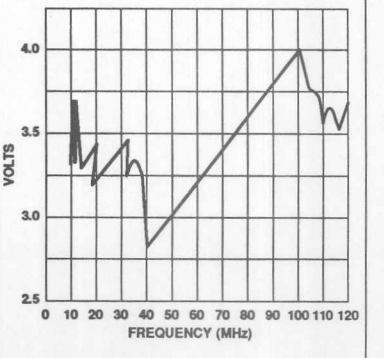


Figure 6. Typical Output Linearity

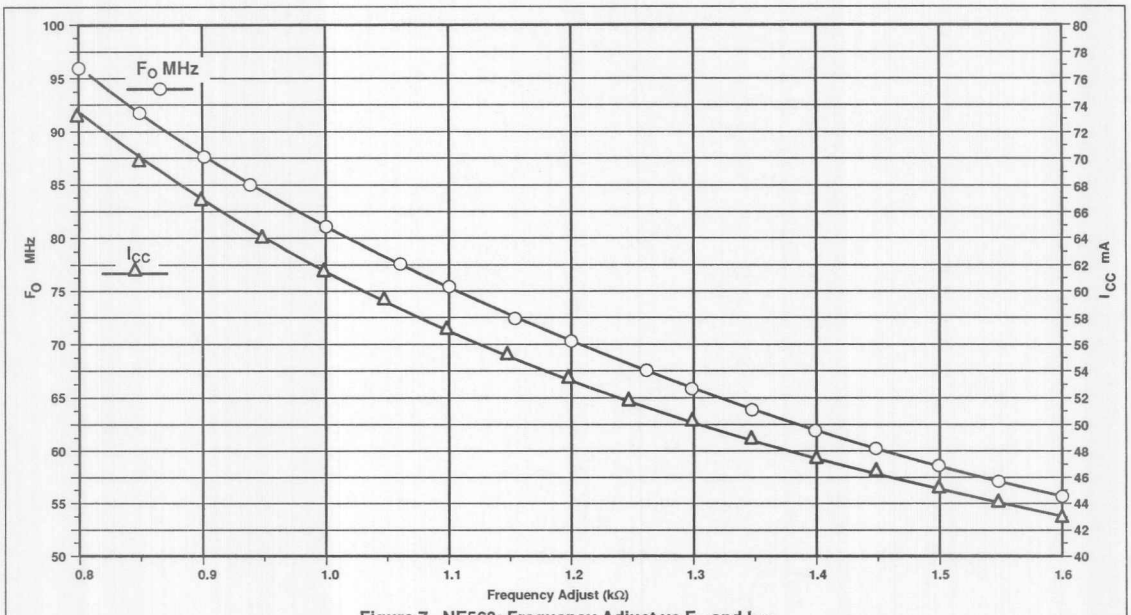


Figure 7. NE568: Frequency Adjust vs F_O and I_{CC}

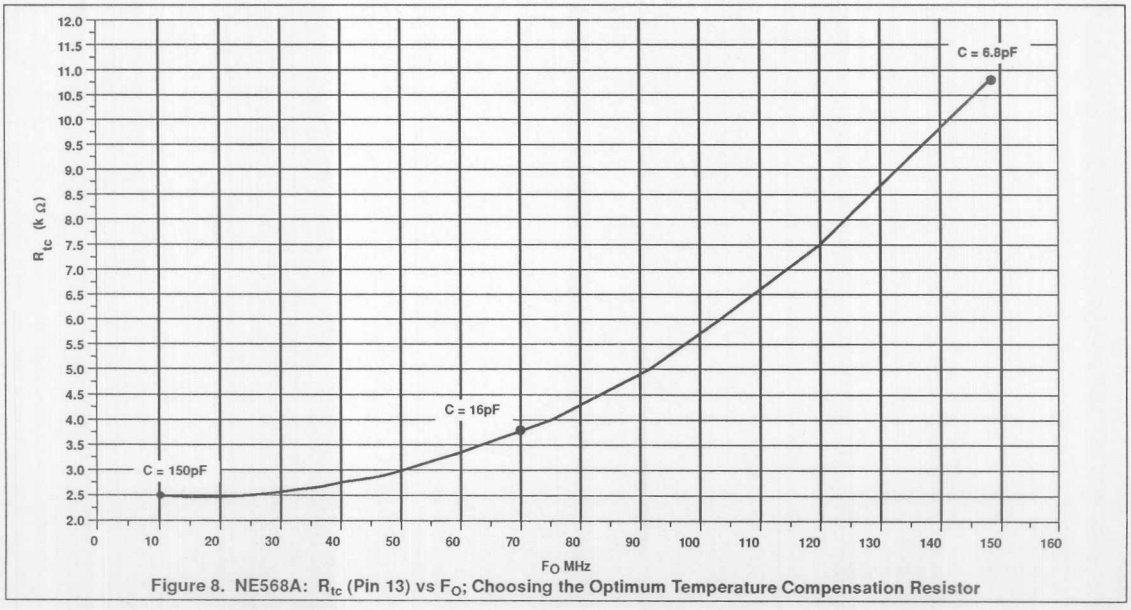
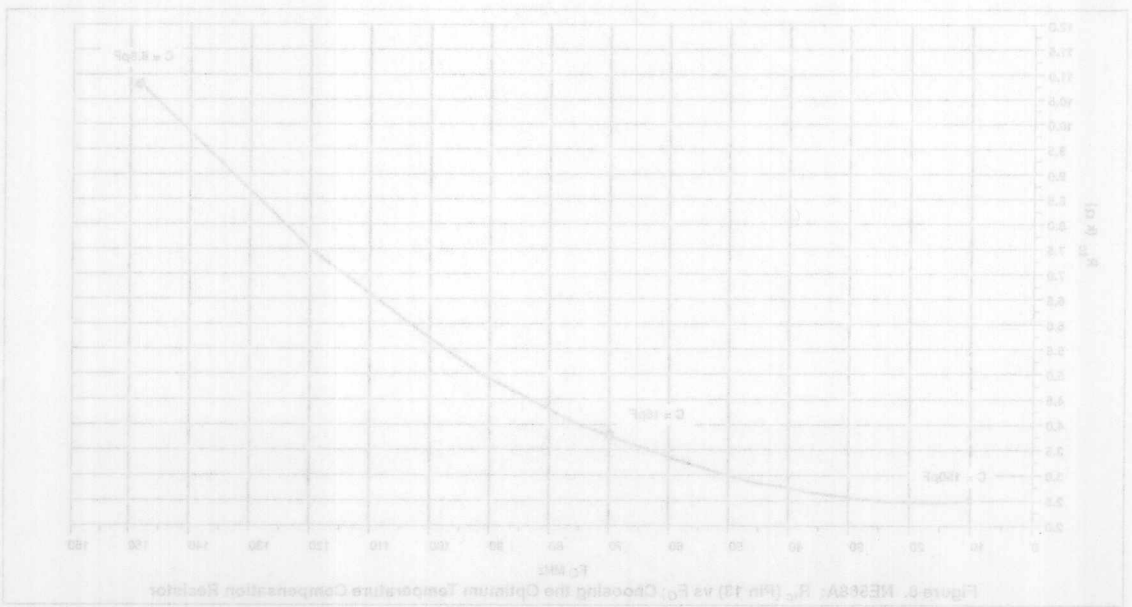


Figure 8. NE568A: R_{tc} (Pin 13) vs F_O; Choosing the Optimum Temperature Compensation Resistor



Section 6
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Section 6
Line Drivers/Receivers, Modems

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NE5170 Octal line driver 300
NE5180/NE5181 Octal differential line receiver 306
AM26LS31 Quad high-speed differential line driver 311
AM26LS32/AM26LS32A Quad high-speed differential line receivers 316
NE5080 Power line modem 320
NE5080 High-speed FSK modem transmitter 328
NE5081 High -speed FSK modem receiver 330

EIA-232-D/V.28 driver/receiver MC145406

DESCRIPTION

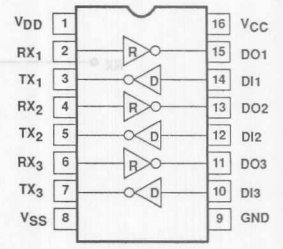
The MC145406 is a silicon-gate CMOS IC that combines 3 drivers and 3 receivers to fulfill the electrical specifications of standards EIA-232-D and CCITT V.28. The drivers feature true TTL input compatibility, slew-rate limited output, 300Ω power-off source impedance, and output typically switching to within 25% of the supply rails. The receivers can handle up to ±25V while presenting 3 to 7kΩ impedance. Hysteresis in the receiver aids reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, the MC145406 provides efficient, low-power solutions for EIA-232-D and V.28 applications.

FEATURES

- **Drivers**
- ±5 to ±12V supply range
- 300Ω power-off source impedance
- Output current limiting
- TTL compatible
- Maximum slew rate = 30V/µs
- **Receivers**
- ±25V input voltage range over the full supply range
- 3 to 7kΩ input impedance
- Hystersis on input switchpoint
- **General**
- Very low supply currents for long battery life
- Operation is independent of power supply sequencing

PIN CONFIGURATION

D and N Packages



NOTE:
D = Driver
R = Receiver

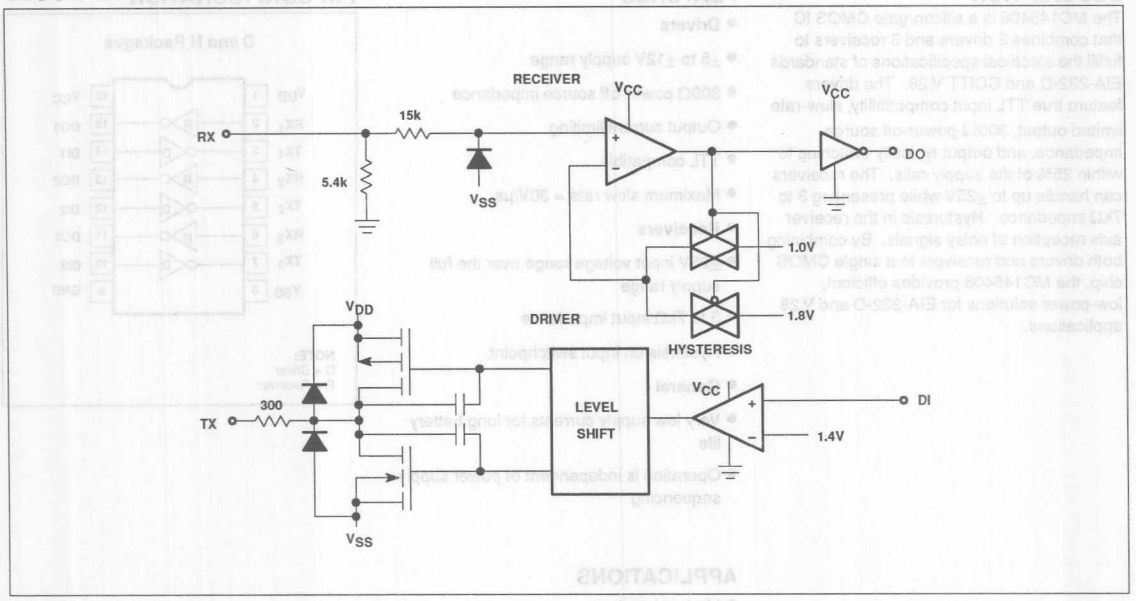
APPLICATIONS

- Modem interface
- Voice/data telephone interface
- Lap-top computers
- UART interface

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	MC145406N
16-Pin SOL	0 to +70°C	MC145406D

BLOCK DIAGRAM



PIN #	SYMBOL	PIN DESCRIPTION
1	V_{DD}	**Positive power supply**. The most positive power supply pin, which is typically 5 to 12 volts.
8	V_{SS}	**Negative power supply.** The most negative power supply pin, which is typically -5 to -12 volts.
16	V_{CC}	**Digital power supply**. The digital supply pin, which is connected to the logic power supply (maximum +5.5V).
9	GND	**Ground.** Ground return pin is typically connected to the signal ground pin of the EIA-232-D connector (Pin 7) as well as to the logic power supply ground.
2, 4, 6	RX_1, RX_2, RX_3	**Receive Data Input.** These are the EIA-232-D receive signal inputs whose voltages can range from +25 to -25V. A voltage between +3 and +25 is decoded as a space and causes the corresponding DO pin to swing to ground (0V); a voltage between -3 and -25V is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn-on input switchpoint is typically biased at 1.8V above ground, and includes 800mV of hysteresis for noise rejection. The nominal input impedance is 5kΩ. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.
11, 13, 15	DO1, DO2, DO3	**Data Output.** These are the receiver digital output pins, which swing from V_{CC} to GND. A space on the RX pin causes DO to produce a logic zero; a mark produces a logic one. Each output pin is capable of driving one LSTTL input load.
10, 12, 14	DI1, DI2, DI3	**Data Input.** These are the high-impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4V above ground. However, 5V CMOS compatibility is maintained as well. Input voltage levels on these pins must be between V_{CC} and GND.
3, 5, 7	TX1, TX2, TX3	**Transmit Data Output.** These are the EIA-232-D transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic one at a DI input causes the corresponding TX output to swing toward V_{SS}. A logic zero causes the output to swing toward V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30V/µs. When the MC145406 is off (V_{DD} = V_{SS} = V_{CC} = GND), the minimum output impedance is 300Ω.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +6.0	V
V_{DD}	Supply voltage	-0.5 to +13.5	V
V_{SS}	Supply voltage	+0.5 to -13.5	V
V_{IR}	Input voltage range RX_{1-3} inputs DI_{1-3} inputs	 $(V_{SS} - 15)$ to $(V_{DD} + 15)$ -0.5 to $(V_{CC} + 0.5)$	V
	DC current per pin	±100	mA
P_D	Power dissipation (package)	1.0	W
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
θ_{JA}	Thermal impedance N package D package	80 105	°C/W

NOTE: This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range $GND \leq V_{DI} \leq V_{DD}$ and $GND \leq V_{DO} \leq V_{CC}$. Also, the voltage at the RX pin should be constrained to ±25V, and TX should be constrained to $V_{SS} \leq V_{TX1-3} \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and V_{SS} or V_{DD} for RX).

DC ELECTRICAL CHARACTERISTICS

Typical values are at $T_A = 0$ to 70°C; GND = 0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DC supply voltage						
V_{DD}			4.5	5 to 12	13.2	V
V_{SS}			-4.5	-5 to -12	-13.2	V
V_{CC}			4.5	5.0	5.5	V
Quiescent supply current (outputs unloaded, inputs low)						
I_{DD}		$V_{DD} = +12V$		20	400	µA
I_{SS}		$V_{SS} = -12V$		280	600	µA
I_{CC}		$V_{CC} = +5V$		260	450	µA

RECEIVER ELECTRICAL CHARACTERISTICS

Typical values are at $T_A = 0$ to 70°C; GND = 0V; V_{DD} = +5 to +12V; V_{SS} = -5 to -12V; V_{CC} = +5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
V_{ON}	Input turn-on threshold	RX_{1-3}	$V_{DO1-3} = V_{OL}$, V_{CC} = 5.0V ±5%	1.35	1.80	2.35	V
V_{OFF}	Input turn-off threshold	RX_{1-3}	$V_{DO1-3} = V_{OH}$, V_{CC} = 5.0V ±5%	0.75	1.00	1.25	V
V_{ON}-V_{OFF}	Input threshold hysteresis	RX_{1-3}	V_{CC} = 5.0V ±5%	0.6	0.8		V
R_{IN}	Input resistance	RX_{1-3}	$(V_{SS}$-15V) ≤ V_{RX1-3} ≤ $(V_{DD}$+15V)	3.0	5.0	7.0	kΩ
V_{OH}	High level output voltage V_{RX1-3} = -3V to $(V_{SS}$-15V)[1]	DO_{1-3}	I_{OH} = -20µA, V_{CC} = +5.0V	4.9	5.0		V
			I_{OH} = -1mA, V_{CC} = +5.0V	3.8	4.4		V
V_{OL}	Low level output voltage V_{RX1-3} = +3V to $(V_{DD}$+15V)[1]	DO_{1-3}	I_{OL} = +20µA, V_{CC} = +5.0V		0.005	0.1	V
			I_{OL} = +2mA, V_{CC} = +5.0V		0.15	0.5	V
			I_{OL} = +4mA, V_{CC} = +5.0V		0.3	0.7	V

NOTE:
1. This is the range of input voltages as specified by EIA-232-D to cause a receiver to be in the high or low logic state.

DRIVER ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V; V_{CC} = +5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
V_{IL}	Digital input voltage	DI_{1-3}	Logic 0			0.8	V
V_{IH}	Digital input voltage	DI_{1-3}	Logic 1	2.0			V
I_{IN}	Input current	DI_{1-3}	V_{DI1-3} = V_{CC}			±1.0	µA
V_{OH}	Output high voltage V_{DI1-3} = Logic 0, R_L = 3.0kΩ	TX_{1-3}	V_{DD} = +5.0V, V_{SS} = -5.0V	3.5	4.1		V
			V_{DD} = +6.0V, V_{SS} = -6.0V	4.3	5.0		V
			V_{DD} = +12.0V, V_{SS} = -12.0V	9.2	10.4		V
V_{OL}	Output low voltage[1] V_{DI1-3} = Logic 0, R_L = 3.0kΩ	TX_{1-3}	V_{DD} = +5.0V, V_{SS} = -5.0V	-4.0	-4.3		V
			V_{DD} = +6.0V, V_{SS} = -6.0V	-4.5	-5.2		V
			V_{DD} = +12.0V, V_{SS} = -12.0V	-10.0	-10.3		V
	Off source resistance Figure 1	TX_{1-3}	V_{DD}=V_{SS}=GND=0V, V_{TX1-3} = ±2.0V	300			Ω
I_{SC}	Output short-circuit current V_{DD} = +12.0V, V_{SS} = -12.0V	TX_{1-3}	TX_{1-3} shorted to GND[2]		±22	+60	mA
			TX_{1-3} shorted to ±15.0V[3]		±60	±100	mA

NOTE:

1. The voltage specifications are in terms of absolute values.
2. Specification is for one TX output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.
3. This condition could exceed package limitations.

SWITCHING CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; V_{CC} = +5V ±5%, unless otherwise specified. (See Figures 2 and 3)

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
Drivers							
t_{PLH}	Propagation delay time	TX_{1-3}	Low-to-High R_L = 3kΩ, C_L = 50pF		300	500	ns
t_{PHL}	Propagation delay time	TX_{1-3}	High-to-Low R_L = 3kΩ, C_L = 50pF		300	500	ns
SR	Output slew rate (minimum load)	TX_{1-3}	R_L = 7kΩ, C_L = 0pF, V_{DD} = 6 to 12.0V, V_{SS} = -6 to -12V		±6	±30	V/µs
	Output slew rate (maximum load)	TX_{1-3}	R_L = 7kΩ, C_L = 2500pF, V_{DD} = 12V, V_{SS} = -12V		±3.0		V/µs
Receivers (C_L = 50pF)							
t_{PLH}	Propagation delay time	DO_{1-3}	Low-to-High		150	425	ns
t_{PHL}	Propagation delay time	DO_{1-3}	High-to-Low		150	425	ns
t_R	Output rise time	DO_{1-3}			120	400	ns
t_F	Output fall time	DO_{1-3}			40	100	ns

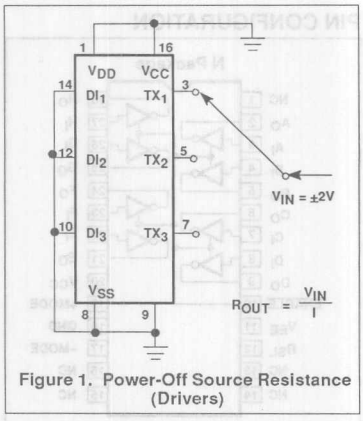


Figure 1. Power-Off Source Resistance (Drivers)

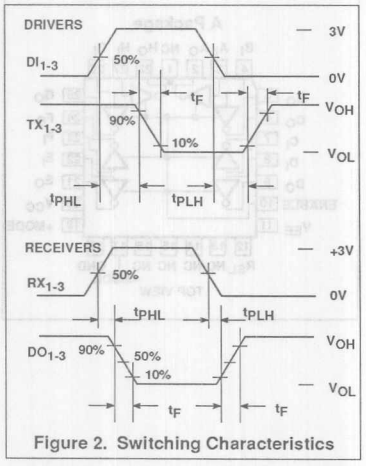


Figure 2. Switching Characteristics

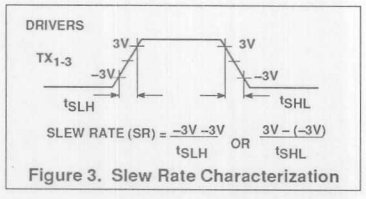


Figure 3. Slew Rate Characterization

APPLICATIONS INFORMATION

The MC145406 has been designed to meet the electrical specifications of standards EIA-232-D/CCITT V.28 and as such, defines the elctrical and physical interface between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). A DCE is connected to a DTE using a cable that typically carries up to 25 leads, which allow the transfer of timing, data, control, and test signals. The MC145406 provides the necessary level shifting between the TTL/CMOS logic levels and the high voltage levels of EIA-232-D (ranging from ±3 to ±25V).

DRIVERS

As defined by the specification, an EIA-232-D driver presents a voltage of between ±5 to ±15V into a load of between 3 to 7kΩ. A logic one at the driver input results in a voltage of between -5 to -15V. A logic zero results in a voltage between ±5 to ±15V. When operating at ±7 to ±12V, the MC145406 meets this requirement. When operating at ±5V, the MC145406 drivers produce less than ±5V at the output (when terminated), which does not meet the EIA-232-D specification. However, the output voltages when using a ±5V power supply are high enough (around ±4V) to permit proper reception by an EIA-232-D receiver, and can be used in applications where strict compliance to EIA-232-D is not required.

Another requirement of the MC145406 drivers is that they withstand a short to another driver in the EIA-232-D cable. The worst-case condition that is permitted by EIA-232-D is a ±15V source that is current limited to 500mA. The MC145406 drivers can withstand this condition momentarily. In most short circuit conditions the source driver will have a series 300Ω output impedance needed to satisfy the EIA-232-D driver requirements. This will reduce the short circuit current to under 40mA which is an acceptable level for the MC145406 to withstand.

Unlike some other drivers, the MC145406 drivers feature an internally-limited output slew rate that does not exceed 30V/µs.

RECEIVERS

The job of an EIA-232-D receiver is to level-shift voltages in the range of -25 to +25V down to TTL/CMOS logic levels (0 to +5V). A voltage of between -3 and -25V on RX_1 is defined as a mark and produces a logic one at DO_1. A voltage between +3 and +25V is a space and produces a logic zero. While receiving these signals, the RX inputs must present a resistance between 3 and 7kΩ. Nominally, the input resistance of the RX_{1-3} inputs is 5.0kΩ.

The input threshold of the RX_{1-3} inputs is typically biased at 1.8V above ground (GND) with typically 800mV of hysteresis included to improve noise immunity. The 1.8V bias forces the appropriate DO pin to a logic one when its RX input is open or grounded as called for in EIA-232-D specification. Notice that TTL logic levels can be applied to the RX inputs in lieu of normal EIA-232-D signal levels. This might be helpful in situations where access to the modem or computer through the EIA-232-D connector is necessary with TTL devices. However, it is important not to connect the EIA-232-D outputs (TX_1) to TTL inputs since TTL operates off +5V only, and may be damaged by the high output voltage of the MC145406.

The DO outputs are to be connected to a TTL or CMOS input (such as an input to a modem chip). These outputs will swing from V_{CC} to ground, allowing the designer to operate the DO and DI pins from the digital power supply. The TX and RX sections are independently powered by V_{DD} and V_{SS} so that one may run logic at +5V and the EIA-232-D signals at ±12V.

Octal line driver

NE5170

DESCRIPTION

The NE5170 is an octal line driver which is designed for digital communications with data rates up to 100kb/s. This device meets all the requirements of EIA standards RS-232C/RS-423A and CCITT recommendations V.10/X.26. Three programmable features: (1) output slew rate, (2) output voltage level, and (3) three-state control (high-impedance) are provided so that output characteristics may be modified to meet the requirements of specific applications.

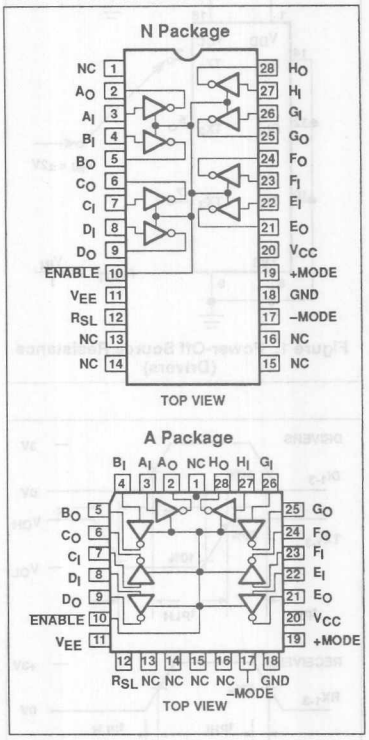
FEATURES

- Meets EIA RS-232C/423A and CCITT V.10/X.26
- Simple slew rate programming with a single external resistor
- 0.1 to 10V/µs slew rate range
- High/low programmable voltage output modes
- TTL compatible inputs

APPLICATIONS

- High-speed modems
- High-speed parallel communications
- Computer I/O ports
- Logic level translation

PIN CONFIGURATION



FUNCTION TABLE

ENABLE	Logic Input	OUTPUT VOLTAGE (V)		
		RS-423A[1]	RS-232C	
			Low Output Mode[1]	High Output Mode[3]
L	L	5 to 6V	5 to 6V	≥ 9V
L	H	–5 to 6V	–5 to 6V	≤ –9V
H	X	High-Z	High-Z	High-Z

NOTES:
1. V_{CC} = +10V and V_{EE} = –10V; R_L = 3kΩ
2. V_{CC} = +12V and V_{EE} = –12V; R_L = 3kΩ

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	0 to +70°C	NE5170N
28-Pin PLCC	0 to +70°C	NE5170A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage and + MODE	15	V
V_{EE}	Supply voltage and – MODE	–15	V
I_{OUT}	Output current[1]	±150	mA
V_{IN}	Input voltage ($\overline{\text{Enable}}$, Data)	–1.5 to +7	V
V_{OUT}	Output voltage[2]	±15	V
	Minimum slew resistor[3]	1	kΩ
P_D	Power dissipation	1200	mW

NOTES:
1. Maximum current per driver. Do not exceed maximum power dissipation if more than one output is on.
2. High impedance mode.
3. Minimum value of the resistor used to set the slew rate.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ±10%; V_{EE} = –10V ±10%; ±MODES = 0V; R_{SL} = 2kΩ, 0°C ≤ T_A ≤ 70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{OH}	Output high voltage	V_{IN} = 0.8V R_L = 3kΩ[2]	5	6	V
		R_L = 450Ω[2]	4.5	6	
		R_L = 3kΩ[3], C_L = 2500pF	V_{CC}–3		
V_{OL}	Output low voltage	V_{IN} = 2.0V R_L = 3kΩ[2]	–6	–5	V
		R_L = 450Ω[2]	–6	–4.5	
		R_L = 3kΩ[3], C_L = 2500pF		V_{EE}+3	
V_{OU}	Output unbalance voltage	V_{CC} = |V_{EE}|, R_L = 450Ω[2]		0.4	V
I_{CEX}	Output leakage current	|V_O| = 6V, ENABLE = 2V or V_{CC} = V_{EE} = 0V	–100	100	µA
V_{IH}	Input high voltage		2.0		V
V_{IL}	Input low voltage			0.8	V
I_{IL}	Logic "0" input current	V_{IN} = 0.4V	–400	0	µA
I_{IH}	Logic "1" input current	V_{IN} = 2.4V	0	40	µA
I_{OS}	Output short circuit current[1]	V_O = 0V	–150	150	mA
V_{CL}	Input clamp voltage	I_{IN} = –15mA	–1.5		V
I_{CC}	Supply current	NO LOAD		35	mA
I_{EE}		NO LOAD	–45		mA

NOTES:
1. Maximum current per driver. Do not exceed maximum power dissipation if more than one output is on.
2. V_{OH}, V_{OL} at R_L = 450Ω will be ≥ 90% of V_{OH}, V_{OL} at R_L = ∞.
3. High Output Mode; +MODE pin = V_{CC}; –MODE pin = V_{EE}; 9V ≤ V_{CC} ≤ 13V; –9V ≥ V_{EE} ≥ –13V.

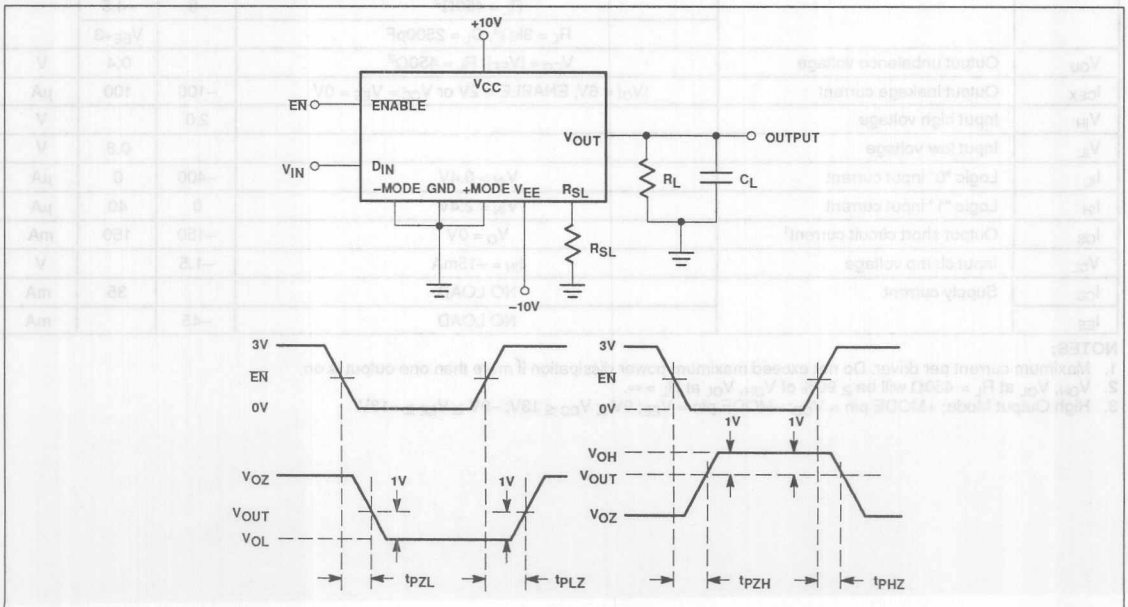
AC ELECTRICAL CHARACTERISTICS

V_{CC} = +10V; V_{EE} = –10V; Mode = GND, 0°C ≤ T_A ≤ 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_{PHZ}	Propagation delay output high to high impedance	R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		5	µs
t_{PLZ}	Propagation delay output low to high impedance	R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		5	µs
t_{PZH}	Propagation delay high impedance to high output	R_{SL} = 200k R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		150	µs
t_{PZL}	Propagation delay high impedance to low output	R_{SL} = 200k R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		150	µs
SR	Output slew rate[1]	R_{SL} = 2k	8	12	V/µs
		R_{SL} = 20k	0.8	1.2	
		R_{SL} = 200k	0.06	0.14	

NOTE:
SR: Load condition. (A) For R_{SL} < 4kΩ use R_L = 450Ω; C_L = 50pF; (B) for R_{SL} > 4kΩ use either R_L = 450Ω, C_L = 50pF or R_L = 3kΩ, C_L = 2500pF.

AC PARAMETER TEST CIRCUIT AND WAVEFORMS



NOTES:
1. See AC electrical characteristics table for values of R_{SL}, R_L and C_L.
2. V_{IN} pulse: Frequency = 1kHz, duty cycle = 50%, Z_{OUT} = 50Ω, $t_r = t_f \leq$ 10ns.

SLEW RATE PROGRAMMING

Slew rate for the NE5170 is set using a single external resistor connected between the R_{SL} pin and ground. Adjustment is made according to the formula:

$$R_{SL}\ (\text{in k}\Omega) = \frac{20}{\text{Slew Rate}}$$

where the slew rate is in V/µs. The slew resistor can vary between 2 and 200kΩ which gives a slew rate range of 10 to 0.1V/µs. This adjustment of the slew rate allows tailoring output characteristics to recommendations for cable length and data rate found in EIA standard RS–423A. Approximations for cable length and data rate are given by:

Max. data rate (in kb/s) = 300/t

Cable length (in feet) = 100×t

where t is the rise time in microseconds. The absolute maximum data rate is 100kb/s and the absolute maximum cable length is 4000 feet.

OUTPUT MODE PROGRAMMING

The NE5170 has two programmable output modes which provide different output voltage levels. The low output mode meets the specifications of EIA standards RS–423A and RS–232C. The high output mode meets the specifications of RS–232C only, since higher output voltages result from programming this mode. The high output mode provides the greater output voltages where higher attenuation levels must be tolerated. Programming the high output mode is accomplished by connecting the +MODE pin to V_{CC} and the –MODE pin to V_{EE}. The low output mode results when both of these pins are connected to ground.

APPLICATION

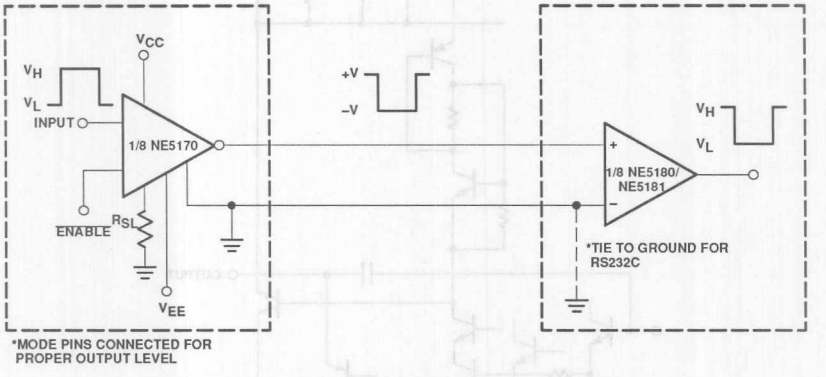


Figure 1. RS-232C/RS-423A Data Transmission

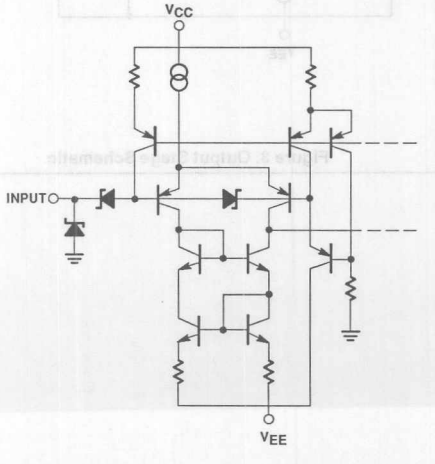


Figure 2. Input Stage Schematic

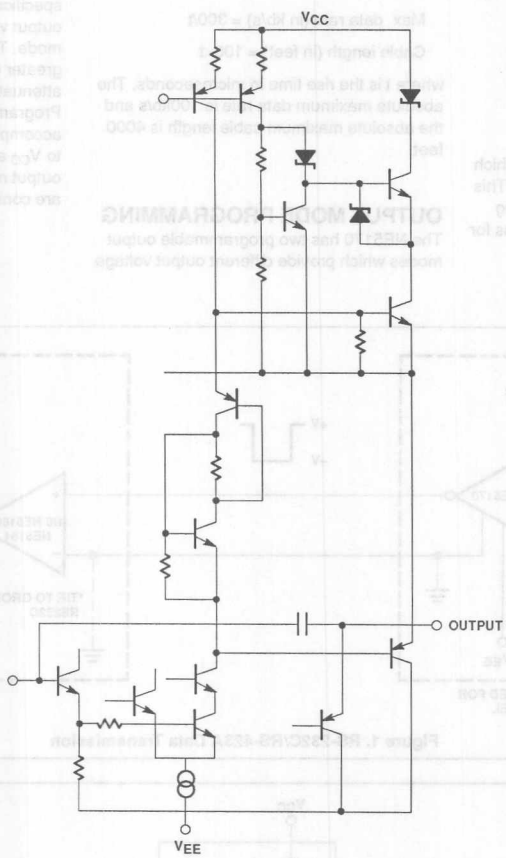


Figure 3. Output Stage Schematic

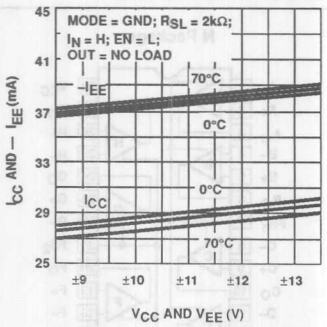


Figure 4. Typical I_{CC} and I_{EE} vs Supply Voltages

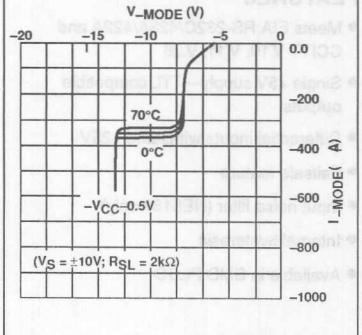


Figure 7. Typical –MODE Current vs –MODE Voltage

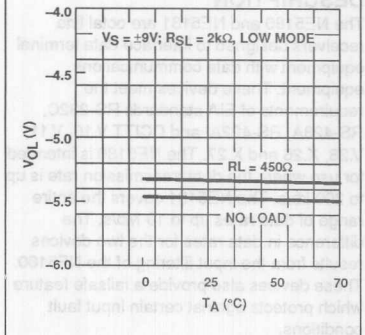


Figure 10. Typical Output Low Voltage vs Temperature

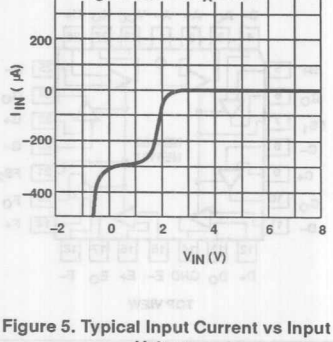


Figure 5. Typical Input Current vs Input Voltage

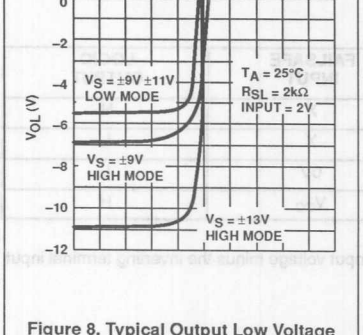


Figure 8. Typical Output Low Voltage vs Load Current

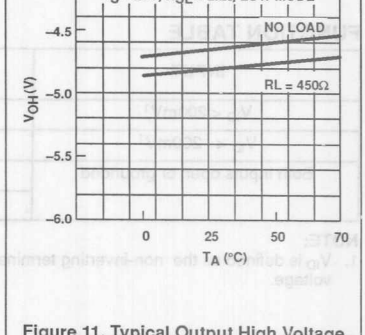


Figure 11. Typical Output High Voltage vs Temperature

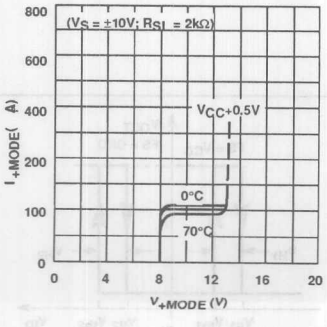


Figure 6. Typical +MODE Current vs +MODE Voltage

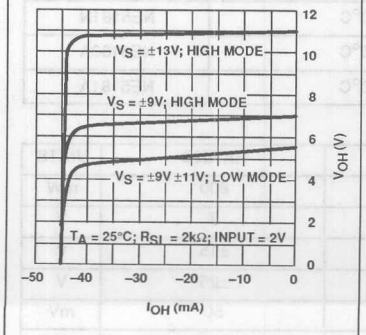


figure 9. Typical Output High Voltage vs Load Current

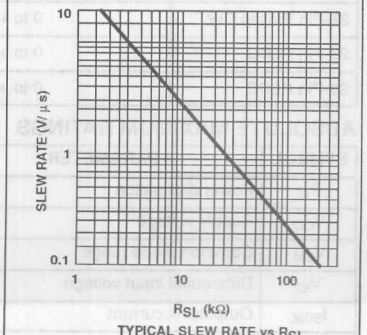


Figure 12. Typical Slew Rate vs R_{SL}

Octal differential line receiver

NE5180/NE5181

DESCRIPTION

The NE5180 and NE5181 are octal line receivers designed to interface data terminal equipment with data communications equipment. These devices meet the requirements of EIA standards RS-232C, RS-423A, RS-422A, and CCITT V.10, V.11, V.28, X.26 and X.27. The NE5180 is intended for use where the data transmission rate is up to 200 kb/s. The NE5181 covers the entire range of data rates up to 10 Mb/s. The difference in data rates for the two devices results from the input filtering of the NE5180. These devices also provide a failsafe feature which protects against certain input fault conditions.

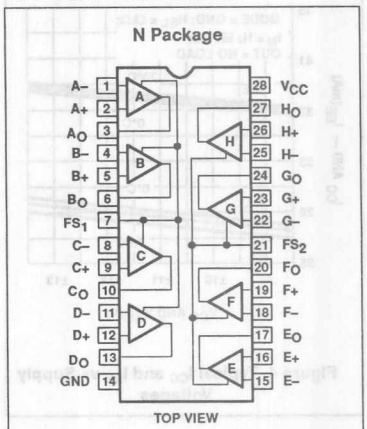
FEATURES

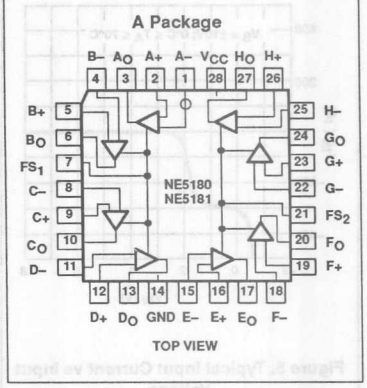
- Meets EIA RS-232C/423A/422A and CCITT V.10, V.11, V.28
- Single +5V supply—TTL compatible outputs
- Differential inputs withstand ±25V
- Failsafe feature
- Input noise filter (NE5180 only)
- Internal hysteresis
- Available in SMD PLCC

APPLICATIONS

- High-speed modems
- High-speed parallel communications
- Computer I/O ports
- Logic level translation

PIN CONFIGURATION





FUNCTION TABLE

INPUT	FAILSAFE INPUT	LOGIC OUTPUT
$V_{ID} < 200mV^1$	X	H
$V_{ID} < -200mV^1$	X	L
Both inputs open or grounded	0V	L
	V_{CC}	H

NOTE:
1. V_{ID} is defined as the non-inverting terminal input voltage minus the inverting terminal input voltage.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
28-Pin Plastic DIP	0 to +70°C	NE5180N
28-Pin Plastic DIP	0 to +70°C	NE5181N
28-Pin PLCC	0 to +70°C	NE5180A
28-Pin PLCC	0 to +70°C	NE5181A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
P_D	Power dissipation	800	mW
V_{CC}	Supply voltage	7	V
V_{CM}	Common mode range	±15	V
V_{ID}	Differential input voltage	±25	V
I_{SINK}	Outputsink current	50	mV
V_{FS}	Failsafe voltage	–0.3 to V_{CC}	V
J_{OS}	Output short-circuit time	1	sec

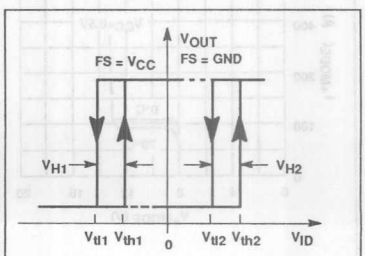


Figure 1. V_{tl}, V_{th}, V_H Definitions

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±5%, 0°C ≤ T_A ≤ +70°C, input common-mode range ±7V

SYMBOL	PARAMETER	TEST CONDITIONS			NE5180 Min	NE5180 Max	NE5181 Min	NE5181 Max	UNIT
R_{IN}	DC input resistance	3V ≤ $\|V_{IN}\|$ ≤ 25V			3	7	3	7	kΩ
V_{OFS}	Failsafe output voltage	Inputs open or shorted to GND	0 ≤ I_{OUT} ≤ 8mA, $V_{failsafe}$ = 0V			0.45		0.45	V
			0 ≥ I_{OUT} ≥ –400µA, $V_{failsafe}$ = V_{CC}		2.7		2.7		
V_{th}	Differential input high[4] threshold	V_{OUT} ≥ 2.7V, I_{OUT} = –440µA		R_S = 0[1]		0.2		0.2	V
				R_S = 500[1]		0.4		0.4	
V_{tl}	Differential input low[4] threshold	V_{OUT} ≤ 0.45V, I_{OUT} = 8mA		R_S = 0[1]	–0.2		–0.2		V
				R_S = 500[1]	–0.4		–0.4		
V_H	Hysteresis[4]	FS = 0V or V_{CC} (See Figure 1)			50	140	50	140	mV
V_{IOC}	Open-circuit input voltage					2		2	V
C_I	Input capacitance					30		30	pF
V_{OH}	High level output voltage	V_{ID} = 1V, I_{OUT} = –440µA			2.7		2.7		V
V_{OL}	Low level output voltage	V_{ID} = –1V		I_{OUT} = 4mA[2]		0.4		0.4	V
				I_{OUT} = 8mA[2]		0.45		0.45	
I_{OS}	Short-circuit output current	V_{ID} = 1V, Note 3			20	100	20	100	mA
I_{CC}	Supply current	4.75V ≤ V_{CC} ≤ 5.25V, V_{ID} = –1V; FS = 0V				100		100	mA
I_{IN}	Input current	Other inputs grounded		V_{IN} = +10V		3.25		3.25	mA
				V_{IN} = –10V	–3.25		–3.25		

NOTES:
1. R_S is a resistor in series with each input.
2. Measured after 100ms warm-up (at 0°C).
3. Only 1 output may be shorted at a time and then only for a maximum of 1 second.
4. See Figure 1 for threshold and hysteresis definitions.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±5%, 0°C ≤ T_A ≤ +70°C

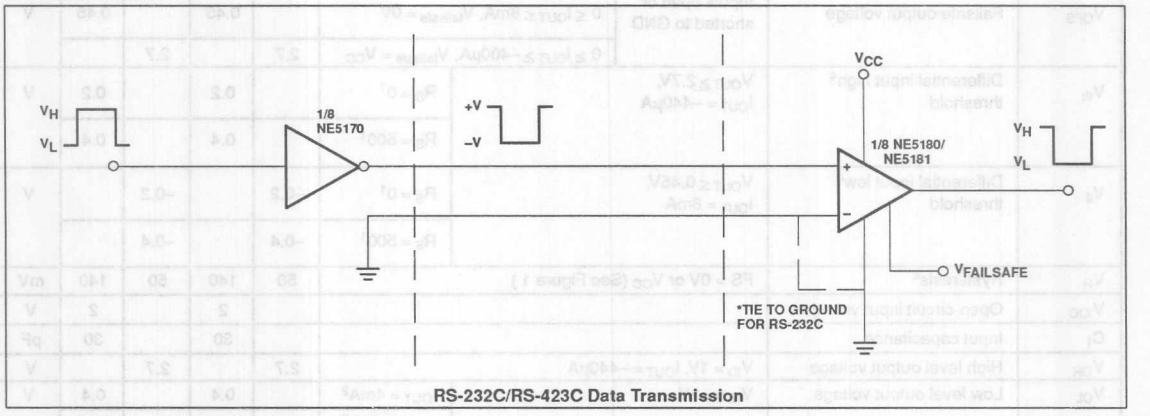
SYMBOL	PARAMETER	TEST CONDITIONS	NE5180 Min	NE5180 Max	NE5181 Min	NE5181 Max	UNIT
t_{PLH}	Propagation delay—low to high	C_L = 50pF, V_{ID} = ±1V		500		100	ns
t_{PHL}	Propagation delay—high to low	C_L = 50pF, V_{ID} = ±1V		500		100	ns
f_a	Acceptable input frequency	Unused input grounded, V_{ID} = ±200mV[1]		0.1		5.0	MHz
f_r	Rejectable input frequency	Unused input grounded, V_{ID} = ±500mV	5.5		NA		MHz

NOTE:
1. V_{ID} = ±1V for NE5181.

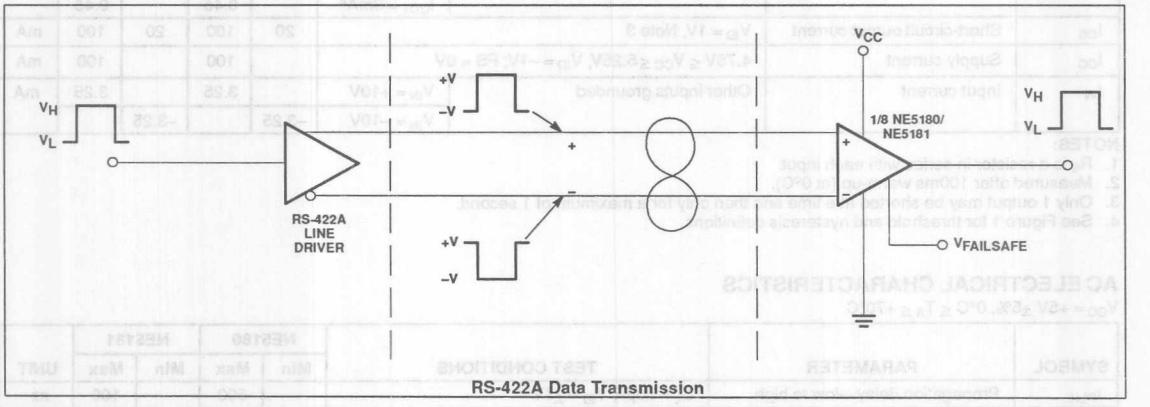
FAILSAFE OPERATION

These devices provide a failsafe operating mode to guard against input fault conditions as defined in RS-422A and RS-423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to V_{CC} or ground. A connection to

APPLICATIONS

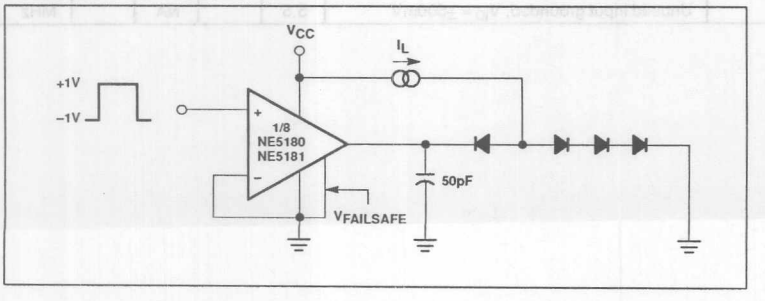


RS-232C/RS-423C Data Transmission

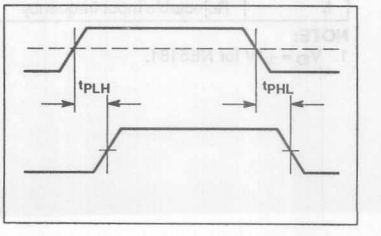


RS-422A Data Transmission

AC TEST CIRCUIT



VOLTAGE WAVEFORMS



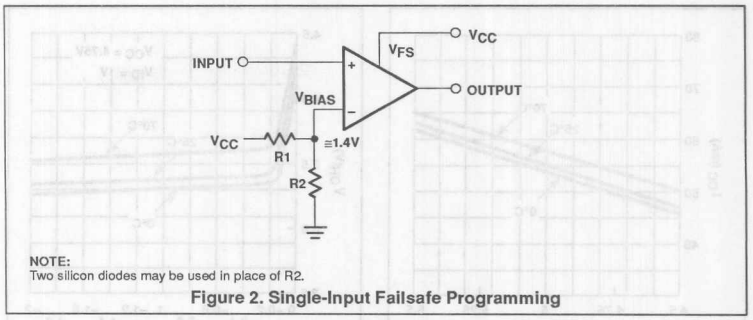
V_{CC} provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the NE5180 or NE5181 where each provides common failsafe control for four receivers.

RS-232 FAILSAFING

The internal failsafe circuitry works by providing a small input offset voltage which can be polarity-switched by using the failsafe control pins. This offset is kept small (approximately 80mV) to avoid degradation of the ±200mV input threshold for RS-423 or RS-422 operation. If the positive and negative inputs to any receiver are both shorted to ground or open circuited, the internal offset drives that output to the programmed failsafe state. If only one input open circuits (as may be the case for RS-232 operation), that input will rise to the "input open circuit voltage" (approximately 700mV). Since this is much greater than the 200mV threshold, the output will be driven to a state that is independent of the failsafe programming. Failsafe programming can be achieved for non-inverting single-ended applications by raising or lowering the unused input bias voltage as shown in Figure 2. For $V_{BIAS} \cong 1.4$, an open (or grounded) INPUT line will be approximately 700mV (0V) and the output will failsafe low. If the resistor divider is not used and V_{BIAS} is connected to ground, the output will failsafe high due to the internal failsafe offset for the INPUT grounded and the 700mV "open circuit input voltage" for the INPUT open circuited. Similar operation holds for an inverting configuration, with V_{BIAS} applied to the positive input and V_{FS} = ground.

INPUT FILTERING (NE5180)

The NE5180 has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5MHz at ±500mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output. As the signal amplitude decreases (increases) the rejected frequency decreases (increases).



NOTE:
Two silicon diodes may be used in place of R2.

Figure 2. Single-Input Failsafe Programming

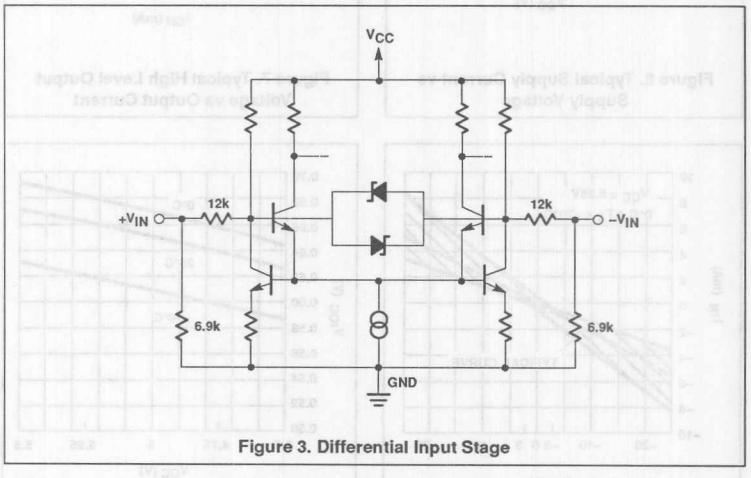


Figure 3. Differential Input Stage

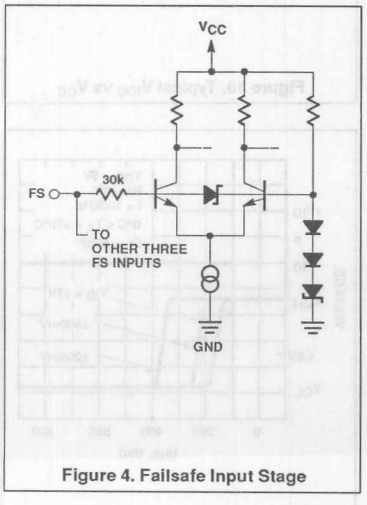


Figure 4. Failsafe Input Stage

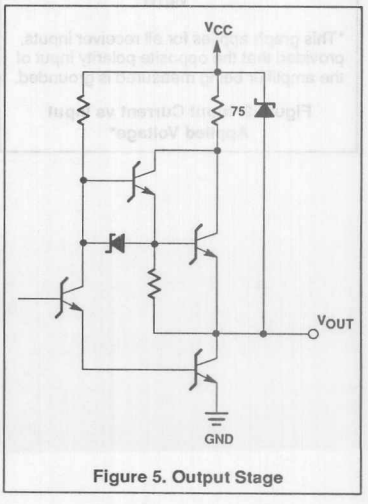


Figure 5. Output Stage

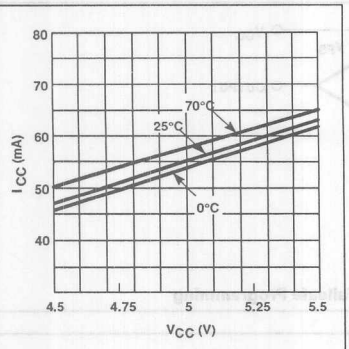


Figure 6. Typical Supply Current vs Supply Voltage

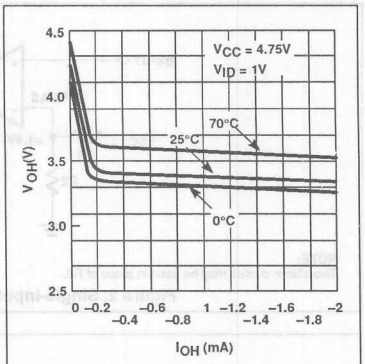


Figure 7. Typical High Level Output Voltage vs Output Current

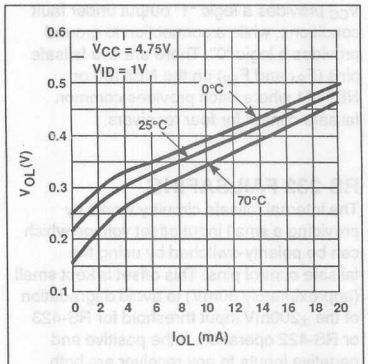
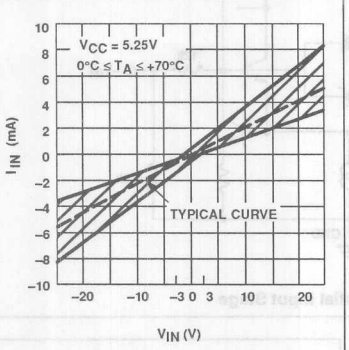


Figure 8. Typical Low Level Output Voltage vs Output Current



*This graph applies for all receiver inputs, provided that the opposite polarity input of the amplifier being measured is grounded.

Figure 9. Input Current vs Input Applied Voltage*

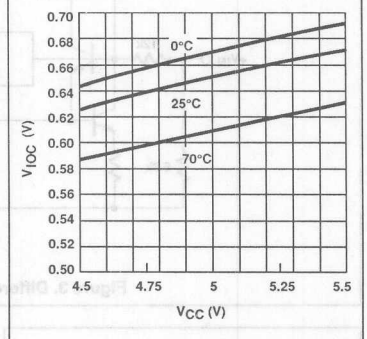


Figure 10. Typical V_{IOC} vs V_{CC}

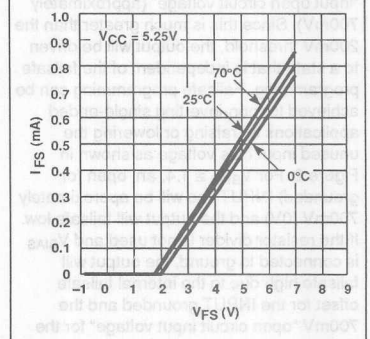


Figure 11. Typical FS Input Current vs FS Applied Voltage

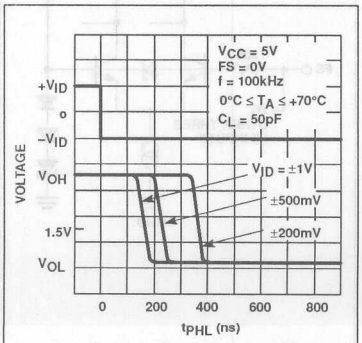


Figure 12. NE5180: Propagation Delay at Various Input Amplitudes

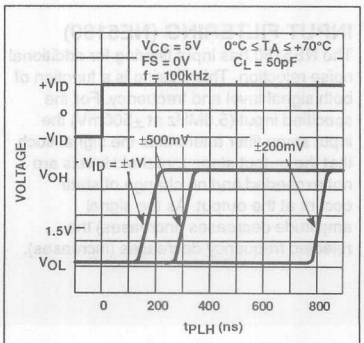


Figure 13. NE5180: Propagation Delay at Various Input Amplitude

DESCRIPTION

The AM26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The AM26LS31 meets all the requirements of EIA standard RS-422 and Federal standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines. The circuit provides an enable and disable function common to all four drivers. The AM26LS31 features 3-State outputs and logical ORed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The AM26LS31 is constructed using advanced Low Power Schottky processing.

FEATURES

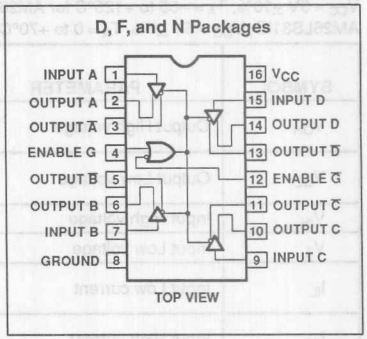
- Output skew of 2.0ns typical
- Input to output delay: 12ns
- Operation from single +5V
- 16-pin DIP and SO packages
- Four line drivers in one package
- Output short-circuit protection
- Complementary outputs
- Meets EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines
- Available in military and commercial temperature range
- Advanced low power Schottky processing
- Outputs won't load line when V_{CC} = 0V

APPLICATIONS

- Data communications equipment
- Computer peripherals
- Workstations
- Automatic test equipment

PIN CONFIGURATION

D, F, and N Packages



TOP VIEW

FUNCTION TABLE (Each Driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	A	$\overline{A}$
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

NOTES:
H = High level
L = Low level
X = Irrelevant
Z = High-impedance (OFF)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	AM26LS31CN
16-Pin SO	0°C to +70°C	AM26LS31CD
16-Pin Plastic DIP	–40°C to +85°C	AM26LS31IN
16-Pin SO	–40°C to +85°C	AM26LS31ID
16-Pin Plastic DIP	–55°C to +125°C	AM26LS31MN

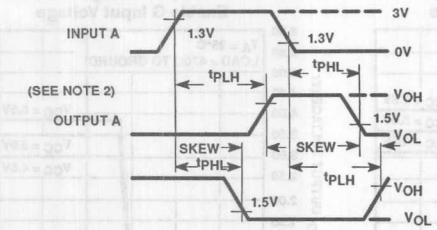
DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%, T_A = –55 to +125°C for AM26LS31MF and AM26LS31MN; V_{CC} = 5V ±5%, T_A = –40 to +85°C for AM26LS31IN and AM26LS31ID; V_{CC} = 5V ±5%, T_A = 0 to +70°C for AM26LS31CN and AM26LS31CD, unless otherwise specified.

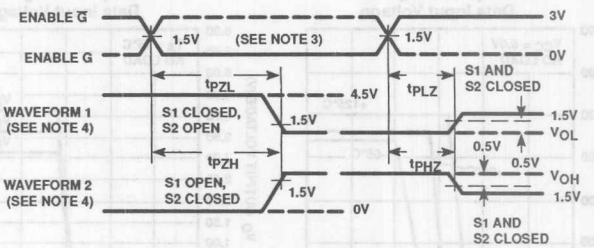
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
V_{OH}	Output High voltage	V_{CC} = Min., I_{OH} = –20mA	2.5	3.0		V
V_{OL}	Output Low voltage	V_{CC} = Min., I_{OL} = 20mA		0.3	0.5	V
V_{IH}	Input High voltage	V_{CC} = Min.	2.0			V
V_{IL}	Input Low voltage	V_{CC} = Max.			0.8	V
I_{IL}	Input Low current	V_{CC} = Max., V_{IN} = 0.4V		–0.26	–0.36	mA
I_{IH}	Input High current	V_{CC} = Max., V_{IN} = 2.7V		0.001	20	µA
I_I	Input reverse current	V_{CC} = Max., V_{IN} = 7.0V		0.001	0.1	mA
I_O	OFF-state (high-impedance) output current	V_{CC} = Max., V_O = 5.5V V_O = 0.5V		0.6 –0.050	20 –20	µA µA
V_I	Input clamp voltage	V_{CC} = Min., I_{IN} = –18mA		–0.8	–1.5	V
I_{SC}	Output short-circuit current	V_{CC} = Max.	–30		–150	mA
I_{CC}	Power supply current	V_{CC} = Max; all outputs disabled		40	80	mA
t_{PLH}	Input to output	T_A = 25°C, load[2]		9	20	ns
t_{PHL}	Input to output	T_A = 25°C, load[2]		9	20	ns
SKEW	Output to output	T_A = 25°C, load[2]		2	6	ns
t_{LZ}	Enable to output	T_A = 25°C, C_L = 10pF		17	35	ns
t_{HZ}	Enable to output	T_A = 25°C, C_L = 10pF		12	30	ns
t_{ZL}	Enable to output	T_A = 25°C, load[2]		14	45	ns
t_{ZH}	Enable to output	T_A = 25°C, load[2]		12	40	ns

NOTES:
1. All typical values are T_A = +25°C; V_{CC} = 5.0V.
2. C_L = 30pF; V_{IN} = 1.3V to V_{OUT} = 1.3V; V_{PULSE} = 0V to 3.0V.

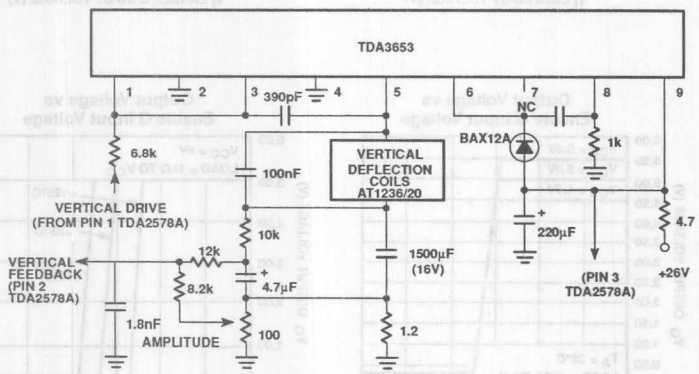
TIMING DIAGRAMS



Propagation Delay Times and Skew



Enable and Disable Times

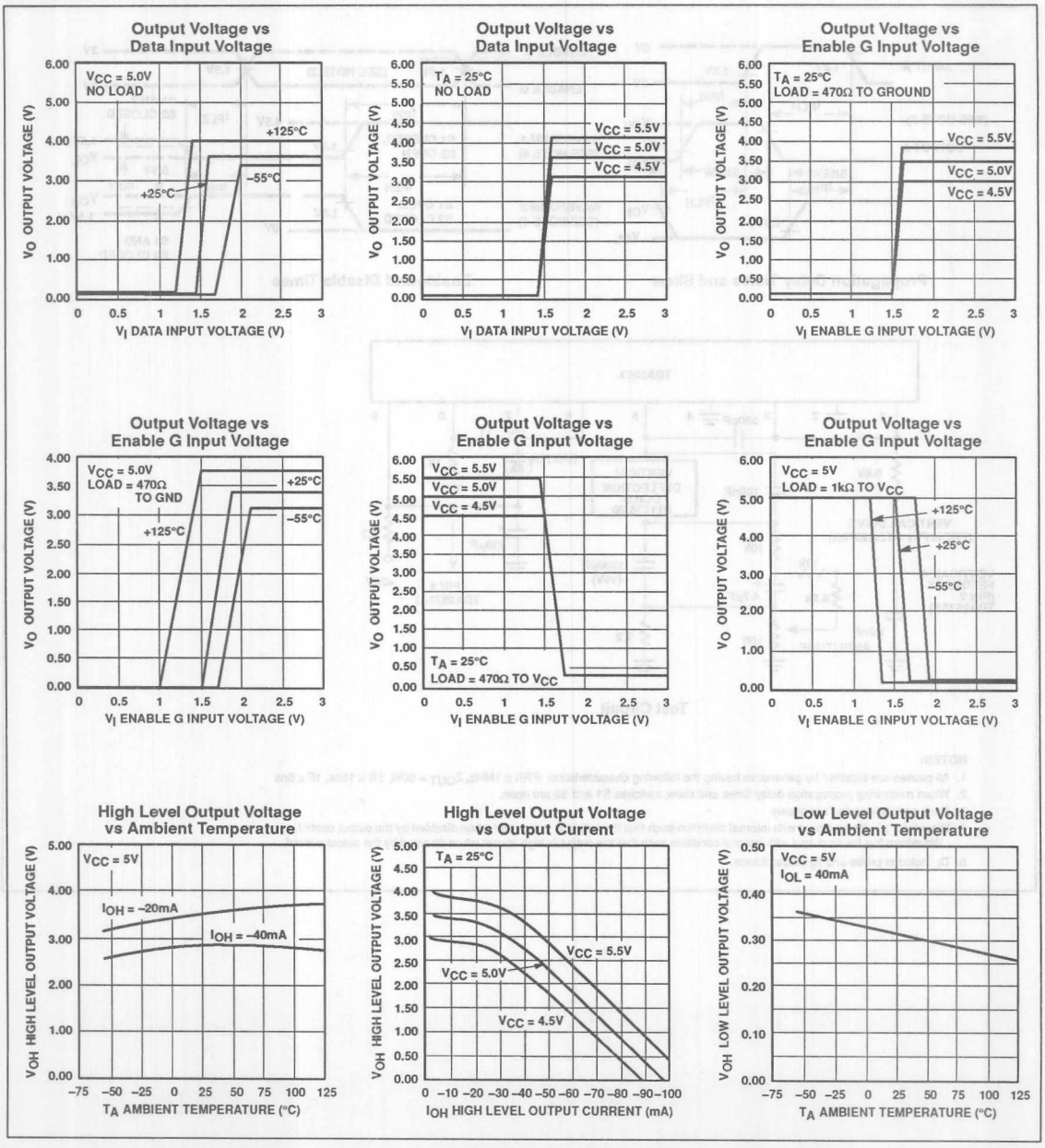


Test Circuit

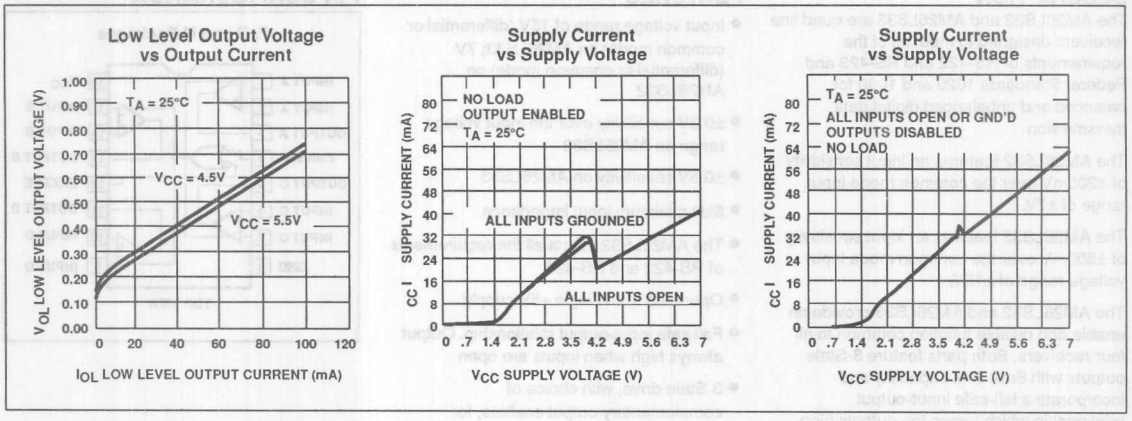
NOTES:

1. All pauses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_{OUT} = 50W, 1R ≤ 15ns, 1F ≤ 6ns
2. When measuring propagation delay times and skew, switches S1 and S2 are open.
3. Each enable is tested separately.
4. Waveform 1 is for an output with internal condition such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal condition such that the output is high except when disabled by the output control.
5. C_L includes probe and jig coapacitance.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Quad high-speed differential line receivers

AM26LS32/ AM26LS33

DESCRIPTION

The AM26LS32 and AM26LS33 are quad line receivers designed to meet all of the requirements of RS-422 and RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The AM26LS32 features an input sensitivity of ±200mV over the common mode input range of ±7V.

The AM26LS33 features an input sensitivity of ±500mV over the common mode input voltage range of ±15V.

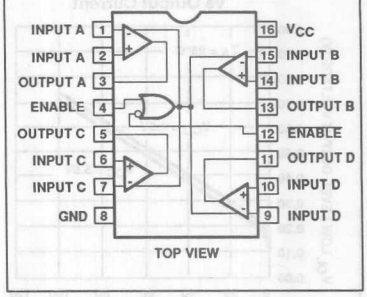
The AM26LS32 and AM26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-State outputs with 8mA sink capability and incorporate a fail-safe input-output relationship which forces the outputs high when the inputs are open.

FEATURES

- Input voltage range of 15V (differential or common mode) on AM26LS33; 7V (differential or common mode) on AM26LS32
- ±0.2V sensitivity over the input voltage range on AM26LS32
- ±0.5V sensitivity on AM26LS33
- 6kΩ minimum input impedance
- The AM26LS32 meets all the requirements of RS-422 and RS-423
- Operation from single +5V supply
- Fail safe input-output relationship. Output always high when inputs are open
- 3-State drive, with choice of complementary output enables, for receiving directly onto a data bus
- 3-State outputs disabled during power up and power down

PIN CONFIGURATION

F, D and N Packages



TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	AM26LS32CN
16-Pin SO	0°C to +70°C	AM26LS32CD
16-Pin Plastic DIP	–40°C to +85°C	AM26LS32IN
16-Pin SO	–40°C to +85°C	AM26LS32ID
16-Pin Plastic DIP	–55°C to +125°C	AM26LS32MN
16-Pin Plastic DIP	0°C to +70°C	AM26LS33CN
16-Pin SO	0°C to +70°C	AM26LS33CD
16-Pin Plastic DIP	–40°C to +85°C	AM26LS33IN
16-Pin SO	–40°C to +85°C	AM26LS33ID
16-Pin Plastic DIP	–55°C to +125°C	AM26LS33MN

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	7	V
V_{IN}	Power supply	7	V
	Output sink current	50	mA
	Common mode range	±25	V
V_{TH}	Differential input voltage	±25	V
T_{STG}	Storage temperature range	–65 to +150	°C

DISSIPATION OPERATING TABLE

PACKAGE	POWER DISSIPATION	DERATING FACTOR	ABOVE T_A
F	1,524mW	12.19mW/°C	25°C
N	1,275mW	10.2mW/°C	25°C
D	1,262W	10.1mW/°C	25°C

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10% for AM26LS32/33MX, V_{CC} = 5.0V ±5% for AM26LS32/33CX and AM26LS32/33IX over operating temperature range unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS			LIMITS AM26LS32/33 Min	LIMITS AM26LS32/33 Typ[1]	LIMITS AM26LS32/33 Max	UNIT
V_{TH}	Differential input voltage	$V_{OUT} = V_{OL}$ or V_{OH} AM26LS32, $-7V \le V_{CM} \le +7V$			–0.2	0.06	0.2	V
		AM26LS33, $-15V \le V_{CM} \le +15V$			–0.5	0.06	0.5	V
R_{IN}	Input resistance	$-15V \le V_{CM} \le +15V$ (One input AC ground)			6.0	9.8		kΩ
I_{IN}	Input current (under test)	$V_{IN} = +15V$ Other input $-10V \le V_{IN} \le +15V$					2.3	mA
I_{IN}	Input current (under test)	$V_{IN} = -15V$ Other input $+10V \le V_{IN} \le -15V$					–2.8	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $I_{OH} = -440\mu A$ $\Delta V_{IN} = +1.0V$ $V_{\overline{ENABLE}} = 0.8V$		Com'l	2.7	3.4		V
				Mil	2.5	3.4		V
V_{OL}	Output LOW voltage	V_{CC} = Min., $V_{\overline{ENABLE}} = 0.8V$ $\Delta V_{IN} = +1.0V$	I_{OL} = 4.0mA			0.3	0.4	V
			I_{OL} = 8.0mA				0.45	V
V_{IL}	Enable LOW voltage						0.8	V
V_{IH}	Enable HIGH voltage				2.0			V
V_I	Enable clamp voltage	V_{CC} = Min., $I_{IN} = -18mA$					–1.5	V
I_O	Off state (high impedance) output current	V_{CC} = Max.	V_O = 2.4V				20	µA
			V_O = 0.4V				–20	µA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 5.0V ±10% for AM26LS32/33MX, V_{CC} = 5.0V ±5% for AM26LS32/33CX and AM26LS32/33IX over operating temperature range unless otherwise specified.

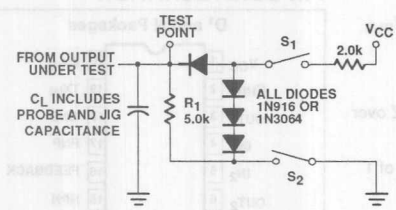
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS AM26LS32/33 Min	LIMITS AM26LS32/33 Typ[1]	LIMITS AM26LS32/33 Max	UNIT
I_{IL}	Enable LOW current	V_{IN} = 0.4V			–0.2	–0.36	mA
I_{IH}	Enable HIGH current	V_{IN} = 2.7V			0.5	20	µA
I_I	Enable input HIGH current	V_{IN} = 5.5V			1	100	µA
I_{SC}	Output short circuit current	V_{CC} = Max., ΔV_{IN} = +1V, V_{OUT} = 0V		–15	–60	–85	mA
I_{CC}	Power supply current	V_{CC} = Max.; All V_{IN} = GND outputs disabled			52	70	mA
V_{HYST}	Input hysteresis	T_A = 25°C, V_{CC} = 5.0V, V_{CM} = 0V	AM26LS32		120		mV
			AM26LS33		120		mV
t_{PLH}	Input to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			10	25	ns
t_{PHL}	Input to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			10	25	ns
t_{LZ}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 5pF (see test condition)			15	30	ns
t_{HZ}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 5pF (see test condition)			12	22	ns
t_{ZL}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			8	22	ns
t_{ZH}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF			9	22	ns

NOTE:
1. All typical values are T_A = 25°C, V_{CC} = 5.0V.

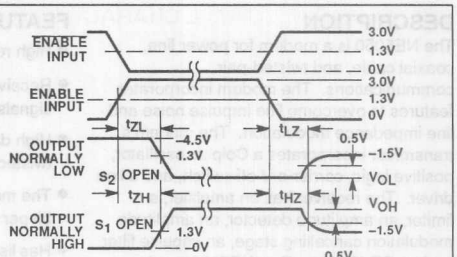
FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUT	ENABLES E	ENABLES $\overline{E}$	OUTPUT
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$V_{TL} \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	X	L	L
	H	X	X
X	L	H	Z

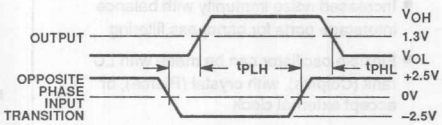
NOTES:
H = High level, L = Low level, X = Irrelevant
Z = High impedance (off), ? = Indeterminate
E = Enable, $\overline{E}$ = $\overline{\text{Enable}}$



Load Test Circuit for 3-State Outputs



Enable and Disable Tmes[2, 3, 4]



Propagation Delay[1, 4]

NOTES:
1. Diagram shown for $\overline{\text{Enable}}$ Low.
2. Enable is tested with $\overline{\text{Enable}}$ High; $\overline{\text{Enable}}$ is tested with Enable Low.
3. S_1 and S_2 of Load Circuit are closed except where shown.
4. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_O = 50Ω; t_r ≤ 15ns; t_f ≤ 6.0ns.

Power line modem — NE5050

DESCRIPTION

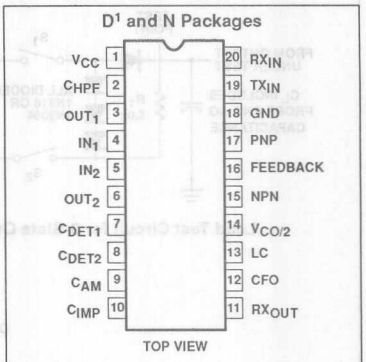
The NE5050 is a modem for power line, coaxial cable, and twisted-pair communications. The modem incorporates features to overcome line impulse noise and line impedance modulation. The modem's transmitter incorporates a Colpitts oscillator, positive logic, carrier-on/-off switch, and a line driver. The receiver has an amplifier, a limiter, an amplitude detector, an amplitude modulation cancelling stage, an impulse filter, and an SR flip-flop. One NE5050 can be used to transmit and receive with Amplitude Shift Key (ASK) carrier-on/-off modulation. With two NE5050s, Frequency Shift Key (FSK) modulation can be implemented. The transmitter input and the receiver output accept TTL or CMOS serial data.

FEATURES

- High receiver sensitivity — typ. 1.5mV_{RMS}
- Receiver input overload protected for signals up to 70V_{P-P}
- High data rates — 300kbit/s ASK NRZ over twisted-pair
- The modem reaches the Nyquist limit of 1 bit per carrier cycle
- Has listen-while-talking for carrier sense multiple access/collision detect (CSMA/CD) networking capability
- Increased noise immunity with balance interstage ports for bandpass filtering
- Flexible oscillator can be made with LC tank (Colpitts), with crystal (Pierce), or accept external clock
- Signals are processed in real-time making this modem suitable for repeater/carrier translation applications

PIN CONFIGURATION

D[1] and N Packages



TOP VIEW

NOTE:
1. SOL — Released in large SO package only.

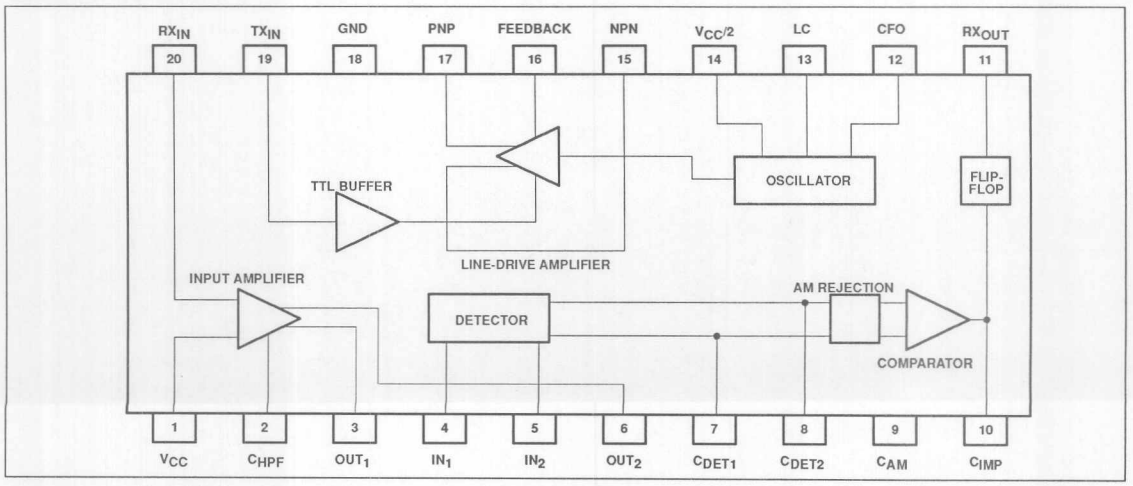
APPLICATIONS

- Twisted-pair communications
- Coaxial cable communications
- 120/277V_{RMS}, 50 or 60Hz, power line communications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE5050N
20-Pin Plastic SOL	0 to +70°C	NE5050D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	18	V
V_{LOGIC}	Logic supply voltage	18	V
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature range	–55 to +150	°C
T_{STG}	Storage temperature range	–65 to +150	°C
P_{DMAX}	Maximum power dissipation[1]	700	mW

NOTE:
1. The power dissipation is based on V_{CC} = 12V, T_J = +150°C, TX_{OFF}: I_{CC} = 20mA, TX_{ON}: I_{CC} = 50mA, θ_{JA} = 61°C/W 20-pin plastic package.

DC ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_{CC} = 12V, F carrier = 120kHz, data = NRZ, 50% duty cycle unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		10	12	16	V
I_{CC}	Supply current	TX_{OFF}	5	8	11	mA
I_{CC}	Supply current	TX_{ON}[1]	18	24	30	mA
V_{LOGIC}	Logic voltage			5	16	V
P_D	Power dissipation	RX_{OFF}, TX_{OFF} RX_{ON}, TX_{ON}, 100Ω load		100 300	220 660	mW mW
V_{IHMIN}	TX TTL input	TX_{ON}, Pin 19	2.4			V
V_{ILMAX}	TX TTL input	TX_{OFF}, Pin 19			0.8	V
V_{OLMAX}	RX open-collector output	I_{OL} = 5mA, Pin 11			0.4	V
I_{OLMAX}	RX open-collector output	Pin 11			5	mA
	TX data rate[2]	f_{CXR} = 120kHz, 500kHz	DC	1k	300k	bit/s
	RX data rate[2]	f_{CXR} = 120kHz, 500kHz	0.1	1k	300k	bit/s
	Carrier cycles per bit, TX and RX[2]		1			cycle
Broadband I/O ports, carrier						
	RX input sensitivity	1:1 input transformer	3.5	1.5		mV_{RMS}
	RX input signal level	V_{CC} ±35V = –25V, +51V			70	V_{P-P}
	RX input impedance	Pin 20		9		kΩ
	RX line impedance modulation rejection	120HzAM 2V/20mV, 1kbit/s	40			dB
	RX carrier frequency[2]		0.1	120	500	kHz
	RX detector differential input impedance	Pin 4, Pin 5, each		27		kΩ
PSRR	RX power supply rejection ratio	60Hz and 120Hz		80		dB
	Broadband port impedance	RX_{OFF} and TX_{OFF}		7.3		kΩ
	TX output signal level	TX_{ON}, 100Ω load		8		V_{P-P}
	TX driver output impedance	TX_{OFF}		40		kΩ
	TX driver output impedance	TX_{ON}		1.2		Ω
	TX amplitude temperature drift	External oscillator		+140		ppm/°C
	TX amplitude temperature drift	LC oscillator		+0.23		%/°C
	TX output current capability	TX_{ON}, Pins 15, 17		40		mA peak
	TX output THD (total harmonic distortion)	TX_{ON}, LC oscillator		1	2	%
	TX line drive amplifier BW	At 6dB gain		500		kHz
	TX carrier frequency[2]		DC	120	500	kHz
	TX oscillator temperature drift	Temperature range		+60		ppm/°C
	TX oscillator initial frequency accuracy	Sam LC tank		±1		%
	TX carrier feedthrough (leakage)	TX_{OFF}		–90		dBmO

ABBREVIATIONS:
TX = transmitter
RX = receiver
NOTES:
1. TX looped back to RX, data = 1kbit/s TTL, NRZ, 50% duty cycle ASK.
2. The NE5050 modem reaches the theoretical maximum data density for a given (fixed) carrier frequency. This limit is set by the maximum data bandwidth required before intersymbol interference occurs. The minimum specified limits are not tested in production. They are guaranteed by design.

PIN FUNCTION DESCRIPTION

Pin 1: $+V_{CC}$

For de-coupling V_{CC} to ground a 0.1µF capacitor must be placed close to Pin 1 and Pin 18.

Pin 2: C_{HPF}

High-pass filter, rejects 60Hz and its harmonics, rejects low frequencies, directing them to ground. Capacitor to ground: C_{HPF} = 10nF for f_{CXR} = 120kHz and C_{HPF} = 4.7nF for f_{CXR} = 300kHz. The input amplifier provides a high-pass function: a +20dB/decade frequency response, with a DC attenuation of –50dB. A frequency of 100kHz is amplified by +24dB. The –3dB point of this high-pass filter is given by the equation:

$10^9/C_{HPF}$ (F) = f_{-3dB} (Hz)

Pin 3: OUT_1

RX amplifier differential (+) output. Low impedance output. See Pin 6. Pin 3 can be connected to Pin 4 directly. A differential, bandpass filter can be connected from Pins 3, 6 to Pins 4, 5. If LC values are used, they are the same as the oscillator LC values (see Pins 13 and 14). The BW_{-3dB} is controlled by the series resistors R_1 and R_2. An external active filter providing gain can improve the RX sensitivity and filter out CW interference.

Pin 4, Pin 5: IN_1, IN_2

AM detector (±) inputs. High-impedance inputs = 27kΩ each. The require DC bias voltage from Pins 3 and 6 or around 4.5V. Pin 3 can be connected to Pin 4 directly. Pin 6 can be connected to Pin 5 directly. A differential bandpass filter can be connected from Pins 3, 6 to Pins 4, 5. If LC values are used, they are the same as the oscillator LC values (see Pins 13 and 14). The BW_{-3dB} is controlled by series resistors. An external active filter providing gain can improve the RX sensitivity and filter out CW interference.

Pin 6: OUT_2

RX amplifier differential (–) output. Low impedance output. See Pin 3. Pin 6 can be connected to Pin 5 directly.

Pin 7, Pin 8: C_{DET}

Amplitude detector (±) output capacitor between Pins 7 and 8. t_{DET} is the time it takes for C_{DET} to charge from 0mV to 50mV, where 50mV is the detection threshold. The detector delay time, t_{DET}, affects the receiver's jitter. t_{DET} is a term in a sum of delays, the sum being the total receiver delay, t_D. See below in 'Receiver Delays' the relation between t_D and the maximum bit rate. The C_{DET} capacitor value is given by:

C_{DET} (F) = t_{DET} (sec)/10^5

Pin 9: C_{AM}

Line impedance modulation rejection capacitor. A 0.1µF capacitor to ground provides about 4s of delay for the transition from receive data to standby. The C_{AM} value is determined in function of the bit string or in the preamble. It is a measure of the "readiness" of the receiver to switch from the "standby" mode to the "receive data mode" with no loss of leading bits. A low C_{AM} value will make the modem react faster (shorter delays) in both transition directions: from "standby" to "receive data" (incoming or departing messages) and from "receive data" to "standby" (absence of data traffic). Its value should be

C_{AM} (F) = 10–4/bit rate [bits/s]

Pin 10: C_{IMP}

Impulse noise rejection cpacitor. At 1kbit/s a 10nF capacitor to ground provides 350µs of delay and impulse rejection. This capacitor determines the receiver impulse noise immunity (transmission channel with non-Gaussian noise). t_{IMP} is the time it takes to ramp up or down the C_{IMP} voltage (the beginning of the ramp is delayed by t_{DET}). The shortest bit should last longer than the widest impulse. t_{IMP} is a term in a sum of delays, the sum being the total receiver delay, t_D. See 'Receiver Delays' for the relation between t_D and the maximum bit rate. The C_{IMP} capacitor value is determined by the equation:

C_{IMP} (F) = t_{IMP} (s)/85kΩ

The following equation determines t_{IMP}:

Maximum rejected or expected impulse noise width (s) < t_{IMP} (s)

Pin 11: RX Data Output

Open-collector RX output. RX data output.

I_{OLMAX} = 5mA = $V_{LOGIC}/R_{PULL-UP}$

Pin 12: C_{F0}

Oscillator feedback input. C_{F0} = 27 to 51pF capacitor between Pins 12 and 13. C_{F1} = capacitor between Pins 12 and GND. If the on-chip oscillator is used, C_{F1} may be omitted. If external oscillations are injected at Pin 13, C_{F0} must be removed and C_{F1} must be connected to GND. Grounding Pin 12 disables the oscillator.

Pin 13: Oscillator I/O

Colpitts LC oscillator tank, Pierce crystal oscillator, or external oscillator input.

On-chip LC oscillator — oscillator output. External oscillator tank present. Parallel LC components attached between Pins 13 and 14. C_{F0} attached between Pin 12 and Pin 13. A resistor between Pins 13 and 14 can decrease the oscillation amplitude to the desired level. Amplitudes above 2V peak may have THD > 2%. C_{F1} is not used. The amplitude varies with temperature; thermistor compensation recommended at Pin 16.

On-chip crystal oscillator — oscillator output. Two external capacitors in series, C_{13} and C_{14}. C_{13} is connected to Pin 13 and C_{14} is connected to Pin 14. The external crystal is attached between Pin 13 and the connection of C_{13} and C_{14}. An optinal inductor L, attached between Pins 13 and 14, tuned at the oscillation frequency by C_{13} and C_{14} prevents oscillations at the crystal overtones. C_{F0} and C_{F1} are not used.

External oscillator — oscillator input. Parallel LC components attached between Pins 13 and 14 provide bias to Pin 13 and perform bandpass filtering. If a square wave is generated from a microprocessor by clock division, a series LC from the divider output to Pin 13 will perform additional bandpass filtering. C_{F1} = 0.1µF is connected to ground. C_{F0} is not used. If a sinusoidal wave is available, a 50Ω resistor may replace the parallel LC bandpass filter and a 0.1µF capacitor may replace the series LC bandpass filter. The amplitude is constant over temperature.

Pin 14: $+V_{CC}/2$

Oscillator bias at $+V_{CC}/2$. A 0.1µF de-coupling capacitor to GND is optional.

Parallel LC components attached between Pins 13 and 14.

Pin 15: TX Carrier Output (NPN Transistor Base)

Transmitter broadband output. Can drive 40mA peak (80mA peak non-repetitive).

NPN external Darlington translator drive — Drives 1Ω loads.

NPN external translator drive — 1Ω – 0.5W – R_{E1} to Pin 16 for 10Ω loads.

On-chip driver — 10Ω R_{E1} between Pins 15 and 16 for 50Ω loads.

Pin 16: TX Line Drive Feedback

$R_{FEEDBACK}$ adjusts the driver amplifier gain. Minimum gain ($R_{FEEDBACK}$ = 0) is 2 (6dB). A thermistor can compensate the LC oscillator amplitude variation. R_{E1} resistor (and NPN EB junction) to Pin 15. R_{E2} resistor (and PNP EB junction) to Pin 17. The C_{DRIVE} coupling capacitor is in series with the R_{DRIVE} resistor from Pin 16 to Pin 20. The R_{DRIVE} value is the assumed line impedance. The C_{DRIVE} impedance is $1/(2 \times f_{CXR} C_{DRIVE})$.

Pin 17: TX Carrier Output (PNP Transistor Base)

Transmitter broadband output. Can drive 40mA peak (80mA peak non-repetitive).

PNP external Darlington translator — Drives 1Ω loads.

PNP external translator drive — 1Ω – 5.0W – R_{E2} to Pin 16 for 10Ω loads.

On-chip driver — 10Ω R_{E2} between Pins 16 and 17 for 50Ω loads.

Pin 18: Ground

Pin 19: TX Data Input

Transmitter TTL data input. Logic 1 will turn the transmit driver on, and sinusoidal carrier will be sent to the line from a low impedance source. Logic 0 will turn the driver off, to high output impedance.

Pin 20: RX Carrier Input

Receiver carrier input. Withstands an over-voltage of $+V_{CC}$ ±35V. DC bias connected through the line coupling transformer secondary to $+V_{CC}$ (Pin 1). The C_{DRIVE} coupling capacitor is in series with the R_{DRIVE} resistor from Pin 16 to Pin 20.

DESCRIPTION OF OPERATION

The NE505 modem has been designed for transmitting and receiving control and data signals over the AC power lines, coaxial cables and twisted-pair cables. The modem overcomes line impulse noise and line impedance modulation. Two carrier modulation methods can be used: carrier on/off ASK, NRZ data and non-coherent FSK. The power line is not an ideal medium for communication. The line noise, interference and losses are caused by: impulse noise, CW interference, line impedance modulation, and distribution transformer attenuation. NE5050 was designed to support both ASK and non-coherent FSK communications in this environment.

Listen-While-Talk

The IC modem is always in the receive mode, even when transmitting (it receives its own carrier). This capability permits remote RX and TX functionality testing for each system node. In the receive mode, the modem receives carrier signals from other transmitters. In the transmit mode, the modem transmits carrier to other receivers and receives its own carrier.

On-Chip Collision Detection

The liten-while-talk capability enables this IC to perform CSMA/CD (carrier-sense, multiple-access/collision detect) networks. Collision is dtected when the local TX intends to transmit and the line is not clear.

In Dense Data Traffic

The RX data output (RX_{OUT}) does not have time to go into the stanby (lower power consumption, inverted logic) mode. In this case the RX_{OUT} is in positive logic (carrier-on = 1, carrier-off = 0). A collision is detected at the local node when the local TX is off and the local RX_{OUT} = 1. Collision: remote carrier present and detected. Abort local transmission. If, however, standby occurs (bursts of high-speed data) a proper value of C_{AN} will inusre capture of all leading bits except for the first "10" transition.

In Rare Data Traffic

The RX_{OUT} is in standby most of the time. In this case the RX_{OUT} logic mode is inverted due to a designed-in offset present in the AM rejection and impulse filter circuits. A logic sequence from the local TX insures proper RX offset adjustment (preamble, the first "10" bits). The collision detection proceeds as in the dense data traffic case. The transition time from the last received bit "1" to the standby mode is proportional to the value of the AM rejection capacitor at Pin 9. For C_{AM} = 10nF, the "receive data" to "standby" transition occurs after 4 seconds from the last "1". Therefore, long strings of "0"s can be transmitted and received. The standby function may be disabled with proper bias at Pin 9 (external components).

TX-to-RX and RX-to-TX Switching Times

With the listen-while-talk capability the TX-to-RX and the RX-to-TX switching times have the meaning of TX_{ON}-to-TX_{OFF} and TX_{OFF}-to-TX_{ON} switching times, respectively. The TX-to-RX and RX-to-TX minimum switching times can be calculated from the maximum data rate. Since one bit can last a minimum of 3µs (NRZ ASK data), this may be considered the minimum switching time.

Data Rate

The maximum data rate is 300kbit/s NRZ ASK. This data rate was achieved on a twisted-pair cable with a 150kHz, 50% duty cycle square wave fro data. The data rate depends on the BPF (between Pins 3 – 4 and 5 – 6), on the AM detector capacitor for delay, C_{DET} (between Pins 7 and 8), on C_{AM} (Pin 9) for capture of leading bits, and on the desired impulse noise immunity for delay, C_{IMP} (Pin 10).

AC Line Coupling Network

One or two (120V or 240V and 277V AC RMS) coupling capacitors rated 600V are connected in series with the primary of a 1:1 transformer and connected to the AC line. The transformer secondary may be tuned to the carrier frequency by a capacitor (TOKO transformer, low data rates) or no secondary tuning capacitor for higher data rates (AIE Magnetics transformer). Two back-to-back zener diodes must be placed between Pins 1 and 20 for the IC transient protection (1N4744 or 1N6275). The transformer secondary carries DC bias current between Pins 1 and 20 of the IC. This coupling network itself attenuates to below the RX input sensitivity the 50 or 60Hz and their harmonic frequencies. In a coaxial cable application the transformer can be replaced with a coupling capacitor.

Receiver (RX)

The typical RX sensitivity is $1.5mV_{RMS}$. For less sensitivity, adjust the turn ratio of the coupling transformer or insert loss in the bandpass filter. The RX-only function can be implemented by not using the oscillator and by grounding the TX input. The maximum data rate is 300kbit/s. The power supply rejection ratio (PSRR) is 80dB for 60Hz and 120Hz. The RX is composed of the following blocks:

The Input Amplifier/Limiter limits its output signals to $1.2V_{P-P}$. The maximum input carrier signal can be $70V_{P-P}$. The gain is 24dB. The input amplifier bandpass characteristic has the upper –3dB frequency

internally fixed at 300kHz. The lower –3dB frequency is adjustable with the C_{HPF} capacitor from Pin 2 to GND. For maximum RX sensitivity CHPF = 10nF at f_{CXR} = 120kHz. A C_{HPF} = 0.1µF value attenuates 60Hz by 50dB and 120Hz by 45dB.

The Bandpass Filter is differential RLC bandpass filter which can be connected from Pins 3, 6 to Pins 4, 5. The LC values are the same as the oscillator LC values (see Pins 13 and 14). The formulae relating the BW_{-3dB} to the RLC values are:

$$\frac{BW_{-3dB}}{\omega_{CXR}} = \frac{(\omega_{CXR} \cdot L)}{(2 \cdot R)} = \frac{1}{Q}$$

$$\frac{BW_{-3dB}}{\omega_{CXR}} = \frac{1}{(\omega_{CXR} \cdot 2 \cdot C \cdot R)} = \frac{1}{Q}$$

$$BW_{-3dB} = \frac{(\omega_{CXR} \cdot \omega_{CXR} \cdot L)}{(2 \cdot R)}$$

$$BW_{-3dB} = \frac{1}{(2 \cdot C \cdot R)} \quad \text{and}$$

$$\omega_{CXR} = 2 \cdot f_{CXR}$$

If no bandpass filter is required, connect Pin 3 to 4 and Pin 5 to 6 ($R_1 = R_2 = 0\Omega$).

The Amplitude Detector is a Gilbert phase detector with a single differential input. The compared signals are always in phase and the demodulatred output is a full rectified wave, function of the bias current, the carrier amplitude, and the collector load. The detected voltage is developed across a differential capacitive load between Pin 7 (+) and Pin 8 (–). DC offset is caused by the line impedance modulation.

The AM Rejection Circuit stabilizes the DC average value of the envelope by adding or subtracting a series voltage to the voltage of the detector capacitor. The AM rejection is 40dB at a modulation rate of 120Hz. The value of the AM rejection capacitor CAM (Pin 9 to GND) determines the transition times to and from receive data and standby.

The Slicing Comparator has current output and a fixed threshold of 50mV.

The Impulse Filter consists of a capacitor, C_{IMP}, at the output of the comparator, from Pin 10 to GND. This capacitor is charged or discharged with constant current from the comparator, causing the voltage variation to be a constant slope in time. Narrow current impulses will not last long enough to fully charge or discharge the capacitor.

$2V_{BE}$ Voltage Hysteresis provides a voltage interval in which the C_{IMP} voltage ramps and in which both inputs to the SR flip-flop are zero.

The Flip-Flop is an SR type, with an open-collector transistor output at Pin 11. The transistor can switch a maximum load of 5mA.

Receiver Delays and Maximum Data Rate

The total receiver delay is a sum of delays, where t_{DET} (sec) is the detector delay, t_{IMP} (sec) is the impulse filter delay, and 2µs is the approximate receiver delay with no C_{DET} and no C_{IMP}:

t_D (sec) = total receiver delay
= t_{DET} (sec) + t_{IMP} (sec) + 2µs

The maximum bit rate, in the no-return-to-zero, amplitude shift keying data format is determined by: Maximum bit rate MRZ ASK (bit/sec) < $1/t_D$ (sec^{-1})

NOTE:
The C_{DET} and C_{IMP} values so calculated are for guidance and the user shall deterine the optimal performance values in a range between 0.1 times to 10 times the calculated values (power line environment assumed). For twisted-pair or coaxial cables the calculated values are close to optimal. Based on power line applications made at 100bits/sec and at 50kbits/sec, the C_{IMP} / C_{DET} capacitor ratio ranges from 100:1 to 1:1.

Transmitter, TX

The transmitter includes an oscillator, a line driver, and a drive switch.

The TTL Switch is a low power TTL gate that switches on/off the bias current for the line driver. A logic "1" at Pin 19 (TXIN) enables the line driver and carrier is being sent on the line. A logic "0" disables the driver.

The Oscillator is a differential transistor pair. It can be configured as a Colpitts LC oscillator, as a Pierce crystal oscillator, or used with external input (microprocessor clock divided to the carrier frequency). When the TX drive is off, the carrier leak is less than –90dBmO. Pin 18 can be used as input for an external oscillator. Grounding Pin 12 disables the oscillation process.

The Line Driver is a class AB push-pull stage with optional external complementary transistor pair for increased current capability. The TX output impedance is 40Ω in the off-state (receive mode) and less than 2Ω in the on-state (transmit mode). Note that in the transmit mode one receives its own signal. To increase the amplitude of the transmitter, add a feedback resistor in the driver amplifier feedback path at Pin 16.

By itself the NE5050 is capable of driving consumer line impedance of 50Ω (40mA peak/80mA peak non-repetitive), the THD being less than 2%. With complementary transistors, 10Ω industrial loads can be driven. With complementary Darlington transistors, 1Ω industrial loads can be driven.

One design objective was to provide the user with a flexible IC modem for residential as well as for industrial AC lines, for twisted-pair, and for coaxial cables. The IC modem can be used for control functions and data applications. Practical observations of power line noise point to a data rate upper boundary of 1kbit/sec. The main sources of interference are the light dimmers. Software for error correction can be used for improved error rates. Two system configurations can be implemented: an ASK system and a non-coherent FSK system. The non-coherent FSK system can continue to transmit ASK data if the other channel is made unusable by CW interference. High-voltage transient protection and filtering are accomplished with user-selected external components.

Additional flexibility is provided by the chip architecture: one-IC real-time repeater, one-IC dual-frequency gateway, external oscillator input port, the listen-while-talk capability (CSMA/CD), immediate TX-to-RX switching, ASK and FSK, and ASK-multinode single-frequency network.

The modem can be used for control systems and data applications in homes and other consumer environments and in industry.

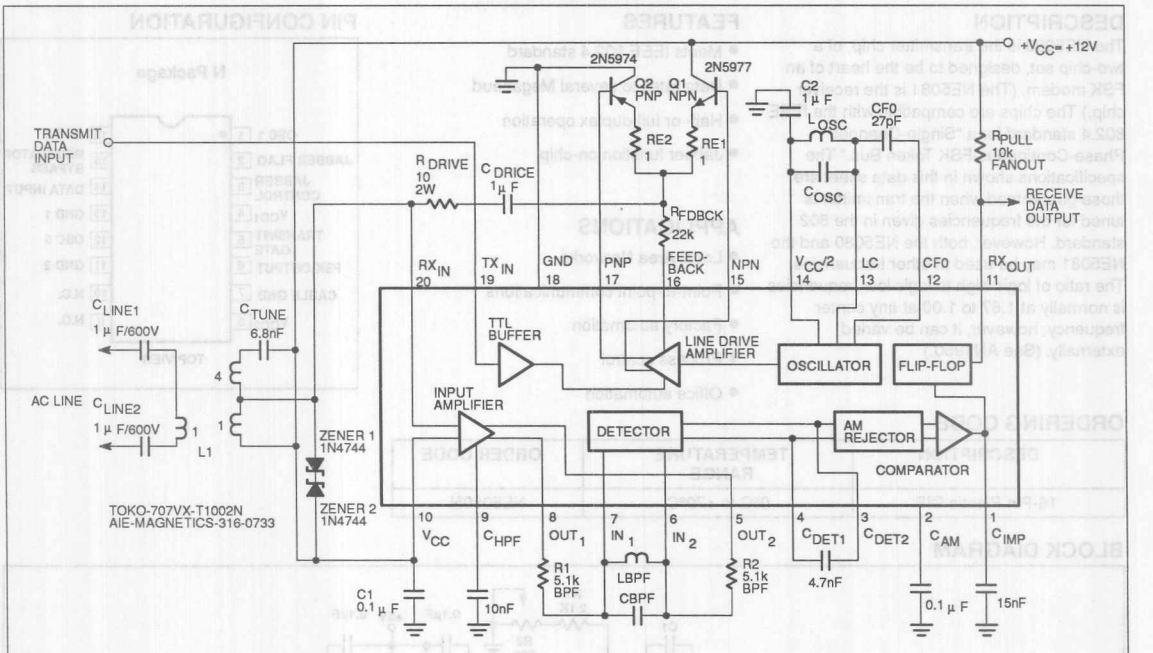


Figure 1. Typical Application Circuit for 1kbit/s on the 120/277V AC Line

High-speed FSK modem transmitter NE5080

DESCRIPTION

The NE5080 is the transmitter chip, of a two-chip set, designed to be the heart of an FSK modem. (The NE5081 is the receiver chip.) The chips are compatible with the IEEE 802.4 standard for a "Single-Channel" Phase-Continuous-FSK Token Bus." The specifications shown in this data sheet are those guaranteed when the transmitter is tuned for the frequencies given in the 802 standard. However, both the NE5080 and the NE5081 may be used at other frequencies. The ratio of logic high to logic low frequencies is normally at 1.67 to 1.00 at any center frequency; however, it can be varied externally. (See AN1950.)

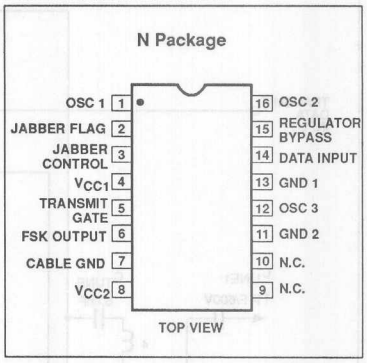
FEATURES

- Meets IEEE 802.4 standard
- Data rates to several Megabaud
- Half- or full-duplex operation
- Jabber function on-chip

APPLICATIONS

- Local Area Networks
- Point-to-point communications
- Factory automation
- Process control
- Office automation

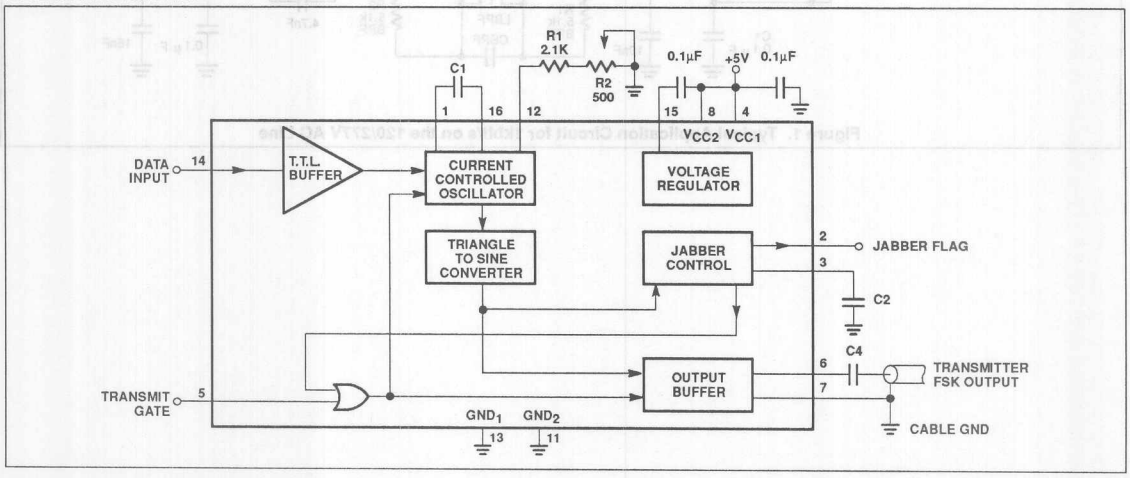
PIN CONFIGURATION



ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	NE5080N

BLOCK DIAGRAM



High-speed FSK modem transmitter NE5080

GENERAL DESCRIPTION

The NE5080 is designed to transmit high frequency asynchronous data on coaxial cable, at rates from DC to 2M baud (see Note 1). The chip accepts serial data and transmits it as a periodic signal whose frequency depends on whether the data is high or low.

The device is meant to operate at a frequency of 6.25MHz for a logic high and 3.75MHz for a logic low (see Note 2). The frequency is set up by external trimming components; however, the ratio of the high and low frequencies is set internally and cannot be altered.

The FSK output can be turned off by use of the transmit gate pin. When turned off, the transmitter has a high output impedance and the oscillator is disabled.

The length of time a transmitter can transmit can be controlled by the use of the Jabber control pin (see description of Jabber Control Pin).

Jabber Control Pin

During the time the transmitter is transmitting, this pin sources a current. This current can be used to set the maximum time that the transmitter can be on. There are three options that can be used:

1. Use the current to charge a capacitor. When the voltage across the cap gets to approximately 1.4V, the transmitter will turn off. A logic low applied to Pin 3 will reset the Jabber function; an open collector output should be used for this purpose. A logic high applied to the pin will disable the transmitter.
2. Use to externally sense the current and have external circuitry to control the length of time the transmitter is on.
3. The pin can be tied to ground and is then not active. Transmission is then controlled solely by the signal at the transmit gate pin.

Jabber Flag Pin

This pin will go to a logic high when the Jabber Control pin is used to shut off the transmitter. It will latch and can be reset by applying a logic low to the Jabber Control pin.

NOTES:

1. The NE5080 is capable of transmitting up to 1M baud of differential Manchester code at a center frequency of 5MHz.
2. Although the chip is designed to meet the requirements of IEEE standard 802.4 (Token-Passing Single-Channel Phase-Continuous-FSK Bus), it can be used at other frequencies.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply Voltage	+6	V
V_{IN}	Input voltage range (Data, Gate)	–0.3 to V_{CC}	V
P_D	Power dissipation	800	mW
T_A	Operating temperature range	0 to +70	°C
T_J	Maximum junction temperature	+150	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 10sec)	300	°C

NE5080 PIN FUNCTION

PIN	FUNCTION
1	**OSC 1:** One end of the external capacitor used to set the carrier frequency.
2	**Jabber Flag:** This pin goes to a logic high if the transmitter attempts to transmit for a longer time than allowed by the Jabber control function.
3	**Jabber Control:** Used to control transmit time. See note on Jabber function.
4	**V_{CC1}:** Voltage supply.
5	**Transmit Gate:** A logic flow on this pin will enable the transmitter; a logic high will disable it.
6	**Transmitter FSK Output**
7	**Cable Ground:** The shield of the coax cable should be connected to this pin and to Pin 11.
8	**V_{CC2}:** Connect to Pin 4 close to device.
9	**No Connection**
10	**No Connection**
11	**Ground 2:** Connect to Analog ground close to device.
12	**OSC 3:** A variable resistor between this point and ground is used to set the carrier frequencies.
13	**Ground 1:** Connect to Analog close to device.
14	**Data Input**
15	**Regulator Bypass:** A bypass capacitor between this pin and V_{CC1} is required for the internal voltage regulator function.
16	**OSC 2:** One end of a capacitor that is between Pin 1 and Pin 16 and is used to set the carrier frequency.

DC ELECTRICAL CHARACTERISTICS $V_{CC1,2}$ = 4.75–5.25V, T_A = 0°C to +70°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_1	Output frequency (Logic high)	Data input ≥2.0V (See Note 1)	6.17	6.25	6.33	MHz
f_0	Output frequency (Logic low)	Data input ≤0.8V (See Note 1)	3.67	3.75	3.83	MHz
V_O	Output amplitude	Data input ≥2.0V or ≤0.8V Output Load = 37.5Ω	0.5		1.0	V_{RMS}
R_{OFF}	Output impedance (gated off)	Transmit gate ≥2.0V	100			kΩ
R_{ON}	Output impedance (gated on)	Transmit gate ≤0.8V			37.5	Ω
C_O	Output capacitance	Transmit gate ≥2.0V or ≤0.8V			10	pF
V_F	Feedthrough	Transmit gate ≥2.0V 2.0MHz sq. wave (TTL levels) input			1	mV_{RMS}
I_J	Jabber current	Transmit gate ≤0.8V Input ≥2.0V or ≤0.8V		1.25		µA
I_{CC}	Supply current	V_{CC1} connected to V_{CC2}		75	100	mA
Logic levels						
	Data Input					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	V_{IN} = 2.4V			40	µA
I_{IL}	Input current	V_{IN} = 0.4V			–1.6	mA
	Transmit gate					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	VG = 2.4V			40	µA
I_{IL}	Input current	VG = 0.4V			–1.6	mA
	Jabber flag					
V_{OH}	Logic high	I_{OH} = –400µA	2.4			V
V_{OL}	Logic low	I_{OL} = 4.0mA			0.4	V
	Jabber control					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V

NOTE:
1. Tuned per instructions in AN195.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_S	Setup time	Data in	Gate on	Figure 1	2	0.1		µs
t_A	Delay time	Output freq. change	Data transition	Figure 2			150	ns
t_B	Delay time	Output disabled	Gate off	Figure 3		0.4	2	µs
t_C	Delay time	Output disabled	Jabber control	Figure 4			100	ns
t_D	Delay time	Jabber flag	Jabber control	Figure 5			100	ns
	Jabber control reset Pulse width (Logic low)				100			ns

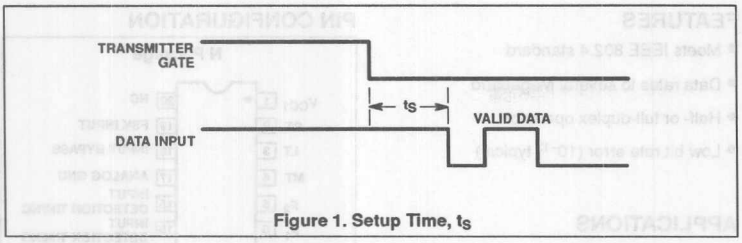


Figure 1. Setup Time, t_S

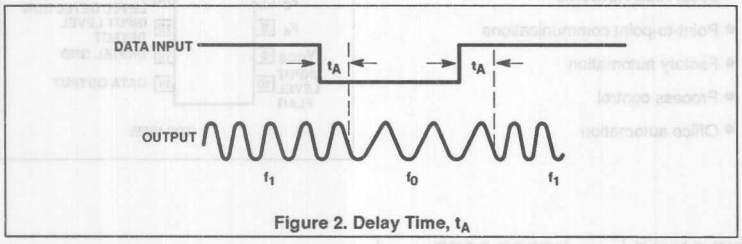


Figure 2. Delay Time, t_A

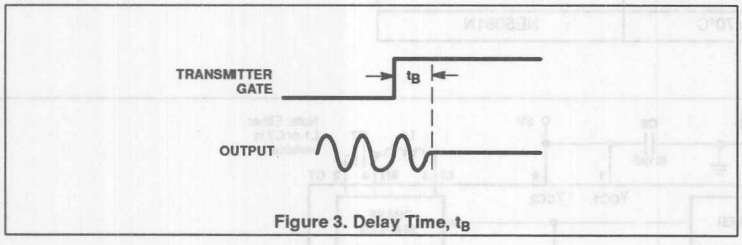


Figure 3. Delay Time, t_B

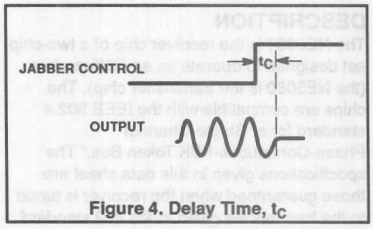


Figure 4. Delay Time, t_C

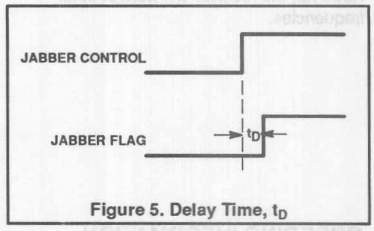


Figure 5. Delay Time, t_D

DESCRIPTION

The NE5081 is the receiver chip of a two-chip set designed to operate as an FSK modem (the NE5080 is the transmitter chip). The chips are compatible with the IEEE 802.4 standard for a "Single-Channel Phase-Continuous-FSK Token Bus." The specifications given in this data sheet are those guaranteed when the receiver is tuned to the frequencies given in the 802 standard. However, the receiver will work at other frequencies.

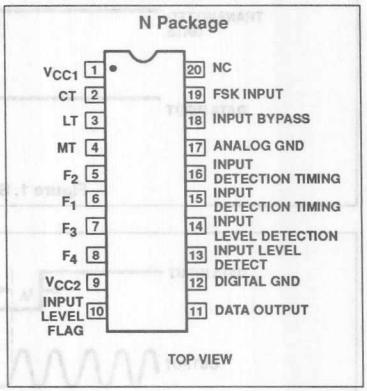
FEATURES

- Meets IEEE 802.4 standard
- Data rates to several Megabaud
- Half- or full-duplex operation
- Low bit rate error (10^{-12} typical)

APPLICATIONS

- Local Area Networks
- Point-to-point communications
- Factory automation
- Process control
- Office automation

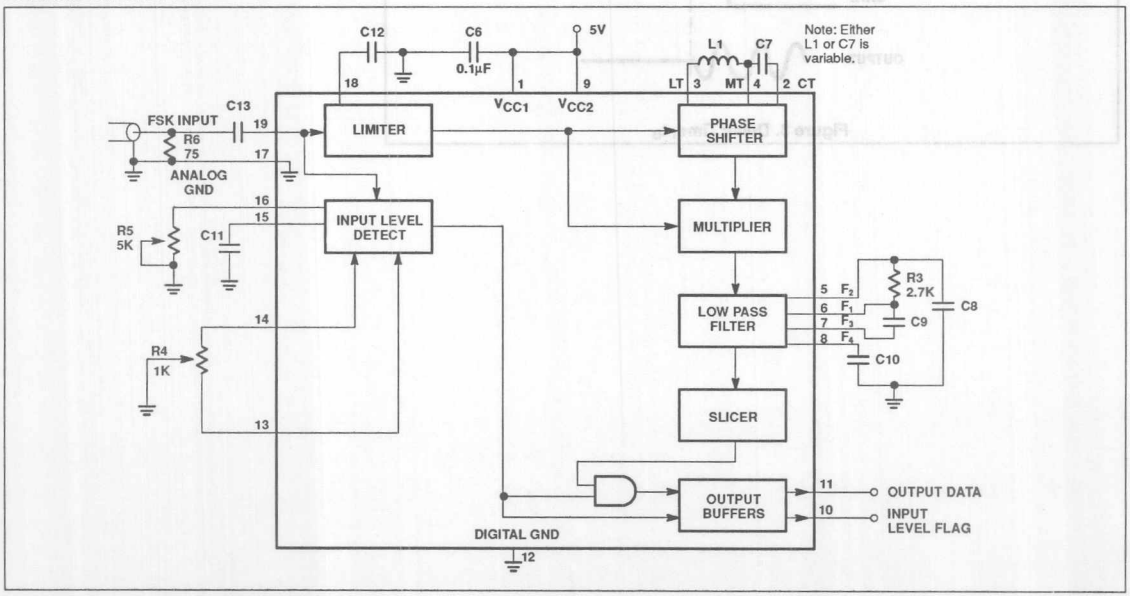
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0°C to +70°C	NE5081N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply voltage	+6	V
V_{IN}	Input voltage range	–0.3 to +V_{CC}	V
I_{DO}	Output (Data, Level detect) Max sink current	20	mA
P_D	Maximum power dissipation, T_A = 25°C, (still-air)[1] N package	1690	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	300	°C
	Max differential voltage between analog and digital grounds	100	mV

NOTE:
1. Derate above 25°C as follows:
   N package at 13.5mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1, 2}$ = 4.75–5.25V. External LC circuit tuned to 5MHz. Input level detect set at 16mV_{RMS}, T_A = 0°C +70°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
f_0	Logic Low Frequency	External LC tuned to 5MHz	3.67	3.75	3.83	MHz
f_1	Logic High Frequency	External LC tuned to 5MHz	6.17	6.25	6.33	MHz
IN_{DL}	Minimum Input Detect Level	Minimum input level that is detected as carrier (See Note 2 in General Description)	5		50	mV_{RMS}
	Logic Levels:					
V_{OL}	Data Output	I_{OL} = 4.0mA V_{IN} > 16mV_{RMS} Freq = f_0			0.4	V
V_{OH}	Data Output	I_{OH} = –400µA V_{IN} > 16mV_{RMS} Freq = f_1	2.4			V
V_{OH}	Data Output	I_{OH} = –400µA V_{IN} < 5mV_{RMS} Freq = f_0	2.4			V
V_{OL}	Input Detect Flag	I_{OL} = 4.0mA V_{IN} = 0V_{RMS}			0.4	V
V_{OH}		I_{OH} = –400µA V_{IN} > 16mV	2.4			V
I_{CC}	Supply Current	V_{CC} = 5.25V (V_{CC1} connected to V_{CC2}) V_{IN} = 1.0V_{RMS} Freq = f_1 or f_0			50	mA
BER	Bit Error Rate	Input Signal > 16mV_{RMS} maximum in-band noise = 1.6mV_{RMS}		10^{-12}	10^{-9}	

AC ELECTRICAL CHARACTERISTICS (AN195, FIGURE 5 WITH A 100KHZ 1V_{P-P})

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
t_B	Delay Time	Input Level Detect Flag	Input On	Figure 1		0.05	1	µs
t_C	Delay Time	Input Level Detect Flag	Input Off	Figure 1	0.5	1.5	2.5	µs
t_D	Delay Time	Output Enabled	Input On	Figure 2			2	µs
t_E	Delay Time	Output Disabled	Input Off	Figure 2	0.5	1.5	2.5	µs
	Required Delay	Carrier Turn Off	Valid Data End		2			µs

High -speed FSK modem receiver NE5081

GENERAL DESCRIPTION

The NE5081 will accept an FSK-encoded signal and provide the demodulated digital data at the output. It is optimized to work at frequencies specified in IEEE 802.4—Token-Passing Single-Channel Phase-Continuous-FSK Bus—(i.e., 3.75MHz and 6.25MHz). However, it will work at other frequencies.[1]

Its normal acceptable input signal level range is from 16mV$_{RMS}$ to 1V$_{RMS}$. This can be adjusted.[3]

The receiver will yield an undetected "Bit Error Rate" of 10^{-9} or lower when receiving signals with a 20dB signal-to-noise ratio. It has a maximum output Jitter of ± 40ns.[3]

NOTES:

1. The receiver can be tuned to accept different frequencies by adjustment of the LC circuit shown in Figure 7. However, the external components have been optimized for 3.75MHz and 6.25MHz. See "Determining Component Values" for use at other frequencies.
2. Input Level Detect
   This is a method of turning off the output of the receiver when the input signal falls below an acceptable level. This level is adjustable within the range given in the electrical specification section. The purpose of this function is to minimize the effect of noise on receiver performance and to indicate when there is an acceptable signal present at the input. All specifications given in this data sheet are with the input level detection set at 16mV$_{RMS}$.
3. Jitter (Definition)
   This is a measure of the ability of the receiver to accurately reproduce the timing of its FSK-coded digital input. The spec indicates the error band in the timing of a logic level change.

NE5081 PIN FUNCTION

PIN	FUNCTION
1	**V_{CC1}:** Should be connected to the 5V supply and Pin 9.
2	**CT:** One end of an external capacitor tthat is used to tune the receiver.
3	**LT:** One end of an indicator that is used to tune the receiver.
4	**MT:** The junction of the capacitor and inductor used for tuning the receiver.
5	**F2**
6	**F1** Pins 5, 6, 7, 8 are used for a low-pass filter to remove carrier
7	**F3** harmonics from the data output.
8	**F4**
9	**V_{CC2}:** Connect to Pin 1 (see Pin 1 function) close to the device.
10	**Input Level Flag:** This pin is used to indicate when there is a signal at the input that is greater than the level set by the input level detection circuitry. A logic high indicates an input greater than the set level.
11	**Data Output:** Supplies T^{2}L level data that corresponds to the FSK input received.
12	**Digital Ground:** Should be connected to digital ground.
13 and 14	**Input Level Detect:** These pins are used to set the level of input signal that the device will accept as valid.
15	**Input Detection Timing:** An external capacitor between this pin and ground is used to determine the time from carrier turn-off to output disable.
16	**Input Detection Timing:** Same as Pin 15, except that a resistor goes between this pin and ground. The values of the C and R depend on the carrier frequency. The values given in this data sheet are for a 5MHz carrier center frequency.
17	**Analog Ground:** Connect to analog ground close to the device.
18	**Input Bypass:** A capacitor between this pin and ground is used to bypass the input bias circuitry.
19	**Input:** The FSK signal from the cable goes to this pin.
20	**No Connection.**

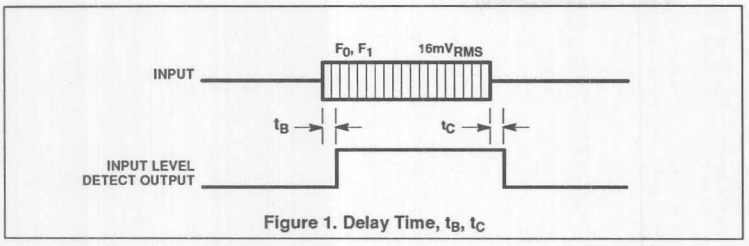


Figure 1. Delay Time, t_B, t_C

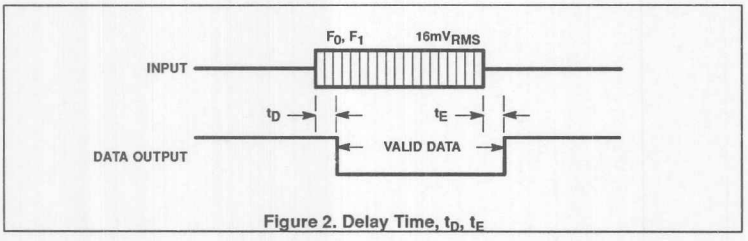


Figure 2. Delay Time, t_D, t_E

Figure 1. Delay Time, t_d, t_c

Figure 2. Delay Time, t_d, t_c

Section 7
Peripheral Drivers

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Symbols and definitions for peripheral drivers 337
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Symbols and definitions for peripheral and display drivers

Linear Products

BCD
Binary Coded Decimal.

$\overline{BI}$/RBO
Blanking Input or Ripple Blanking Output.

CE
Chip Enable

CLR
Clear. Clear command will preset all internal circuits to a predetermined state.

Duty Cycle
Ratio of time on to time off. Generally expressed in percentage.

f_{MAX}
The maximum clock frequency; the maximum input frequency at a clock input for the predictable performance. Above this frequency the device may cease to function.

I_{BIAS}
Input Bias Current. Current into an analog circuit input, specified at a particular voltage level.

I_{CC} ($-I_{CC}$)
Supply Current. The current flowing into the $+V_{CC}$ ($-V_{CC}$) supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.

I_H
Input High Current. The current flowing into or out of an input when a specified HIGH level voltage is applied to that input.

I_{IL}
Input Low Current. The current flowing out of an input when a specified LOW level voltage is applied to that input.

I_{OH}
Output Current Source the device can supply while maintaining a specified voltage output level.

I_{OL}
Output Low Current. The current flowing into an output when it is in the LOW state.

I_{OS}
Output Short-Circuit Current. The current flowing out of an output which is in the High state when that output is shorted to ground.

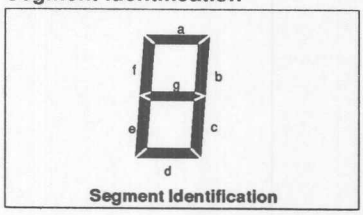
I_S
Source Current. Current flowing into the V_S supply terminal of the device with specified operating conditions.

I_{SEG}
Segment Current. The amount of current supplied to each segment as a display. Current ratios are generally compared to segment 'b'.

LED
Light-Emitting Diode.

$\overline{RBI}$
Ripple Blanking Input.

Segment Identification



Segment Identification

t_H
Hold Time. The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the current logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_{PHL}
Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{PLH}
Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{TREC}
Recovery Time. The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

t_S
Setup Time. The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

Truth Tables
0 = logic level LOW
1 = logic level HIGH
x = don't care condition; has no effect under circuit conditions listed.

Typical Value
The typical value of a particular parameter at 25°C determined by characterization of the device or sampling. Usually indicates that the particular device is not 100% tested for the parameter because it does not vary or can be determined by design and other tested variables. Occasionally typical values are given rather than min/max values because 100% testing would raise the cost of the product to a prohibitive level. If a typical value must be guaranteed to ensure specific operation, custom testing can often be provided at an additional cost to the user.

V_{BR}
Output Breakdown Voltage. Maximum voltage applied to a disabled (off) output to ensure a leakage current less than the specified value.

V_{CC} ($-V_{CC}$)
Supply Voltage. The range of power supply voltage over which the device will operate safely.

Symbols and definitions for peripheral and line drivers

V_F
Forward voltage drop of a device at a specified current level.

V_{IH}
Input High Voltage. The range of input voltages recognized by the device as a logic HIGH.

V_{IL}
Input High Voltage. The range of input voltages recognized by the device as a logic LOW.

V_{IN}
The range of voltage on any input which the device can safely handle or a specified input voltage to the device.

V_{OH}
Output Low Voltage. The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OL}
Output Low Voltage. The maximum guaranteed low voltage at an output terminal sinking the specified load current I_{OL}.

V_{OUT}
The range of voltage on any output which the device can safely handle or a specified output voltage to the device.

V_S
Source Voltage. A separate V_{CC} line depending on part type.

$\overline{XX}$
Negate Bar. When it appears over a function indicates that the "true" or valid condition of that function is a logic LOW level; i.e., LE would require a logic HIGH level to cause a latch enable; $\overline{LE}$ would require a logic LOW level to cause a latch enable.

Addressable relay driver NE/SA5090

DESCRIPTION

The NE/SA5090 addressable relay driver is a high-current latched driver, similar in function to the 9934 address decoder. The device has 8 open-collector Darlington power outputs, each capable of 150mA load current. The outputs are turned on or off by respectively loading a logic "1" or logic "0" into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{CE}$ input line which also serves the function of further address decoding. A common clear input, $\overline{CLR}$, turns all outputs off when a logic "0" is applied. The device is packaged in a 16-pin plastic or Cerdip package.

FEATURES

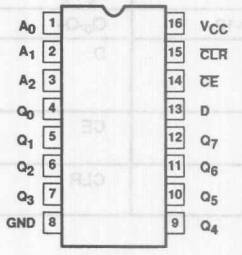
- 8 high-current outputs
- Low-loading bus-compatible inputs
- Power-on clear ensures safe operation
- Will operate in addressable or demultiplex mode
- Allows random (addressed) data entry
- Easily expandable
- Pin-compatible with 9334 (Siliconix or Fairchild)

APPLICATIONS

- Relay driver
- Indicator lamp driver
- Triac trigger
- LED display digit driver
- Stepper motor driver

PIN CONFIGURATION

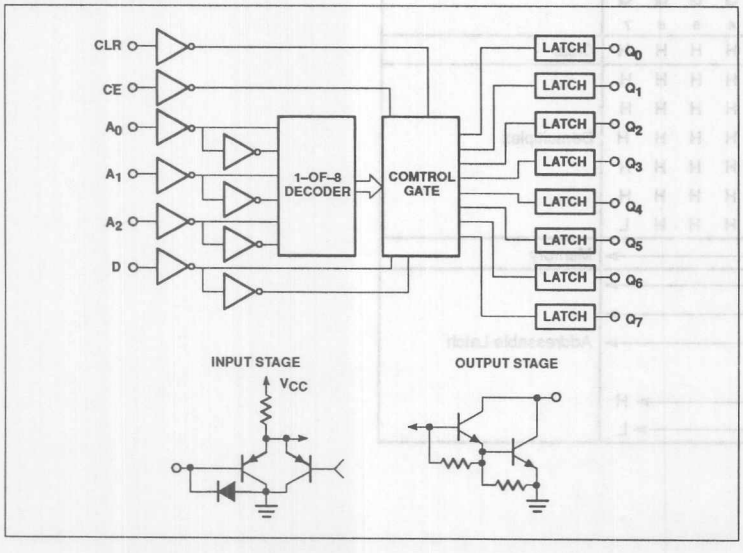
D[1], N Packages



TOP VIEW

NOTE:
1. SOL - Released in Large SO package only.

BLOCK DIAGRAM



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1-3	A_0-A_2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	Q_0-Q_7	The 8 device outputs.
13	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF"
14	CE	The chip enable. When this input is low, the output latches will accept data. When CE goes high, all outputs will retain their existing state, regardless of address of data input condition.
15	CLR	The clear input. When CLR goes low all output switches are turned "OFF". The high data input will override the clear function on the addressed latch.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SOL	0 to +70°C	NE5090D
16-Pin Plastic DIP	0 to +70°C	NE5090N
16-Pin Plastic DIP	-40 to +85°C	SA5090N
16-Pin Plastic SOL	–40 to +85°C	SA5090D

TRUTH TABLE

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A 0	A 1	A 2	Q 0	Q 1	Q 2	Q 3	Q 4	Q 5	Q 6	Q 7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	H	Q_{N-1} →							
H	L	H	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1} →						Addressable Latch
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	L	H	H	H	Q_{N-1} →							H	
H	L	H	H	H	H	Q_{N-1} →							L	

NOTES:
X=Don't care condition
Q_{N-1}=Previous output state
L=Low voltage level/"ON" output state
H=High voltage level/"OFF" output state

Addressable relay driver NE/SA5090

ABSOLUTE MAXIMUM RATINGS

T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V
V_{IN}	Input voltage	-0.5 to +15	V
V_{OUT}	Output voltage	0 to +30	V
I_{GND}	Ground current	500	mA
I_{OUT}	Output current Each output	200	mA
P_D	Maximum power dissipation, T_A=25°C (still-air)[1]		
	N package	1712	mW
	D package	1315	mW
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec. max)	300	°C

NOTES:
1. Derate above 25°C at the following rates:
   F package at 11.1mW/°C
   N package at 13.7mW/°C
   D package at 10.5mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75V to 5.25V, 0°C ≤T_A ≤ +70°C, unless otherwise specified.[1]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					
V_{IH}	High		2.0			V
V_{IL}	Low				0.8	
	Output voltage					
V_{OL}	Low	I_{OL}=150mA, T_A=25°C		1.05	1.30	V
		Over temperature			1.50	
	Input current					
I_{IH}	High	V_{IN}=V_{CC}		<1.0	10	µA
I_{IL}	Low	V_{IN}=0V		-3.0	-250	
I_{OH}	Leakage current	V_{OUT}=28V,		5	250	µA
	Supply current					
I_{CCL}	All outputs low	V_{CC}=5.25V		35	60	mA
I_{CCH}	All outputs high			22	50	
P_D	Power dissipation	No output load			315	mW

NOTES:
1. All typical values are at V_{CC}=5V and T_A=25°C

Addressable relay driver | NE/SA5090

SWITCHING CHARACTERISTICS

V_{CC}=5V, T_A=25°C, V_{OUT}=5V, I_{OUT}=100MA, V_{IL}=0.8V, V_{IH}=2.0V.

SYMBOL	PARAMETER	TO	FROM	MIN	TYP	MAX	UNIT
	Propagation delay time						
t_{PLH}	Low-to-high[1]	Output	$\overline{CE}$		900	1800	ns
t_{PHL}	High-to-low[1]				130	260	
t_{PLH}	Low-to-high[2]	Output	Data		920	1850	ns
t_{PHL}	High-to-low[2]				130	260	
t_{PLH}	Low-to-high[3]	Output	Address		900	1800	ns
t_{PHL}	High-to-low[3]				130	260	
t_{PLH}	Low-to-high[4]	Output	$\overline{CLR}$		920	1850	ns
t_{PHL}	High-to-low[4]						
Switching setup requirements							
$t_{S(H)}$	Setup time high	Chip enable	High data	40			ns
	Setup time low	Chip enable	Low data	50			
$t_{S(A)}$	Address setup time	Chip enable	Address	40			ns
$t_{H(H)}$	Hold time high	Chip enable	High data	10			ns
	Hold time low	Chip enable	Low data	10			
$t_{PW(E)}$	Chip enable pulse width[1]			40			ns

NOTES:
1. See Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data-to-Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address-to-Output timing diagram.
4. See Turn-Off Delay, Clear-to-Output timing diagram.
5. See Setup and Hold Time, Data-to-Enable timing diagram.
6. See Setup Time, Address-to-Enable timing diagram.

FUNCTIONAL DESCRIPTION

This peripheral driver has latched outputs which hold the input date until cleared. The NE5090 has active-Low, open-collector outputs, all of which are cleared when power is first applied. This device is identical to the NE590, except the outputs can withstand 28V.

Addressable Latch Function

Any given output can be turned on or off by presenting the address of the output to be set or cleared to the three address pins, by holding the "D" input High to turn on the selected output, or by holding it Low to turn off, holding the $\overline{CLR}$ input High, and bringing the $\overline{CE}$ input Low. Once an output is turned on or off, it will remain so until addressed again, or until all outputs are cleared by bringing the $\overline{CLR}$ input Low while holding the $\overline{CE}$ input High.

Demultiplexer Operation

By holding the $\overline{CLR}$ and $\overline{CE}$ inputs Low and the "D" input High, the addressed output will remain on and all other outputs will be off.

High Current Outputs

The obvious advantage of this device over other drivers such as the 9334 and N74LS259 is the fact that the outputs of the NE5090 are each capable of 250mA and 28V. It must be noted, however, that the total power dissipation would be over 2.5W if all 8 outputs were on together and carrying 250mA each. Since the total power dissipation is limited by the package to 1W, and since power dissipation due to supply current is 0.25W, the total load power dissipation by the device is limited to 0.75W at room temperature, and decreases as ambient temperature rises.

The maximum die junction temperature must be limited to 165°C, and the temperature rise above ambient and the junction temperature are defined as:

$$T_R=\theta_{JA}\times P_D$$
$$T_J=T_A+t_R$$

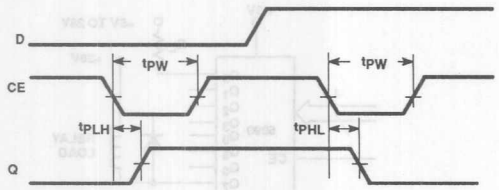
where

For example, if we are using the NE5090 in a plastic package in an application where the ambient temperature is never expected to rise above 50°C, and the output current at the 8 outputs, when on, are 100, 40, 50, 200, 15, 30, 80, and 10mA, we find from the graph of output voltage vs load current that the output voltages are expected to be about 0.92, 0.75, 0.78, 1.04, 0.5, 0.7, 0.9, and 0.4V, respectively. Total device power due to these loads is found to be 473.5mW. Adding the 250mW due to the power supply brings total device power dissipation to 723.5mW. The thermal resistances are 83°C,per W for plastic packages and 100°C per W for Cerdips. Using the equations above we find:

Plastic T_R=83×0.7235=60°C
Plastic T_J =50+60=100°C
Cerdip T_R=100×0.7235=72.4°C
Cerdip T_J =50+72.4=122.4°C

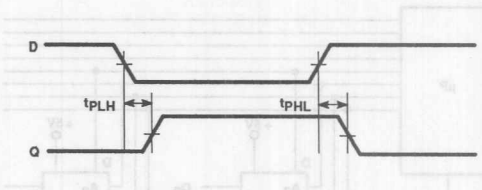
Thus we find that T_J for either package is below the 165°C maximum and either package could be used in this application. The graphs of total load power vs ambient temperature would also give us this same information, although interpreting the graphs would not yield the same accuracy.

TIMING DIAGRAMS



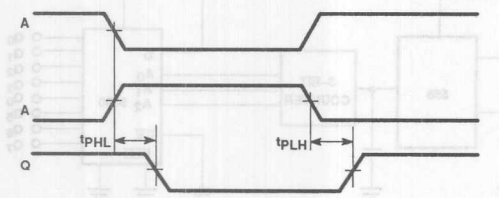
NOTE:
Other Inputs: $\overline{CLR}$ = H, A = Stable

Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width



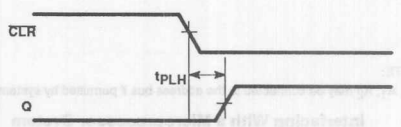
NOTE:
Other Inputs: $\overline{CE}$ = I, $\overline{CLR}$ = H, A = Stable

Turn-On and Turn-Off Delays, Data-to-Output

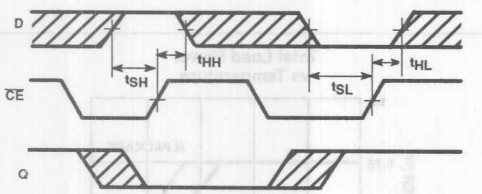


NOTE:
Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

Turn-On and Turn-Off Delays, Address-to-Output

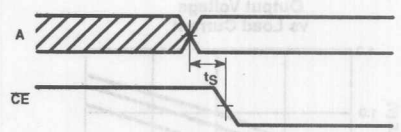


Turn-Off Delays, Clear-to-Output



NOTE:
Other Inputs: $\overline{CLR}$ = H, A = Stable

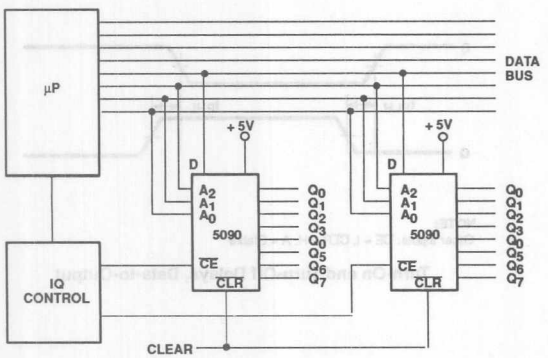
Setup and Hold Time, Data-to-Enable



NOTE:
Other Inputs: $\overline{CLR}$ = H

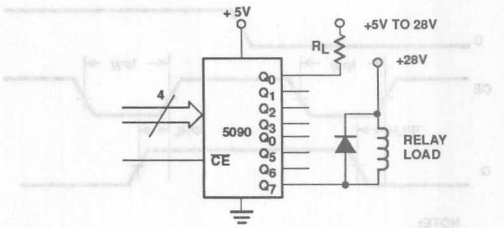
Setup Time, Address-to-Enable

TYPICAL APPLICATIONS

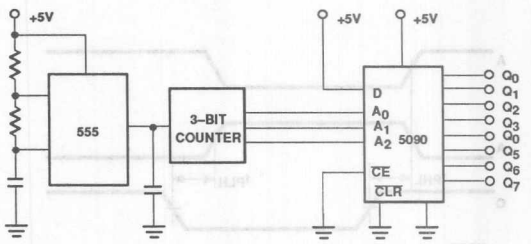


NOTE:
A_0, A_1, A_2 may be connected to the address bus if permitted by system design.

Interfacing With a Microprocessor System



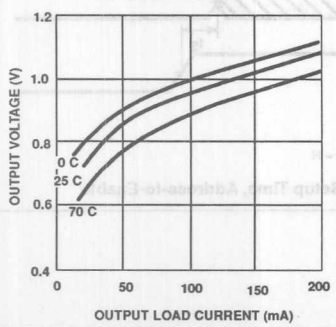
Driving Simple Loads



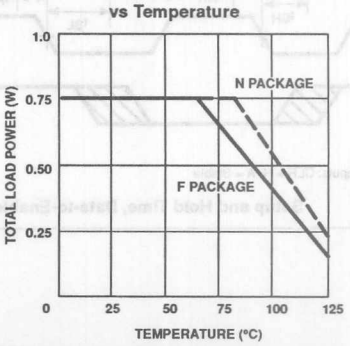
Operating in Demultiplex Mode

TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage vs Load Current



Total Load Power vs Temperature



Addressable peripheral drivers

NE590/591

DESCRIPTION

The NE590/591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has eight Darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic high or logic low into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{CE}$ input line. A common clear input, $\overline{CLR}$, turns all outputs off when a logic low is applied.

The NE590 has eight open-collector Darlington outputs which sink current to ground. The device is packaged in a 16-pin plastic or Cerdip package.

The NE591 has eight open-emitter Darlington outputs which source current to an external load from a common collector line, V_S. This V_S line need not necessarily be the same as the 5V V_{CC} supply. The device is packaged in an 18-pin plastic or Cerdip package.

FEATURES

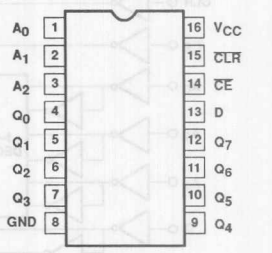
- 8 high current outputs
- Low-loading bus compatible inputs
- Power-on clear ensures safe operation
- NE590 will operate in addressable or demultiplex mode
- Allows random (addressed) data entry
- Easily expandable
- NE590 is pin compatible with 54/74LS259

APPLICATIONS

- Relay driver
- Indicator lamp driver
- Triac trigger
- LED display digit driver
- Stepper motor driver

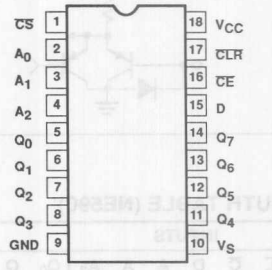
PIN CONFIGURATIONS

N Package



TOP VIEW
NE590

N Package



TOP VIEW
NE591

ORDERING INFORMATION

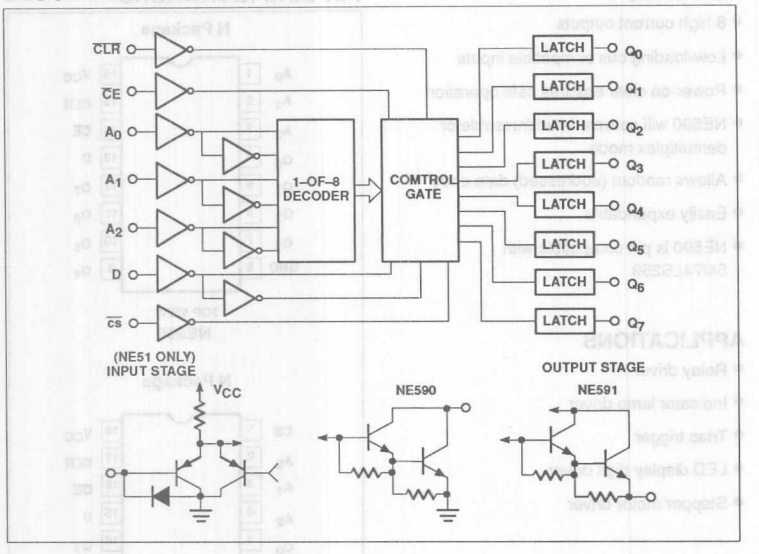
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic	0 to +70°C	NE590N
18-Pin Plastic	0 to +70°C	NE591N

PIN DESIGNATION

590 PIN NO.	591 PIN NO.	SYMBOL	NAME & FUNCTION
1-3	2-4	A_0-A_2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	5-8, 11-14	Q_0-Q_7	The 8 device outputs. The NE590 has open-collector Darlington outputs. The NE591 has open emitter-follower outputs.
13	15	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF" Thus in logic terms, the NE590 inverts data to the relevant output. The NE591 retains true data at the output.
14	16	$\overline{CE}$	The chip enable. When this input is low, the output latches will accept data. When $\overline{CE}$ goes high, all outputs will retain their existing state regardless of address or data input conditions.
15	17	$\overline{CLR}$	The clear input. When $\overline{CLR}$ goes low all output switches are turned "OFF". On the NE590, a high data input will override the clear function on the addressed latch. On the NE591, $\overline{CLR}$ low will override any other condition.
-	1	$\overline{CS}$	The chip select input provides for an additional level of address decoding.
-	10	V_S	The V_S line provides the power to all 8 output devices. It is connected to the collectors of all 8 output transistors. This pin may be connected to the V_{CC} or another supply.

Addressable peripheral drivers | NE590/591

BLOCK DIAGRAM



TRUTH TABLE (NE590)

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	H	Q_{N-1} →							
H	L	H	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1} →						Addressable Latch
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	L	H	H	H	Q_{N-1} →							H	
H	L	H	H	H	H	Q_{N-1} →							L	

NOTES:
X=Don't care condition
Q_{N-1}=Previous output state
L=Low voltage level/"OFF" output state
H=High voltage level/"ON" output state

TRUTH TABLE (NE591)

INPUTS							OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	$\overline{CS}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	X	X	X	X	X	X	L	L	L	L	L	L	L	L	Clear
H	H	H	X	X	X	X	Q_{N-1} →								
H	H	L	X	X	X	X	Q_{N-1} →								Memory
H	L	H	X	X	X	X	Q_{N-1} →								
H	L	L	L	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	L	H	Q_{N-1} →							
H	L	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						Addressable Latch
H	L	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	L	L	H	H	H	Q_{N-1} →							L	
H	L	L	H	H	H	H	Q_{N-1} →							H	

NOTES:
X=Don't care condition
Q_{N-1}=Previous output state
L=Low voltage level/"OFF" output state
H=High voltage level/"ON" output state

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V
V_{IN}	Input voltage	-0.5 to +15	V
V_{OUT}	Output voltage		V
	NE590	0 to +7	
	NE591	0 to V_{CC}	
V_S	Source bus voltage NE591 only	-0.5 to +7	V
V_S-V_{CC}	Source/supply differential voltage NE591 only	-5 to +2	V
I_{OUT}	Output current		
	Each output	300	mA
	All outputs	1000	
P_D	Maximum power dissipation T_A=25°C (still air)		
	NE590[1] N package	1450	mW
	NE591[2] N package	1690	
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature	165	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec max)	300	°C

NOTES:
1. Derate above 25°C at the following rates: N package at 11.6mW/°C
2. Derate above 25°C at the following rates: N package at 13.5mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}=4.75 to 5.25V, 0°C ≥ T_A ≤ 70°C unless otherwise specified. [1,2]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					
V_{IH}	High		2.0			V
V_{IL}	Low				0.8	
	Output voltage					
V_{OL}	Low (NE590 only)	I_{OL}=250mA, T_A=25°C		1.0	1.3	
		Over temperature			1.5	V
V_{OH}	High (NE591 only)	I_{OH}=-250mA, V_{CC}=V_S=5V	2.9			
	Input current					
I_{IH}	High	V_{IN}=V_{CC}		0.1	10	
I_{IL}	Low	V_{IN}=0V				
	$\overline{CE}$ input			-25	-60	µA
	All other inputs			-15	-50	
I_{OH}	Leakage current	V_{OUT}=5.25V		10	250	µA
	Supply current[3]	V_S=V_{CC}=5V				
I_{CCL}	All outputs low					
	NE590			33	50	
	NE591			15	50	
I_{CCH}	All outputs high					mA
	NE590			15	50	
	NE591			30	50	
P_D	Power dissipation	No output load			350	mW

NOTES:
1. All typical values are at V_{CC}=5V and T_A=25°C
2. For the NE591 V_S=V_{CC} in all tests.
3. Supply current for the NE591 is measured with no output load.

SWITCHING CHARACTERISTICS

V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	TO	FROM	NE590			NE591			UNIT
				Min	Typ	Max	Min	Typ	Max	
	Propagation delay time									
t_{PLH}	Low-to-High[1]	Output	$\overline{CE}$		65	150		50	80	ns
t_{PHL}	High-to-Low[1]				115	230		70	120	
t_{PLH}	Low-to-High[2]	Output	Data		65	130		45	70	ns
t_{PHL}	High-to-Low[2]				120	240		65	100	
t_{PLH}	Low-to-High[3]	Output	Address		100	200		45	80	ns
t_{PHL}	High-to-Low[3]				130	260		75	140	
t_{PLH}	Low-to-High[4]	Output	$\overline{CLR}$		65	130				ns
t_{PHL}	High-to-Low[4]							45	140	
t_{PLH}	Low-to-High[1]	Output	$\overline{CS}$					40	80	ns
t_{PHL}	High-to-Low[1]							70	120	
Switching setup requirements										
$t_{S(H)}$		Chip enable	High data	210			100			ns
$t_{S(L)}$		Chip enable	Low data	210			100			ns
$t_{S(A)}$		Chip enable	Address	30			30			ns
$t_{H(H)}$		Chip enable	High data	40			10			ns
$t_{H(L)}$		Chip enable	Low data	30			10			ns
$t_{S(CS)}$		Chip enable	Low chip select				100			ns
$t_{PW(E)}$	Chip enable pulse width[1]			120			120			ns

NOTES:
1. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
4. See Turn-Off Delay, Clear to Output timing diagram.
5. See Setup and Hold Time, Data to Enable timing diagram.
6. See Setup Time, Address to Enable timing diagram.

FUNCTIONAL DESCRIPTION

These peripheral drivers have latched outputs which hold the input data until cleared. The NE590 has active-Low, open-collector outputs, while the NE591 has active-High, uncommitted (open) emitter outputs. All outputs are cleared when power is first applied.

Addressable Latch Function

Any given output can be turned on or off by presenting the address of the output to be set or cleared to the three address pins, by holding the "D" input High to turn on the selected input, or by holding it Low to turn off, holding the $\overline{CLR}$ input High, and bringing the $\overline{CE}$ input Low. Once an output is turned on or off, it will remain so until addressed again, or until all outputs are cleared by bringing the $\overline{CLR}$, $\overline{CE}$, and "D" inputs Low. For NE591, $\overline{CS}$ must be brought Low any time CE is Low if any outputs are to be changed.

Demultiplexer Operation

By bringing the $\overline{CLR}$ and $\overline{CE}$ inputs Low and the "D" input High, the addressed output will remain on and all other outputs will be off. This condition will remain only as long as the output is addressed. For the NE591, the $\overline{CS}$ input must also be Low.

High Current Outputs

The obvious advantage of these devices over the 9334 and N74LS259 (which provide a similar function) is the fact that the NE590 and NE591 are capable of output currents of 250mA at each of their eight outputs. It should be noted, however, that the load power dissipation would be over 2.5W if all 8 outputs were to carry their full rated load current at one time. Since the total power dissipation is limited by the package to 1W, and since the power dissipation due to supply current is 0.25W, the total load power dissipation by the device is limited to 0.75W, and decreases as ambient temperature rises.

The maximum die junction temperature must be limited to 165°C, and the temperature rise above ambient and the junction temperature are defined as:

$$t_R = \theta_{JA} \times P$$
$$t_J = t_A + t_R$$

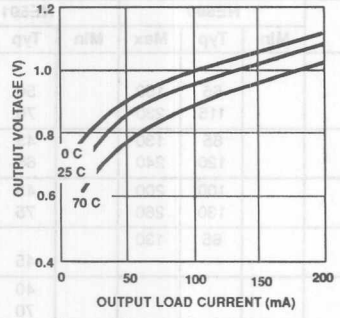
where

For example, if we are using the NE5090 in a plastic package in an application where the ambient temperature is never expected to rise above 50°C, and the output current at the 8 outputs, when on, are 100, 40, 50, 200, 15, 30, 80, and 10mA, we find from the graph of output voltage vs load current that the output voltages are expected to be about 0.92, 0.75, 0.78, 1.04, 0.5, 0.7, 0.9, and 0.4V, respectively. Total device power due to these loads is found to be 473.5mW. Adding the 250mW due to the power supply brings total device power dissipation to 723.5mW. The thermal resistances are 83°C per W for plastic packages and 100°C per W for Cerdips. Using the equations above we find:

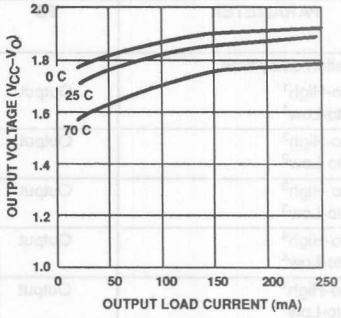
Plastic $t_R = 83 \times 0.7235 = 60°C$
Plastic $t_J = 50 + 60 = 100°C$
Cerdip $t_R = 100 \times 0.7235 = 72.40°C$
Cerdip $t_J = 50 + 72.4 = 122.4°C$

Thus we find that t_J for either package is below the 165°C maximum and either package could be used in this application. The graphs of total load power vs ambient temperature would also give us this same information, although interpreting the graphs would not yield the same accuracy.

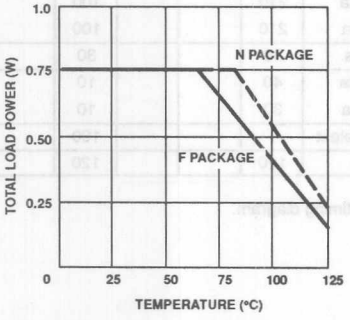
TYPICAL PERFORMANCE CHARACTERISTICS



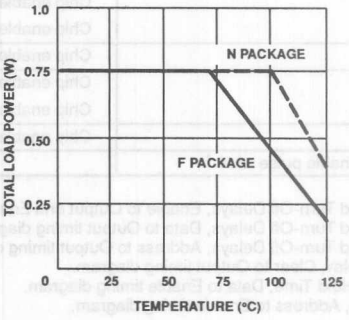
Output Voltage vs Load Current (NE590)



Output Voltage Drop vs Load Current (NE591)

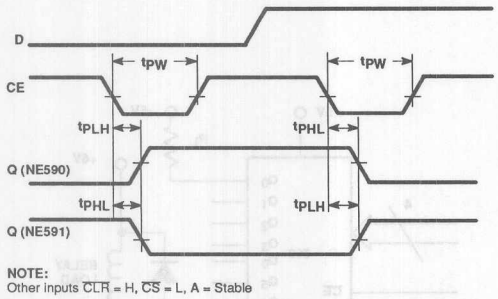


Total Load Power vs Temperature (NE590)



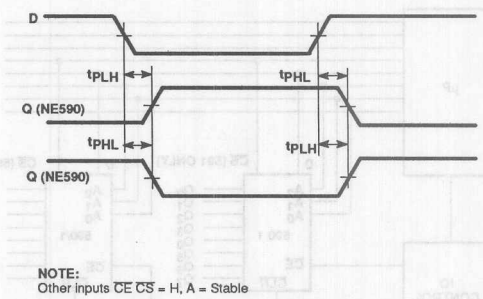
Total Load Power vs Temperature (NE591)

TIMING DIAGRAMS



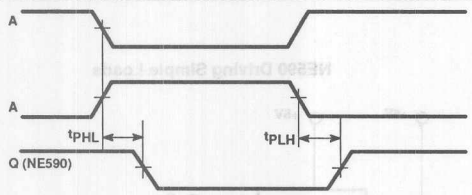
NOTE:
Other inputs $\overline{CLR}$ = H, $\overline{CS}$ = L, A = Stable

Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width



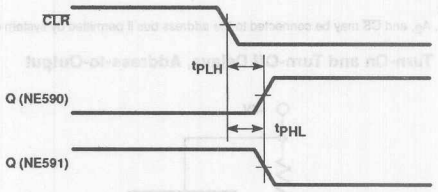
NOTE:
Other inputs $\overline{CE}$ $\overline{CS}$ = H, A = Stable

Turn-On and Turn-Off Delays, Data-to-Output



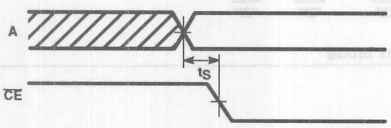
NOTE:
Other inputs $\overline{CE}$ = L, $\overline{CR}$ = L, D = H

Turn-On and Turn-Off Delays, Address-to-Output



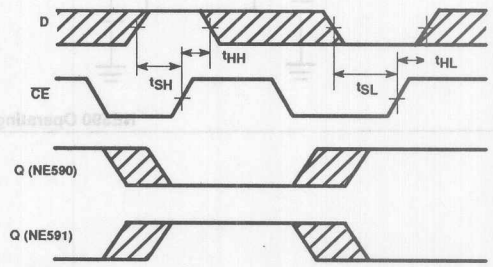
NOTE:
Other inputs $\overline{CS}$ = H, $\overline{CE}$ = H

Turn-On and Turn-Off Delays, Clear-to-Output



NOTE:
Other inputs $\overline{CLR}$ = H, $\overline{CS}$ = L

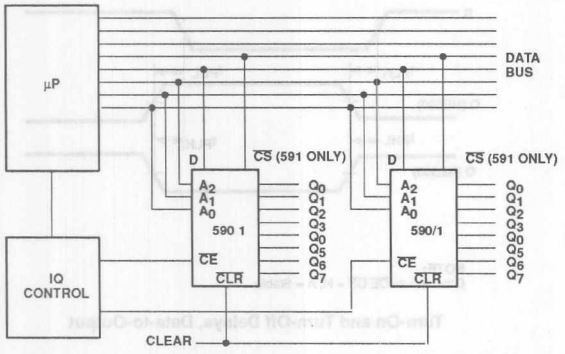
Set-Up Time, Address-to-Enable



NOTE:
Other inputs $\overline{CLR}$ = H, $\overline{CS}$ = L, A = Stable

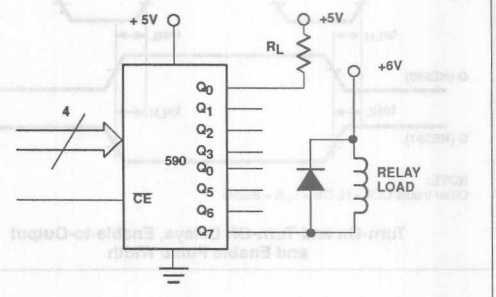
Set-Up and Hold Time, Data-to-Enable

TYPICAL APPLICATIONS

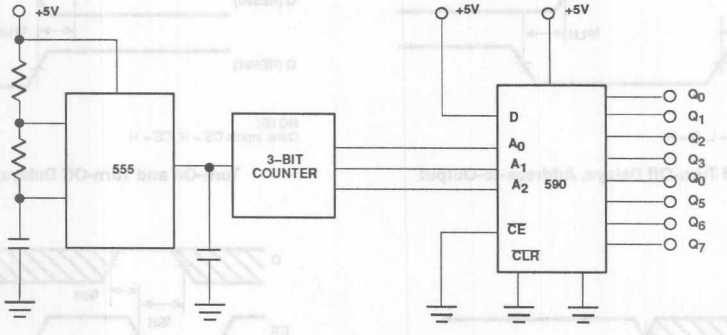


NOTE:
A_0, A_1, A_2, and $\overline{CS}$ may be connected to the address bus if permitted by system design.

Turn-On and Turn-Off Delays, Address-to-Output



NE590 Driving Simple Loads



NE590 Operating in Demultiplex Mode

Section 8
Display Drivers

INDEX

NE587	LED decoder/driver	355
NE/SA594	Vacuum fluorescent display driver	364

LED decoder/driver

NE587

DESCRIPTION

The NE587 is a latch/decoder/driver for 7-segment common anode LED displays. The NE587 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES

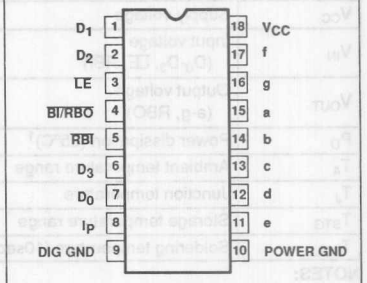
- Latched BCD inputs
- Low loading bus-compatible inputs
- Ripple-blanking on leading- and/or trailing-edge zeros

APPLICATIONS

- Digital panel motors
- Measuring instruments
- Test equipment
- Digital clocks
- Digital bus monitoring

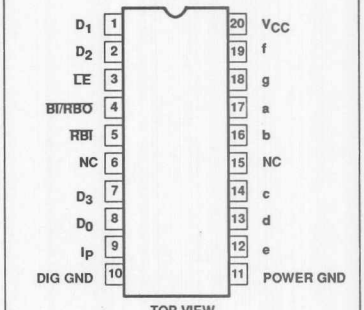
PIN CONFIGURATIONS

N Package



TOP VIEW

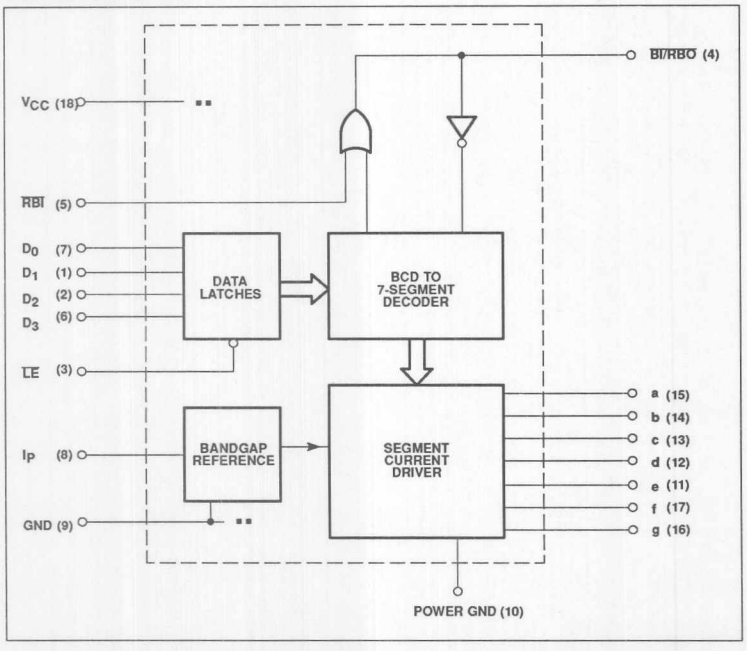
D[1] Package



TOP VIEW

NOTE:
1. SOL and non-standard pinout.

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL	0 to +70°C	NE587D[1]
18-Pin Plastic DIP	0 to +70°C	NE587N

NOTES:
1. SOL and non-standard pinout

ABSOLUTE MAXIMUM RATINGS

T_A=25°C unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V
V_{IN}	Input voltage (D_0-D_3, $\overline{LE}$, $\overline{RBI}$)	-0.5 to +15	V
V_{OUT}	Output voltage (a-g, RBO)	-0.5 to +7	V
P_D	Power dissipation (25°C)[1]	1000	mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Soldering temperature (10sec max)	300	°C

NOTES:

1. Derate power dissipation as indicated
   N package—95°C/W above 55°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}=4.75 to 5.25V, 0°C < T_A < 70°C. Typical values are at V_{CC}=5V, T_A=25°C, R_P=1kΩ (±1%), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All inputs except $\overline{BI}$	2.0		15	V
		$\overline{BI}$	2.0		5.5	
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp voltage	I_{IN}=-12mA, T_A=25°C			-1.5	V
I_{IH}	Input high current	Inputs D_0-D_3, $\overline{LE}$, $\overline{RBI}$				µA
		V_{IN}=2.4V		1.0	10	
		V_{IN}=15V		15	15	
		Input $\overline{BI}$ (Pin 4)		10	100	µA
		$\overline{RBI}$=H				
		V_{IN}=V_{CC}=5.25V				
I_{IL}	Input low current	V_{IN}=0.4V, Inputs D_0-D_3		-5		
		$\overline{LE}$, $\overline{RBI}$		-200		µA
		Input $\overline{BI}$				
		V_{CC}=5.25V		-0.7		mA
		$\overline{RBI}$=H, V_{IN}=0.4V				
V_{OL}	Output low voltage	Output $\overline{RBO}$		0.2	0.5	V
		I_{OUT}=3.0mA				
V_{OH}	Output high voltage	Output $\overline{RBO}$				
		I_{OUT}=-50µA	3.5	4.5		V
		$\overline{RBI}$=H				
I_{OUT}	Output segment "ON" current	Outputs "a" through "g"	20	25	30	mA
		V_{OUT}=2.0V				
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment	0.90	1.00	1.10	
		V_{OUT}=2.0V				
I_{OFF}	Output segment "OFF" current	Outputs "a" through "g"				
		V_{OUT}=5.0V		20	250	µA
I_{CCO}	Supply current	V_{CC}=5.25V				
		All outputs "ON"		33	55	mA
		V_{OUT}>1V				
I_{CCI}	Supply current	V_{CC}=5.25V				
		All outputs blanked		50	70	mA

NOTES:

NE587 Programming:

The NE587 output current can be programmed, provided a program resistor, R_P, be connected between I_P (Pin 8) and Ground (Pin 9). The voltage at I_P (Pin 8) is constant (≈1.3V). Thus, a current through R_P is $I_P \approx 1.3V/R_P$, as shown in Figure 5. I_O/I_P is 20 in the 15 to 50mA output current range.

AC ELECTRICAL CHARACTERISTICS

V_{CC}=5V, T_A=25°C, R_L=130Ω, C_L=30pF including probe capacity.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{DAV}	Propagation delay Figure 2	From data to output		135		ns
t_{DAV}	Propagation delay Figure 3	From $\overline{LE}$ to output		135		ns
t_W	Latch enable pulse width Figure 4		30			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{LE}$	20			ns
t_H	Latch enable hold time Figure 4	From $\overline{LE}$ to data	0			ns

NOTES:
$t_{DAV}=(t_{HL}+t_{LH})$

TRUTH TABLE

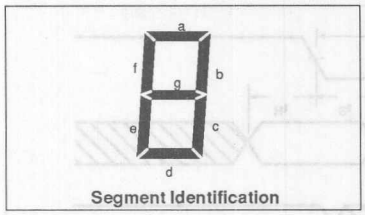
BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
-	H	*	X	X	X	X	STABLE							**	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	-
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	Blank
**BI	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	Blank

NOTES:
H=HIGH voltage level, output is "OFF"
L=LOW voltage level, output is "ON"
X=Don't care
* The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
** $\overline{RBO}$/$\overline{BI}$ used as an input overrides all other input conditions.

NE587 PROGRAMMING

587 output current can be programmed by using a programming resistor, RP, connected between RP (Pin 8) and GND (Pin 9). The voltage at RP (Pin 8) is constant (κ 1.40V). A partial schematic of the voltage reference used in the NE587 is shown in Figure 1.

Output current to program current ratio, I_O/I_P, is 20 in the 15mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high-impedance source such as an I_{OUT} DAC used to control display brightness.



Segment Identification

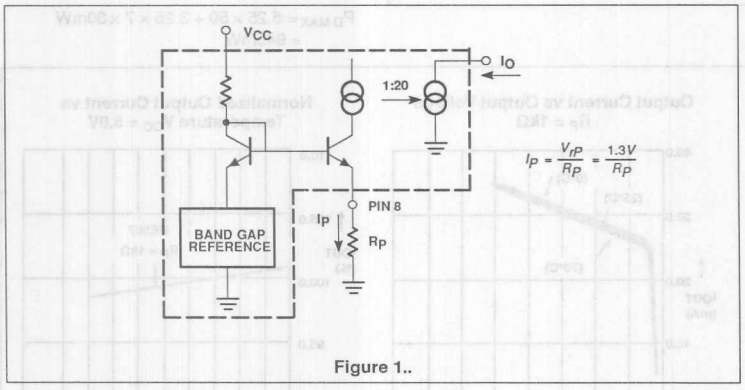


Figure 1..

TIMING DIAGRAMS

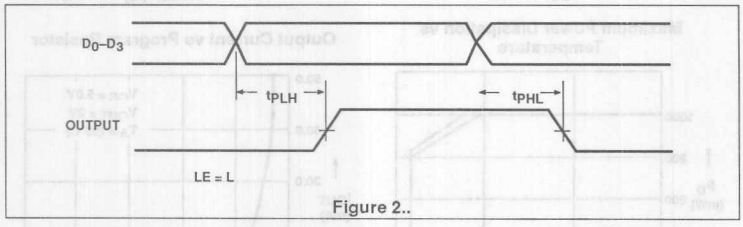


Figure 2..

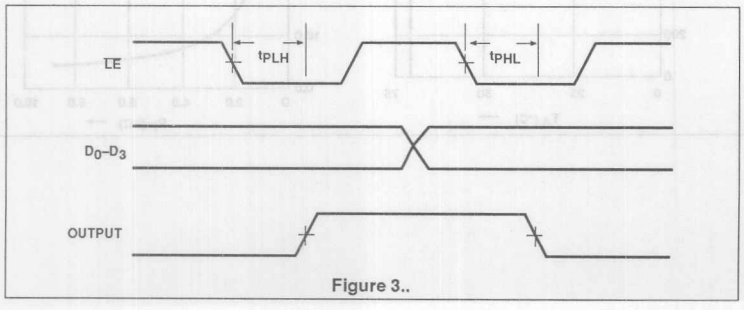


Figure 3..

POWER DISSIPATION CONSIDERATIONS

D displays are power-hungry devices, and inevitably, somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation; but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large-size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant-current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible, consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to Figure 6, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC}	Supply voltage to driver
V_S	Supply voltage to display
I_{CC}	Quiescent supply current of driver
I_{SEG}	LED segment current
V_F	LED segment forward voltage at I_{SEG}
K_{DC}	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

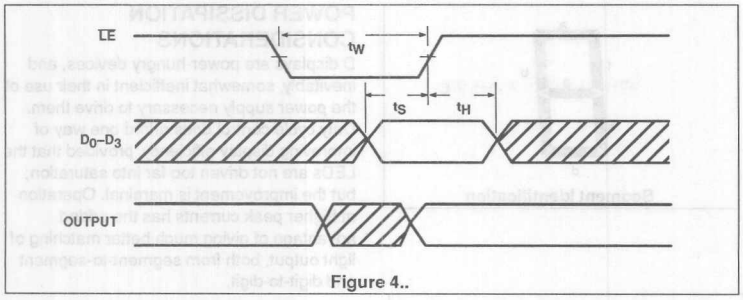


Figure 4..

These voltages are all for single-diode displays. Some early red displays had 2 series LEDs per segment; hence the forward voltage drop was around 3.5V.

Thus, a maximum power dissipation calculation when all segments are on, is:

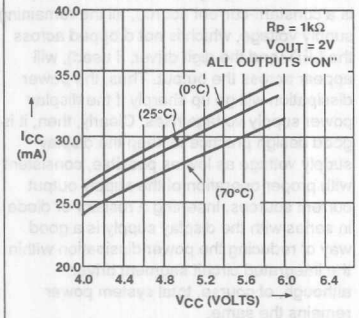
$$P_D = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{SEG} \times K_{DC}mW$$

Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$

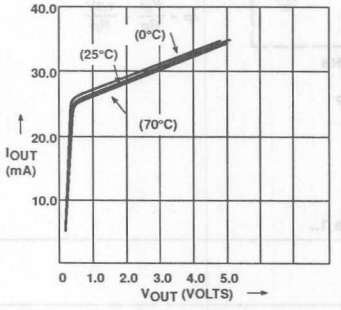
$P_{D\,MAX} = 5.25 \times 50 + 3.25 \times 7 \times 30mW$
$= 945mW$

TYPICAL PERFORMANCE CURVES

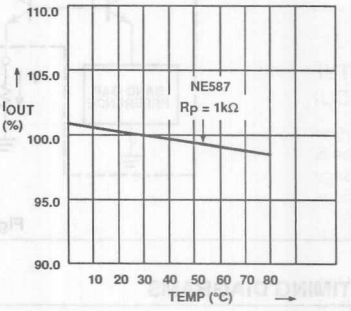
Supply Current vs Supply Voltage



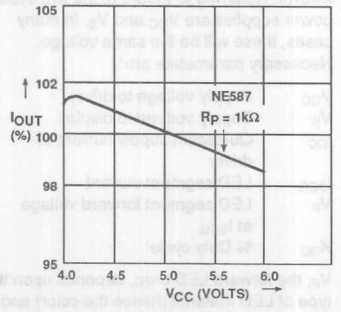
Output Current vs Output Voltage
$R_P = 1k\Omega$



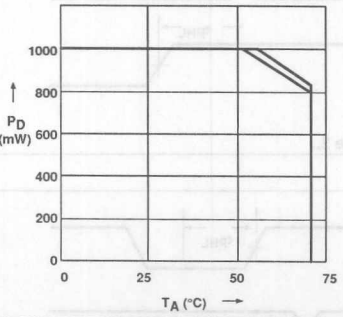
Normalized Output Current vs Temperature $V_{CC} = 5.0V$



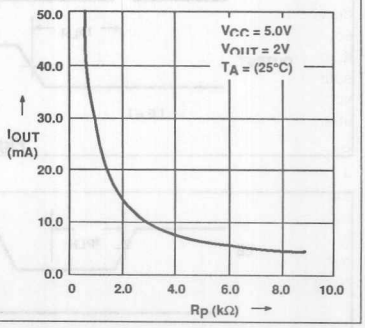
Normalized Output Current vs Supply Voltage $V_O = 2V$, $T_A = 25°C$

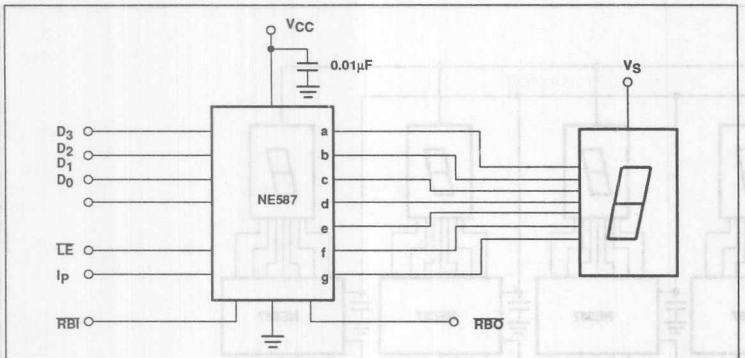


Maximum Power Dissipation vs Temperature



Output Current vs Program Resistor





NOTE:
Decoupling capacitor on V_{CC} should be 0.01µF ceramic.

Figure 5.. Driving a Single Digit

TYPICAL PERFORMANCE CURVES

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$P_{D\,MAX} = 5.0 \times 30 + 3.00 \times 5 \times 25mW$
$= 525mW$

Operating temperature range limitations can be deduced from the power dissipation graph. (See Typical Performance Characteristics.)

However, a major portion of this power dissipation ($P_{D\,MAX}$) is because the current source output is operating with 3.25V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst-case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{SEG}} \approx 10\Omega \ (\frac{1}{2} W \ rating)$$

assuming worst case I_{SEG} of 30mA.

Hence now

$P_{D\,MAX} = V_{CC} \times I_{CC} +$
$(V_S - V_V - R_X \times 7 \times I_{SEG})$
$\times 7 \times I_{SEG} \times K_{DC}$
$= 5.25 \times 50 + 1.25 \times$
$7 \times 30mW$
$= 525mW$

and

$P_{D\,av} = 5.0 \times 30 + 1.25 \times 5 \times 25$
$= 306\ mW.$

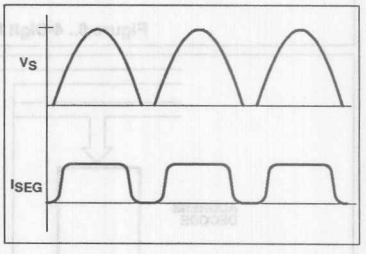
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$V_S - V_F - nV_d$, $V_D \approx 0.8V$

Where n is the number of diodes used, power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in Figure 9. For example a Darlington PNP or NPN emitter-follower may be preferable. Figure 8 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact, a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V_{RMS} works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With
$V_S = 4.9V$ peak
$V_F = 2.0V$

The duty cycle is approximately 60%.

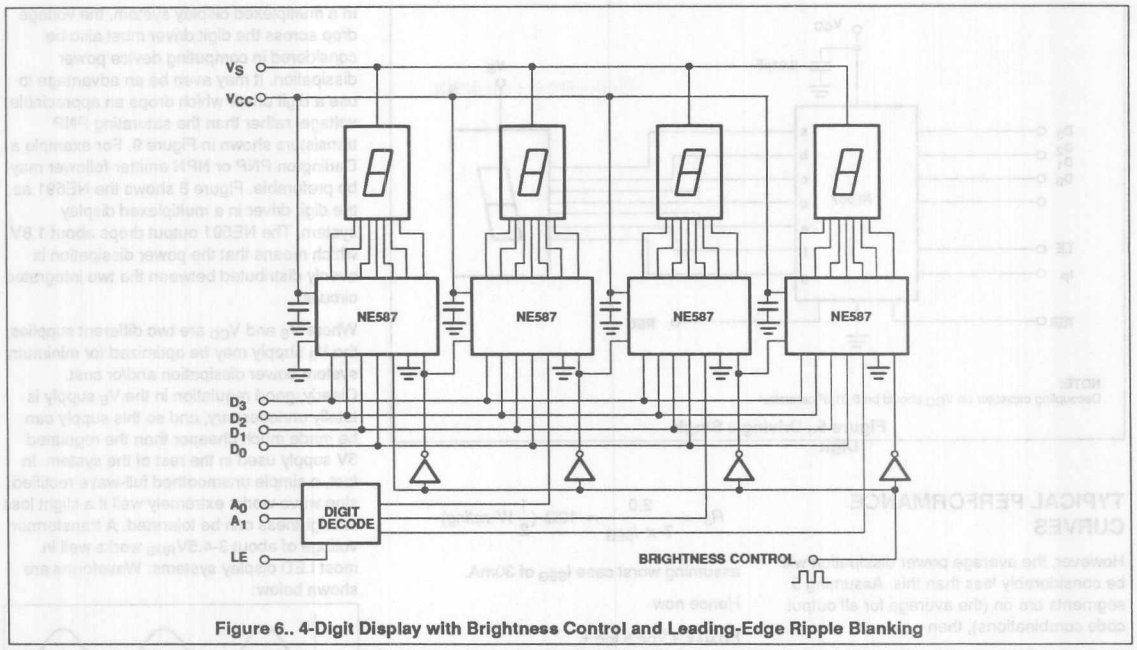


Figure 6.. 4-Digit Display with Brightness Control and Leading-Edge Ripple Blanking

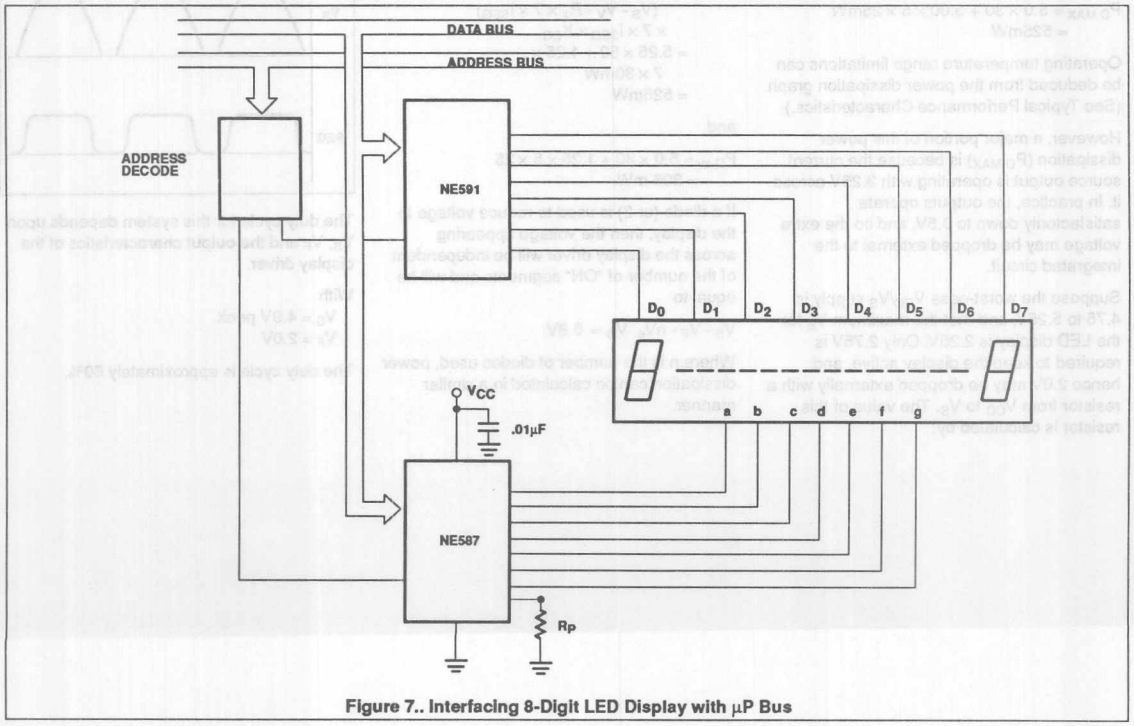


Figure 7.. Interfacing 8-Digit LED Display with µP Bus

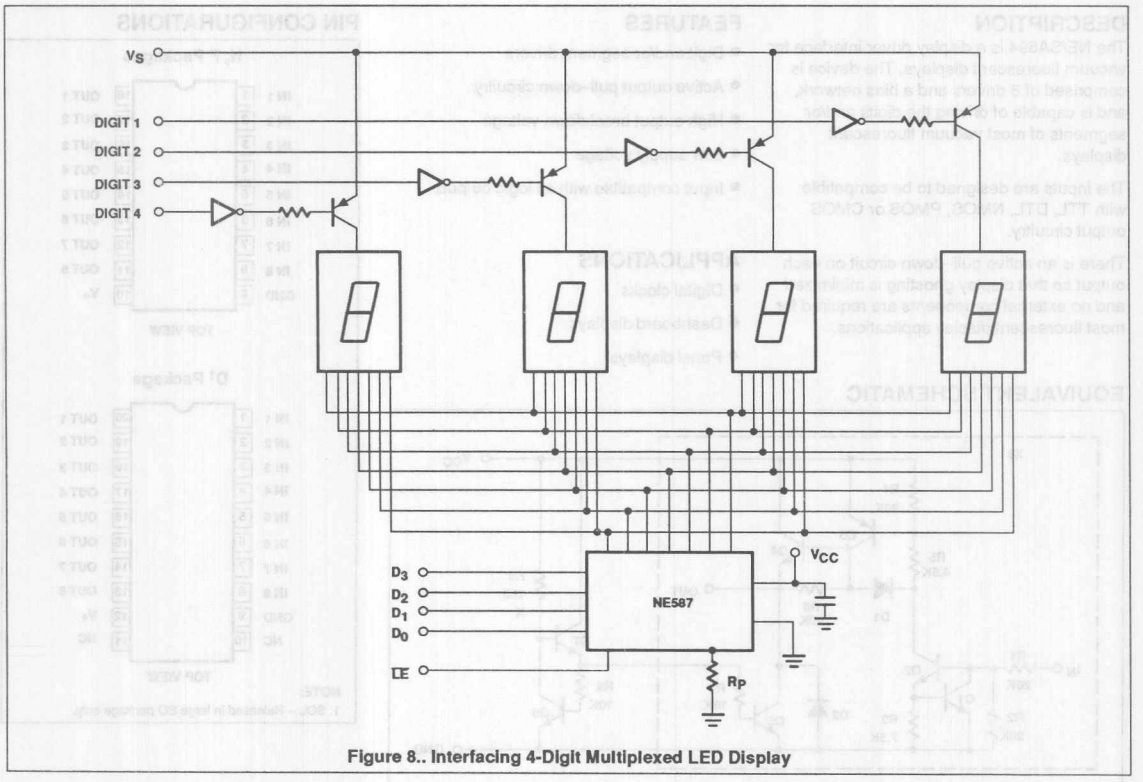


Figure 8.. Interfacing 4-Digit Multiplexed LED Display

Vacuum fluorescent display driver

NE/SA594

DESCRIPTION

The NE/SA594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network, and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

There is an active pull–down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.

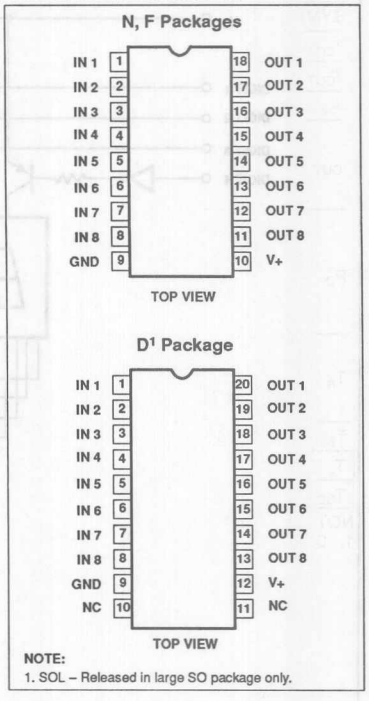
FEATURES

- Digit and/or segment drivers
- Active output pull–down circuitry
- High output breakdown voltage
- Low supply voltage
- Input compatible with all logic outputs

APPLICATIONS

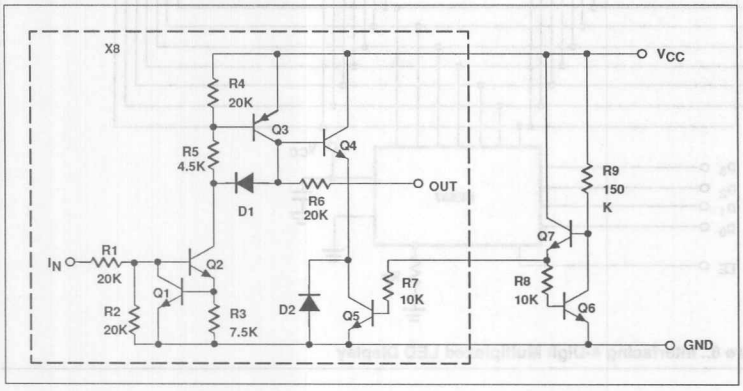
- Digital clocks
- Dashboard displays
- Panel displays

PIN CONFIGURATIONS



NOTE:
1. SOL – Released in large SO package only.

EQUIVALENT SCHEMATIC



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18–Pin Plastic DIP	0 to +70°C	NE594N
18–Pin Ceramic DIP	0 to +70°C	NE594F
20–Pin Plastic SO	0 to +70°C	NE594D
18–Pin Plastic DIP	–40°C to +85°C	SA594N
18–Pin Ceramic DIP	–40°C to +85°C	SA594F

ABSOLUTE MAXIMUM RATINGS (at 25°C, unless otherwise noted)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	45	V
V_{OUT}	Output voltage	V_{CC}	
V_{IN}	Input voltage	–0.3, +20	V
I_{OUT}	Output current		
	Each output	50	mA
	All outputs	200	mA
P_D	Maximum power dissipation, T_A=25°C (still–air)[1]		
	F package	1500	mW
	N package	1690	mW
	D package	1390	mW
T_A	Operating ambient temperature range		
	NE594	0 to 70	°C
	SA594	–40 to +85	°C
T_{STG}	Storage temperature range	+65 to +150	°C
T_J	Maximum junction temperature	–150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. Derate above 25°C, at the following rates:
   F package at 12.0mW/°C
   N package at 13.5mW/°C
   D package at 11.1mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}=+4.75 to +40V, T_A= 0 to 70°C (NE), T_A= –40 to +85°C (SA), unless otherwise stated.

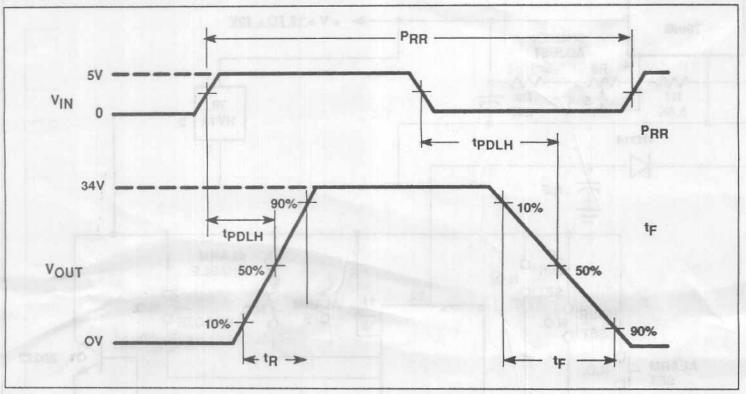
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ	Max	
V_{CC}	Supply voltage range			4.75	35	40	V
I_{CCH}	Supply current (all outputs high)	V_{CC}=40V, V_{IN}=3.5V			3	6	mA
I_{CCL}	Supply current (all outputs low)	V_{CC}=40V, V_{IN}=0.4V			0.4	1	mA
V_{IN}	Input voltage range			0		15	V
V_{IH}	Input voltage to ensure logic "1"			2.6			V
V_{IL}	Input voltage to ensure logic "0"					0.8	V
I_{IH}	Input current to ensure logic "1"			100			µA
I_{IL}	Input current to ensure logic "0"					10	µA
I_{IN}	Input current	V_{IN}=2.6V			60	130	µA
		V_{IN}=5.0V			180	330	µA
		V_{IN}=15.0V			.68	1.3	mA
V_{OH}	Output high voltage	V_{IN}=3.5V, I_{OUT}=–25mA	T_A=25°C	V_{CC} –1.5	V_{CC} –1.1		V
			Over temp.	V_{CC} –2	V_{CC} –1.3		V
		V_{OUT} with respect to V_{CC}					
V_{OH}	Output high, no load voltage	V_{IN}=3.5V, I_{OUT}=0, T_A=25°C, V_{OUT} with respect to V_{CC}		V_{CC} –1	V_{CC} –0.8		V
V_{OFF}	Output 'OFF' voltage level	V_{IN}=0.8V, I_{OUT}=0			10	200	mV
I_{OH}	Available output current	V_{CC}=35V, V_{IN}=3.5V, V_{OUT}=30V, T_A=25°C		–35			mA
I_{OUT}	Output pulldown current	V_{CC}=V_{OUT}=35V, Inputs open		100	200	400	µA
I_{CEX}	Output leakage current	T_A=25°C, V_{IN}=0.4V V_{CC}=40V, V_{OUT}=0V			–1 –1		µA

AC ELECTRICAL CHARACTERISTICS

V_{CC}=35V, T_A=25°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_{PLH}	Propagation delay—low–to–high output transition	50% V_{IN} to 50% V_{OUT}		1	5	µs
t_{PHL}	Propagation delay—high–to–low output transition	50% V_{IN} to 50% V_{OUT}		3	10	µs
t_R	Output rise time	10% V_{OUT} to 90% V_{OUT}		0.5	3	µs
t_F	Output fall time	90% V_{OUT} to 10% V_{OUT}		1.5	5	µs

SWITCHING TIMES OF DRIVERS



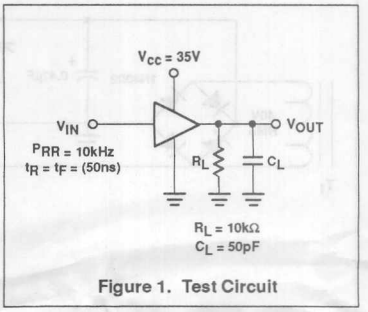
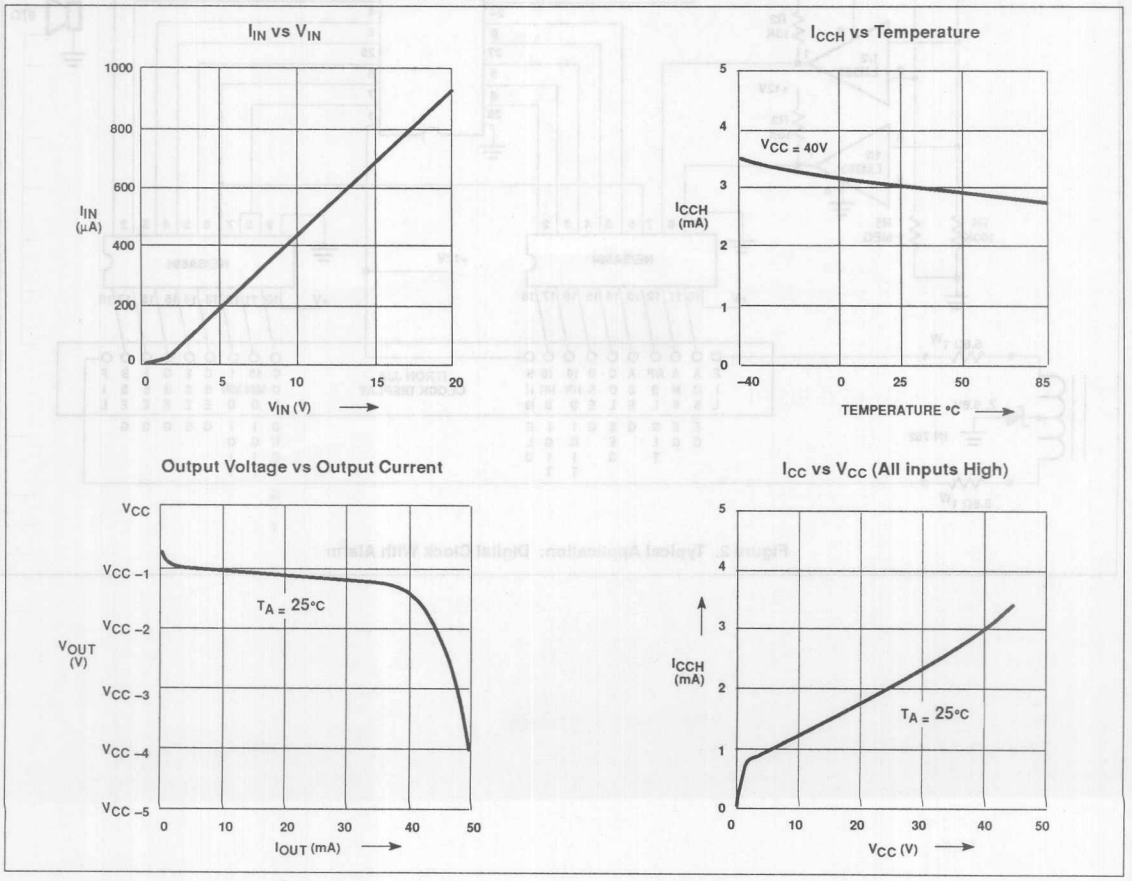


Figure 1. Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS



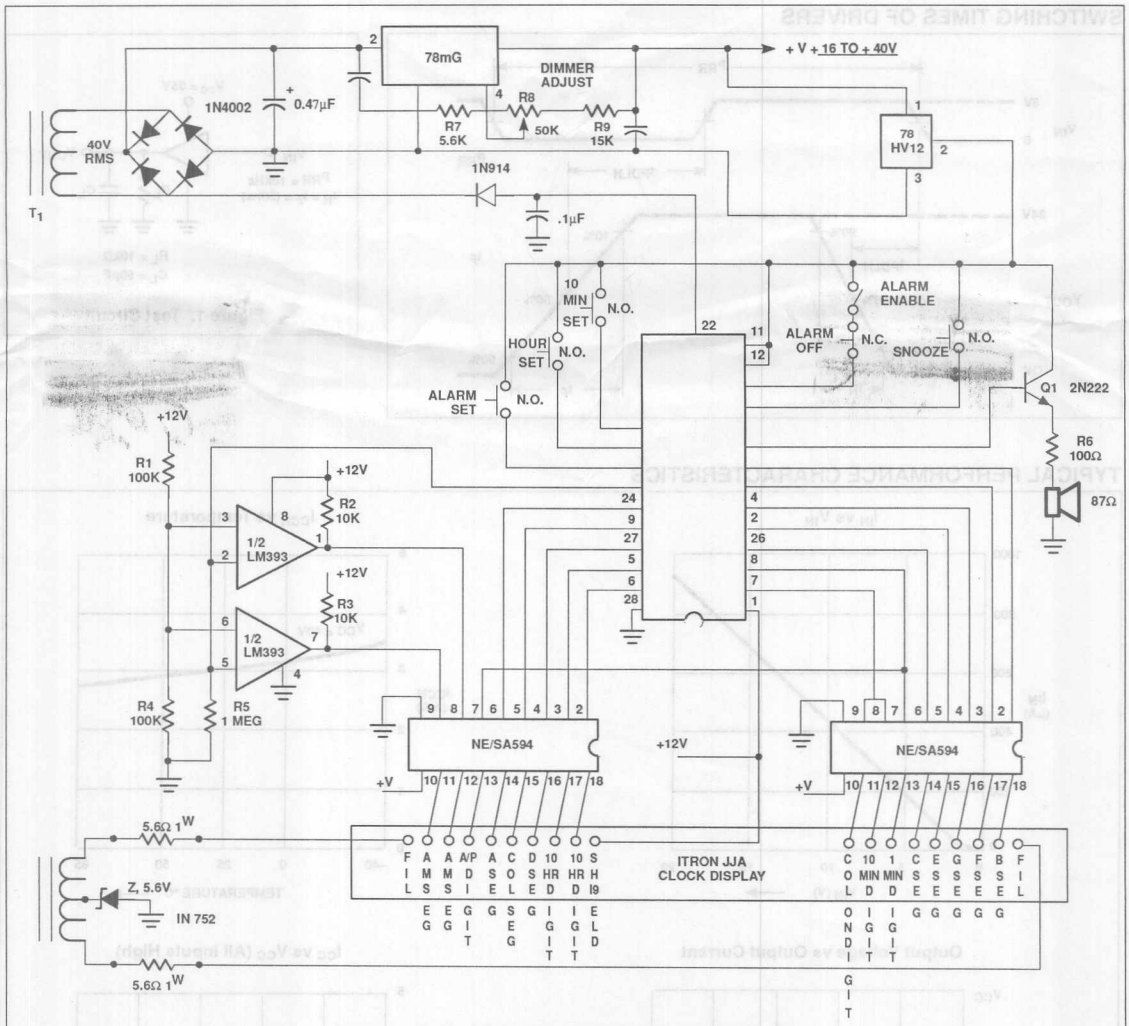


Figure 2. Typical Application: Digital Clock With Alarm

Section 9
Analog-to-Digital Converters

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Symbols and definitions for analog-to-digital converters (ADCs)

Absolute Accuracy Error

Absolute Accuracy Error at a given output code is the difference between the theoretical analog input voltage required to produce a given output code and the actual analog input voltage required to produce the same code. Since the same output code is produced by a finite band of input voltages, the "analog input voltage required" is defined as the midpoint of the band of input voltages that will produce that code..

Absolute accuracy error includes gain error, offset error and relative accuracy error and is typically expressed in LSBs or in percent of full-scale range (FSR).

Conversion Time

Conversion Time is the time required for a conversion cycle to be completed while meeting the specification.

Differential Linearity Error

Differential Linearity Error of an ADC is the in the analog value of code width between adjacent digital codes over the full range of digital output values.

Full-Scale Range (FSR)

The Full-Scale Range (FSR) of an ADC is the scale factor that determines the nominal conversion relationship; e.g., 2.5V span for a full-scale change in a fixed reference converter.

In a unipolar ADC of n bits, the ideal first code transition occurs at FSR x 2^{-N} x 1/2 and the final code transition occurs at FSR x ($1-2^{-N}$ x 3/2). The ideal code transition from code C-1 to C occurs at FSR x ($C-1/2$) x $1/2^N$.

In a bipolar ADC, the ideal first code transition occurs at FSR x (2^N-1) x 1/2 and the final code transition occurs at FSR x ($1-3 \times 2^{-N}$) x 1/2.

Gain Error

Gain Error is the deviation between the ideal and actual analog input voltage to cause the final code transition to a full-scale output code after nulling offset error. It is usually expressed in LSBs or in percent of FSR.

Integral Non-Linearity

Same as Relative Accuracy.

Least Significant Bit

The Least Significant Bit (LSB) is the lowest-order bit and carries the smallest weight. In an n-bit ADC, the weight of the LSB is FSR/(2^N-1). It is the smallest change that can be resolved by an n-bit ADC.

Missing Code

A missing code is a code combination that does not appear at the ADC's output.

Most Significant Bit

The Most Significant Bit (MSB) is the highest order bit and carries the most weight. The weight of the MSB is 1/2 the full-scale range of the ADC.

Offset Error (Unipolar and Bipolar)

In an ADC, unipolar offset is the difference between the actual analog input voltage that causes the first code transition point and the ideal value to cause the first code transition, which is 1/2 LSB above analog ground. Similarly for bipolar offset, it is the difference between the actual analog input voltage that causes the code transition from 1 LSB below half-scale to half-scale and the ideal analog value to cause the same code transition which is 1/2 LSB above Analog Ground

Power Supply Sensitivity

The Power Supply Sensitivity of an ADC is the change in the code transition points with changes in the DC power supply voltages. It is usually expressed in LSBs/V or in %FSR/V.

Quantization Error

ADCs of any resolution exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be eliminated.

Relative Accuracy

Relative Accuracy Error is the deviation of the ADCs actual code transition points from the ideal code transition points on a straight line which connects the ideal first code transition point and the final code transition point, after nulling the offset error and gain error. It is generally expressed in LSBs or in percent of FSR.

Resolution

Resolution of an ADC is the number of bits at its output. The number of output states is 2^N where N is the resolution of the converter.

Temperature Coefficients

In general, Temperature Coefficients are expressed either in ppm/°C or in LSBs/°C or as a change in the specified parameter over the temperature range. Measurements are usually made at room temperature and at the temperature extremes of the specified temperature range; the Temperature Coefficient is defined as the change in the parameter from its room temperature value divided by the corresponding temperature change.

CMOS 8-bit A/D converters — ADC0803/4-1

DESCRIPTION

The ADC0803 family is a series of three CMOS 8-bit successive approximation A/D converters using a resistive ladder and capacitive array together with an auto-zero comparator. These converters are designed to operate with microprocessor-controlled buses using a minimum of external circuitry. The 3-State output data lines can be connected directly to the data bus.

The differential analog voltage input allows for increased common-mode rejection and provides a means to adjust the zero-scale offset. Additionally, the voltage reference input provides a means of encoding small analog voltages to the full 8 bits of resolution.

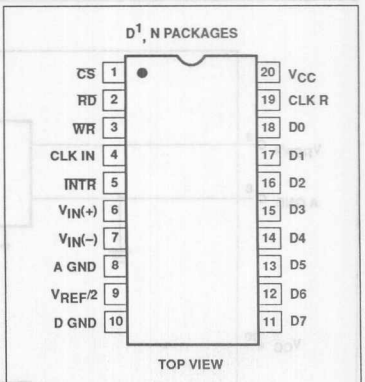
FEATURES

- Compatible with most microprocessors
- Differential inputs
- 3-State outputs
- Logic levels TTL and MOS compatible
- Can be used with internal or external clock
- Analog input range 0V to VCC
- Single 5V supply
- Guaranteed specification with 1MHz clock

APPLICATIONS

- Transducer-to-microprocessor interface
- Digital thermometer
- Digitally-controlled thermostat
- Microprocessor-based monitoring and control systems

PIN CONFIGURATION



NOTE:
SOL — Released in large SO package only.

ORDERING INFORMATION

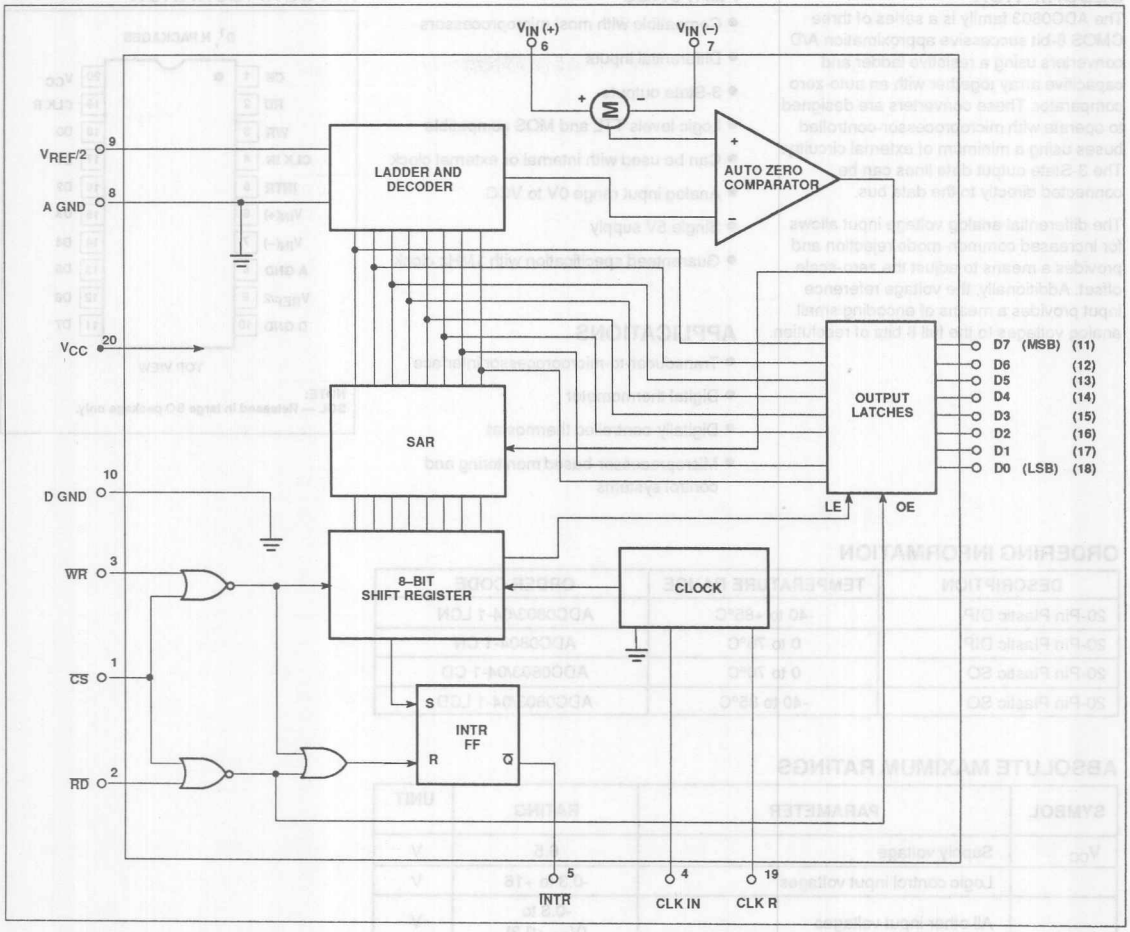
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	-40 to +85°C	ADC0803/04-1 LCN
20-Pin Plastic DIP	0 to 70°C	ADC0804-1 CN
20-Pin Plastic SO	0 to 70°C	ADC0803/04-1 CD
20-Pin Plastic SO	-40 to 85°C	ADC0803/04-1 LCD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	6.5	V
	Logic control input voltages	-0.3 to +16	V
	All other input voltages	-0.3 to (V_{CC} +0.3)	V
T_A	Operating temperature range		
	ADC0803/04-1 LCD	-40 to +85	°C
	ADC0803/04-1 LCN	-40 to +85	°C
	ADC0803/04-1 CD	0 to +70	°C
	ADC0804-1 CN	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C
P_D	Maximum power dissipation T_A=25°C (still air)[1]		
	N package	1690	mW
	D package	1390	mW

NOTES:
1. Derate above 25°C, at the following rates:
   N package at 13.5mW/°C
   D package at 11.1mW/°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V, f_{CLK} = 1MHz, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	ADC0803/4			UNIT
			Min	Typ	Max	
	ADC0803 relative accuracy error (adjusted)	Full-Scale adjusted			0.50	LSB
	ADC0804 relative accuracy error (unadjusted)	$V_{REF}/2 = 2.500V_{DC}$			1	LSB
R_{IN}	$V_{REF}/2$ input resistance	$V_{CC} = 0V$[2]	400	680		Ω
	Analog input voltage range		–0.05		V_{CC}+0.05	V
	DC common-mode error	Over analog input voltage range		1/16	1/8	LSB
	Power supply sensitivity	V_{CC} = 5V ±10%[1]		1/16		LSB
Control inputs						
V_{IH}	Logical "1" input voltage	$V_{CC} = 5.25V_{DC}$	2.0		15	V_{DC}
V_{IL}	Logical "0" input voltage	$V_{CC} = 4.75V_{DC}$			0.8	V_{DC}
I_{IH}	Logical "1" input current	$V_{IN} = 5V_{DC}$		0.005	1	μA_{DC}
I_{IL}	Logical "0" input current	$V_{IN} = 0V_{DC}$	–1	–0.005		μA_{DC}
Clock in and clock R						
V_{T+}	Clock in positive-going threshold voltage		2.7	3.1	3.5	V_{DC}
V_{T-}	Clock in negative-going threshold voltage		1.15	1.8	2.1	V_{DC}
V_H	Clock in hysteresis (V_{T+})–(V_{T-})		0.6	1.3	2.0	V_{DC}
V_{OL}	Logical "0" clock R output voltage	$I_{OL} = 360\mu A$, $V_{CC} = 4.75V_{DC}$			0.4	V_{DC}
V_{OH}	Logical "1" clock R output voltage	$I_{OH} = -360\mu A$, $V_{CC} = 4.75V_{DC}$	2.4			V_{DC}
Data output and $\overline{INTR}$						
V_{OL}	Logical "0" output voltage					
	Data outputs	I_{OL} = 1.6mA, $V_{CC} = 4.75V_{DC}$			0.4	V_{DC}
	$\overline{INTR}$ outputs	I_{OL} = 1.0mA, $V_{CC} = 4.75V_{DC}$			0.4	V_{DC}
V_{OH}	Logical "1" output voltage	$I_{OH} = -360\mu A$, $V_{CC} = 4.75V_{DC}$	2.4			V_{DC}
		$I_{OH} = -10\mu A$, $V_{CC} = 4.75V_{DC}$	4.5			V_{DC}
I_{OZL}	3-state output leakage	$V_{OUT} = 0V_{DC}$, $\overline{CS}$ = logical "1"	–3			μA_{DC}
I_{OZH}	3-state output leakage	$V_{OUT} = 5V_{DC}$, $\overline{CS}$ = logical "1"			3	μA_{DC}
I_{SC}	+Output short-circuit current	V_{OUT} = 0V, T_A = 25°C	4.5	12		mA_{DC}
I_{SC}	–Output short-circuit current	$V_{OUT} = V_{CC}$, T_A = 25°C	9.0	30		mA_{DC}
I_{CC}	Power supply current	f_{CLK} = 1MHz, $V_{REF}/2$ = OPEN, $\overline{CS}$ = Logical "1", T_A = 25°C		3.0	3.5	mA

NOTES:
1. Analog inputs must remain within the range: $-0.05 \le V_{IN} \le V_{CC} + 0.05V$.
2. See typical performance characteristics for input resistance at V_{CC} = 5V.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	ADC0803/4			UNIT
					Min	Typ	Max	
	Conversion time			f_{CLK}=1MHz[1]	66		73	µs
f_{CLK}	Clock frequency[1]				0.1	1.0	3.0	MHz
	Clock duty cycle[1]				40		60	%
CR	Free-running conversion rate			$\overline{CS}$=0, f_{CLK}=1MHz $\overline{INTR}$ tied to $\overline{WR}$			13690	conv/s
$t_{W(\overline{WR})L}$	Start pulse width			$\overline{CS}$=0	30			ns
t_{ACC}	Access time	Output	$\overline{RD}$	$\overline{CS}$=0, C_L=100pF		75	100	ns
t_{1H}, t_{0H}	3-State control	Output	$\overline{RD}$	CL=10pF, R_L=10kΩ See 3-State test circuit		70	100	ns
t_{W1}, t_{R1}	$\overline{INTR}$ delay	$\overline{INTR}$	$\overline{WD}$ or $\overline{RD}$			100	150	ns
C_{IN}	Logic input=capacitance					5	7.5	pF
C_{OUT}	3-State output capacitance					5	7.5	pF

NOTES:
1. Accuracy is guaranteed at f_{CLK}=1MHz. Accuracy may degrade at higher clock frequencies.

FUNCTIONAL DESCRIPTION

These devices operate on the Successive Approximation principle. Analog switches are closed sequentially by successive approximation logic until the input to the auto-zero comparator [$V_{IN(+)}$-$V_{IN(-)}$] matches the voltage from the decoder. After all bits are tested and determined, the 8-bit binary code corresponding to the input voltage is transferred to an output latch. Conversion begins with the arrival of a pulse at the $\overline{WR}$ input if the CS input is low. On the High-to-Low transition of the signal at the WR or the CS input, the SAR is initialized, the shift register is reset, and the $\overline{INTR}$ output is set high. The A/D will remain in the reset state as long as the $\overline{CS}$ and $\overline{WR}$ inputs remain low. Conversion will start from one to eight clock periods after one or both of these inputs makes a Low-to-High transition. After the conversion is complete, the $\overline{INTR}$ pin will make a High-to-Low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion result. A read ($\overline{RD}$) operation (with $\overline{CS}$ low) will clear the $\overline{INTR}$ line and enable the output latches. The device may be run in the free-running mode as described later. A conversion in progress can be interrupted by issuing another start command.

Digital Control Inputs

The digital control inputs (CS, WR, $\overline{RD}$) are compatible with standard TTL logic voltage levels. The required signals at these inputs correspond to Chip Select, START Conversion, and Output Enable control signals, respectively. They are active-Low for easy interface to microprocessor and microcontroller control buses. For applications not using microprocessors, the $\overline{CS}$ input (Pin 1) can be grounded and the A/D START function is achieved by a negative-going pulse to the $\overline{WR}$ input (Pin 3). The Output Enable function is achieved by a logic low signal at the $\overline{RD}$ input (Pin 2), which may be grounded to constantly have the latest conversion present at the output.

ANALOG OPERATION

Analog Input Current

The analog comparisons are performed by a capacitive charge summing circuit. The input capacitor is switched between $V_{IN(+)}$4 and $V_{IN(-)}$, while reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the most recent total value set by the successive approximation register.

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These transient currents occur at the leading edge of the internal clock pulses. They decay rapidly so do not inherently cause errors as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors and Source Resistance

Bypass capacitors at the input will average the charges mentioned above, causing a DC and an AC current to flow through the output resistance of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input at full scale. This current can be a few microamps, so bypass capacitors should NOT be used at the analog inputs of the V_{REF}/2 input for high resistance sources (> 1kΩ). If input bypass capacitors are desired for noise filtering and a high source resistance is desired to minimize capacitor size, detrimental effects of the voltage drop across the input resistance can be eliminated by adjusting the full scale with both the input resistance and the input bypass capacitor in place. This is possible because the magnitude of the input current is a precise linear function of the differential voltage.

Large values of source resistance where an input bypass capacitor is not used will not cause errors as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (< 1kΩ) for a passive RC section or add an op amp active filter (low pass). For applications with source resistances at or below 1kΩ, a 0.1µF bypass capacitor at the inputs will prevent pickup due to series lead inductance or a long wire. A 100Ω series resistor can be used to isolate this capacitor (both the resistor and capacitor should be placed out of the feedback loop) from the output of the op amp, if used.

Analog Differential Voltage Inputs and Common-Mode Rejection

These A/D converters have additional flexibility due to the analog differential voltage input. The $V_{IN(-)}$ input (Pin 7) can be used to

subtract a fixed voltage from the input reading (tare correction). This is also useful in a 4/20mA current loop conversion. Common-mode noise can also be reduced by the use of the differential input.

The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is 4.5 clock periods. The maximum error due to this time difference is given by:

$$V(max)=(V_P)\ (2f_{CM})\ (4.5/f_{CLK}),$$

where:

V=error voltage due to sampling delay

V_P=peak value of common-mode voltage

f_{CM}=common mode frequency

For example, with a 60Hz common-mode frequency, f_{cm}, and a 1MHz A/D clock, F_{CLK}, keeping this error to 1/4 LSB (about 5mV) would allow a common-mode voltage, V_P, which is given by:

$$V_P = \frac{[V(max)\ (f_{CLK})}{(2f_{CM})(4.5)}$$

or

$$V_P = \frac{(5\ x\ 10^{-3})\ (10^4)}{(6.28)\ (60)\ (4.5)} = 2.95\,V$$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode voltage levels than this, however.

An analog input span less than the full 5V capability of the device, together with a relatively large zero offset, can be easily handled by use of the differential input. (See Reference Voltage Span Adjust).

Noise and Stray Pickup

The leads of the analog inputs (Pins 6 and 7) should be kept as short as possible to minimize input noise coupling and stray signal pick-up. Both EMI and undesired digital signal coupling to these inputs can cause system errors. The source resistance for these inputs should generally be below 5kΩ to help avoid undesired noise pickup. Input bypass capacitors at the analog inputs can create errors as described previously. Full scale adjustment with any input bypass capacitors in place will eliminate these errors.

Reference Voltage

For application flexibility, these A/D converters have been designed to accommodate fixed reference voltages of 5V to Pin 20 or 2.5V to Pin 9, or an adjusted reference voltage at Pin 9. The reference can be set by forcing it at $V_{REF}/2$ input, or can be determined by the supply voltage (Pin 20). Figure 1 indicates how this is accomplished.

Figure 2. Offsetting the Zero Scale and Adjusting the Input Range (Span)

Reference Voltage Span Adjust

Note that the Pin 9 ($V_{REF}/2$) voltage is either 1/2 the voltage applied to the V_{CC} supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. In addition to allowing for flexible references and full span voltages, this also allows for a ratiometric voltage reference. The internal gain of the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at Pin 9.

For example, a dynamic voltage range of the analog input voltage that extends from 0 to 4V gives a span of 4V (4-0), so the $V_{REF}/2$ voltage can be made equal to 2V (half of the 4V span) and full scale output would correspond to 4V at the input.

On the other hand, if the dynamic input voltage had a range of 0.5 to 3.5V, the span or dynamic input range is 3V (3.5-0.5). To encode this 3V span with 0.5V yielding a code of zero, the minimum expected input (0.5V, in this case) is applied to the $V_{IN}(-)$ pin to account for the offset, and the $V_{REF}/2$ pin is set to 1/2 the 3V span, or 1.5V. The A/D converter will now encode the $V_{IN}(+)$ signal between 0.5 and 3.5V with 0.5V at the input corresponding to a code of zero and 3.5V at the input producing a full scale output code. The full 8 bits of resolution are thus applied over this reduced input voltage range. The required connections are shown in Figure 2.

Operating Mode

These converters can be operated in two modes:

1) absolute mode
2) ratiometric mode

In absolute mode applications, both the initial accuracy and the temperature stability of the reference voltage are important factors in the accuracy of the conversion. For $V_{REF}/2$ voltages of 2.5V, initial errors of ±10mV will cause conversion errors of ±1 LSB due to the gain of 2 at the $V_{REF}/2$ input. In reduced span applications, the initial value and stability of the $V_{REF}/2$ input voltage become even more important as the same error is a larger percentage of the $V_{REF}/2$ nominal value. See Figure 3.

In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter, and, therefore, cancels out in the final digital code. See Figure 4.

Generally, the reference voltage will require an initial adjustment. Errors due to an improper reference voltage value appear as full-scale errors in the A/D transfer function.

ERRORS AND INPUT SPAN ADJUSTMENTS

There are many sources of error in any data converter, some of which can be adjusted out. Inherent errors, such as relative accuracy, cannot be eliminated, but such errors as full-scale and zero scale offset errors can be eliminated quite easily. See Figure 2.

Zero Scale Error

Zero scale error of an A/D is the difference of potential between the ideal 1/2 LSB value (9.8mV for $V_{REF}/2$=2.500V) and that input voltage which just causes an output transition from code 0000 0000 to a code of 0000 0001.

If the minimum input value is not ground potential, a zero offset can be made. The converter can be made to output a digital code of 0000 0000 for the minimum expected input voltage by biasing the $V_{IN}(-)$ input to that minimum value expected at the $V_{IN}(-)$ input to that minimum value expected at the $V_{IN}(+)$ input. This uses the differential mode of the converter. Any offset adjustment should be done prior to full scale adjustment.

Full Scale Adjustment

Full scale gain is adjusted by applying any desired offset voltage to $V_{IN}(-)$, then applying the $V_{IN}(+)$ a voltage that is 1-1/2 LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of $V_{REF}/2$ input voltage (or the V_{CC} supply if there is no $V_{REF}/2$ input connection) for a digital output code which just changes from 1111 1110 to 1111 1111. The ideal $V_{IN}(+)$ voltage for this full-scale adjustment is given by:

$$V_{IN}(+) = V_{IN}(-) - 1.5\ x\ \frac{V_{MAX} - V_{MIN}}{255}$$

where:

V_{MAX}=high end of analog input range (ground referenced)

V_{MIN}=low (zero offset) of analog input (ground referenced)

CLOCKING OPTION

The clock signal for these A/Ds can be derived from external sources, such as a system clock, or self-clocking can be

accomplished by adding an external resistor and capacitor, as shown in Figure 5.

Heavy capacitive or DC loading of the CLK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF are allowed. This permits driving up to seven A/D converter CLK IN pins of this family from a single CLK R pin of one converter. For larger loading of the clock line, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the CLK R pin.

Restart During a Conversion

A conversion in process can be halted and a new conversion began by bringing the $\overline{CS}$ and $\overline{WR}$ inputs low and allowing at least one of them to go high again. The output data latch is not updated if the conversion in progress is not completed; the data from the previously completed conversion will remain in the output data latches until a subsequent conversion is completed.

Continuous Conversion

To provide continuous conversion of input data, the $\overline{CS}$ and $\overline{RD}$ inputs are grounded and $\overline{INTR}$ output is tied to the $\overline{WR}$ input. This $\overline{INTR}$/$\overline{WR}$ connection should be momentarily forced to a logic low upon power-up to insure circuit operation. See Figure 6 for one way to accomplish this.

DRIVING THE DATA BUS

This CMOS A/D converter, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry tied to the data bus will add to the total capacitive loading, even in the high impedance mode.

There are alternatives in handling this problem. The capacitive loading of the data bus slows down the response time, although DC specifications are still met. For systems with a relatively low CPU clock frequency, more time is available in which to establish proper logic levels on the bus, allowing higher capacitive loads to be driven (see Typical Performance Characteristics).

At higher CPU clock frequencies, time can be extended for I/O reads (and/or writes) by inserting wait states (8880) or using clock-extending circuits (6800, 8035).

Finally, if time is critical and capacitive loading is high, external bus drivers must be used. These can be 3-State buffers (low power Schottky is recommended, such as the N74LS240 series) or special higher current drive products designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended as the PNP input offers low loading of the A/D output, allowing better response time.

POWER SUPPLIES

Noise spikes on the V_{CC} line can cause conversion errors as the internal comparator will respond to them. A low inductance filter capacitor should be used close to the converter V_{CC} pin and values of 1µF or greater are recommended. A separate 5V regulator for the converter (and other 5V linear circuitry) will greatly reduce digital noise on the V_{CC} supply and the attendant problems.

WIRING AND LAYOUT PRECAUTIONS

Digital wire-wrap sockets and connections are not satisfactory for breadboarding this (or any) A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped or kept as far as possible from the analog signal leads. Single wire analog input leads may pick up undesired hum and noise, requiring the use of shielded leads to the analog inputs in many applications.

A single-point analog ground separate from the logic or digital ground points should be used. The power supply bypass capacitor and the self-clocking capacitor, if used, should be returned to digital ground. Any $V_{REF}/2$ bypass capacitor, analog input filter capacitors, and any input shielding should be returned to the analog ground point. Proper grounding will minimize zero-scale errors which are present in every code. Zero-scale errors can usually be traced to improper board layout and wiring.

APPLICATIONS

Microprocessor Interfacing

This family of A/D converters was designed for easy microprocessor interfacing. These converters can be memory mapped with appropriate memory address decoding for $\overline{CS}$ (read) input. The active-Low write pulse from the processor is then connected to the $\overline{WR}$ input of the A/D converter, while the processor active-Low read pulse is fed to the converter $\overline{RD}$ input to read the converted data. If the clock signal is derived from the microprocessor system clock, the designer/programmer should be sure that there is no attempt to read the converter until 74 converter clock pulses after the start pulse goes high. Alternatively, the $\overline{INTR}$ pin may be used to interrupt the processor to cause reading of the converted data. Of course, the converter can be connected and addressed as a peripheral (in I/O space), as shown in Figure 7. A bus driver should be used as a buffer to the A/D output in large microprocessor systems where the data leaves the PC board and/or must drive capacitive loads in excess of 100pF. See Figure 9.

Interfacing the SCN8048 microcomputer family is pretty simple, as shown in Figure 8. Since the SCN8048 family has 24 I/O lines, one of these (shown here as bit 0 or port 1) can be used as the chip select signal to the converter, eliminating the need for an address decoder. The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing to a dummy address.

Digitizing a Transducer Interface Output

Circuit Description

Figure 10 shows an example of digitizing transducer interface output voltage. In this case, the transducer interface is the NE5521, an LVDT (Linear Variable Differential Transformer) Signal Conditioner. The diode at the A/D input is used to insure that the input to the A/D does not go excessively beyond the supply voltage of the A/D. See the NE5521 data sheet for a complete description of the operation of that part.

Circuit Adjustment

To adjust the full scale and zero scale of the A/D, determine the range of voltages that the transducer interface output will take on. Set the LVDT core for null and set the Zero Scale Scale Adjust Potentiometer for a digital output from the A/D of 1000 000. Set the LVDT core for maximum voltage from the interface and set the Full Scale Adjust potentiometer so the A/D output is just barely 1111 1111.

A Digital Thermostat

Circuit Description

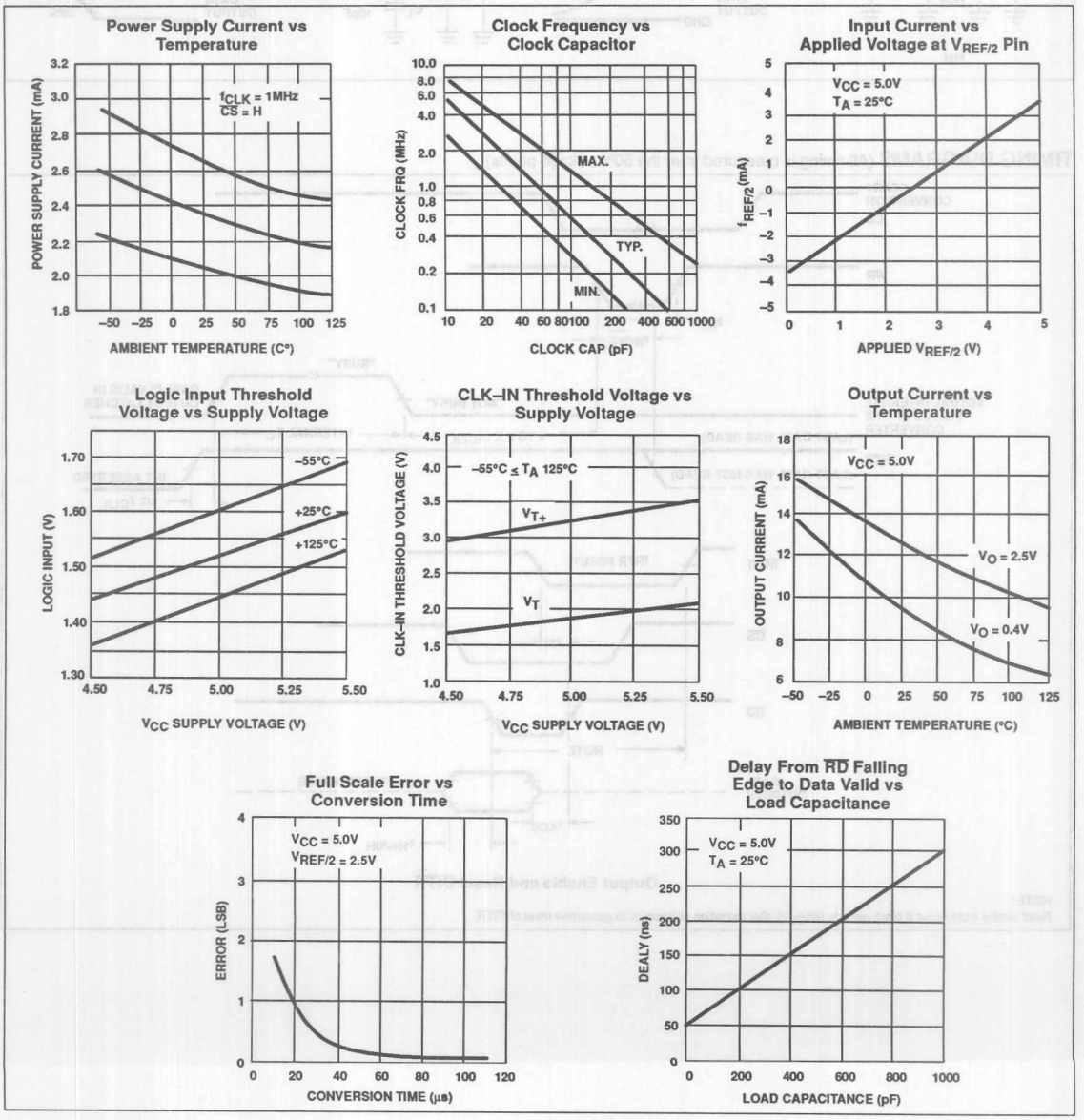
The schematic of a Digital Thermostat is shown in Figure 11. The A/D digitizes the output of the LM35, a temperature transducer IC with an output of 10mV per °C. With $V_{REF}/2$ set for 2.56V, this 10mV corresponds to 1/2 LSB and the circuit resolution is 2°C. Reducing $V_{REF}/2$ to 1.28 yields a resolution of 1°C. Of course, the lower $V_{REF}/2$ is, the more sensitive the A/D will be to noise.

The desired temperature is set by holding either of the set buttons closed. The SCC80C451 programming could cause the desired (set) temperature to be displayed while either button is depressed and for a short time after it is released. At other times the ambient temperature could be displayed.

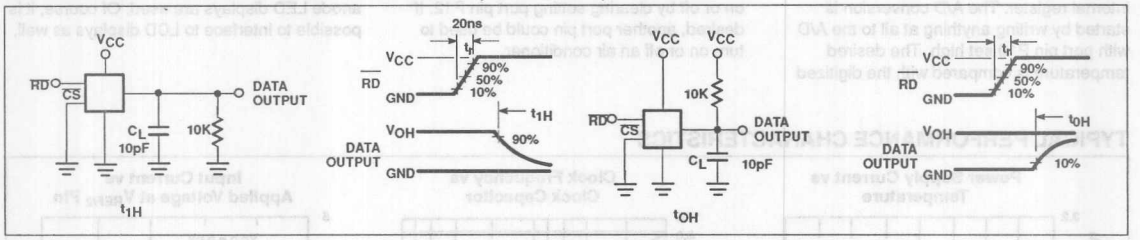
The set temperature is stored in an SCN8051 internal register. The A/D conversion is started by writing anything at all to the A/D with port pin P10 set high. The desired temperature is compared with the digitized actual temperature, and the heater is turned on or off by clearing setting port pin P12. If desired, another port pin could be used to turn on or off an air conditioner.

The display drivers are NE587s if common anode LED displays are used. Of course, it is possible to interface to LCD displays as well.

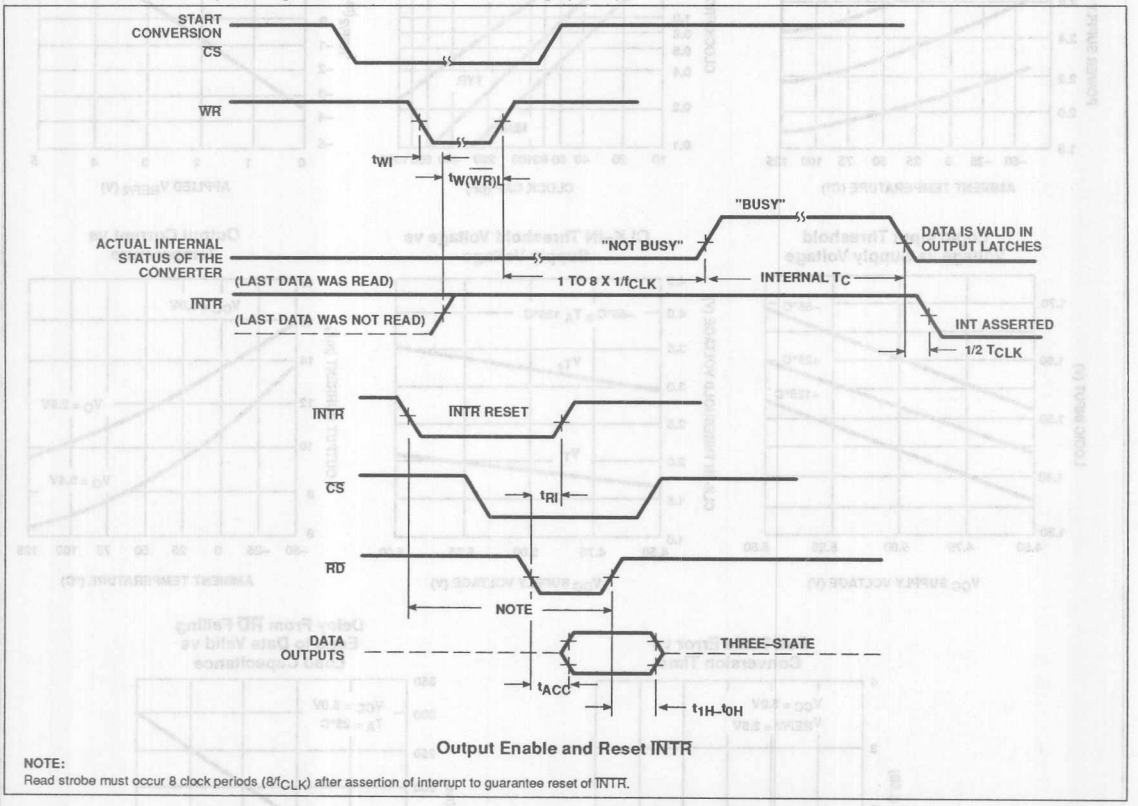
TYPICAL PERFORMANCE CHARACTERISTICS



3-STATE TEST CIRCUITS AND WAVEFORMS (ADC0801-1)

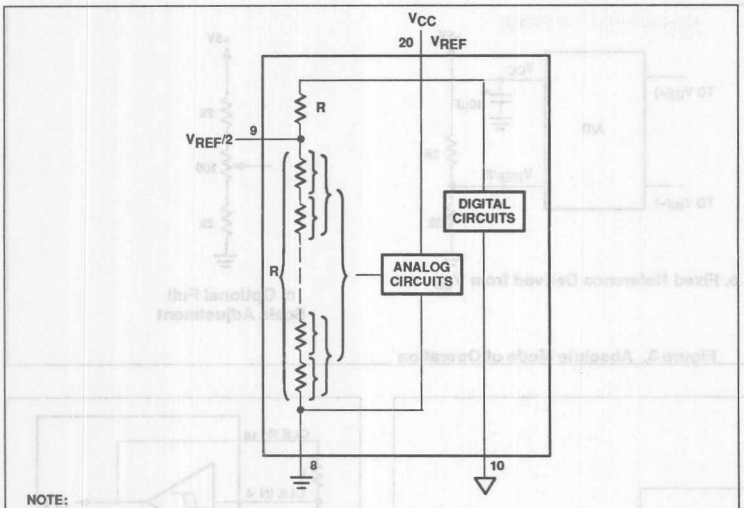


TIMING DIAGRAMS (All timing is measured from the 50% voltage points)



Output Enable and Reset INTR

NOTE:
Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of INTR.



NOTE:
The $V_{REF}/2$ voltage is either 1/2 the V_{CC} voltage or is that which is forced at Pin 9.

Figure 1. Internal Reference Design

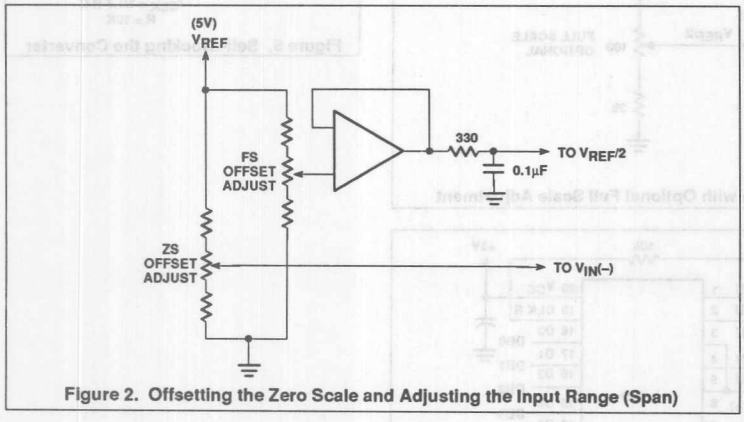


Figure 2. Offsetting the Zero Scale and Adjusting the Input Range (Span)

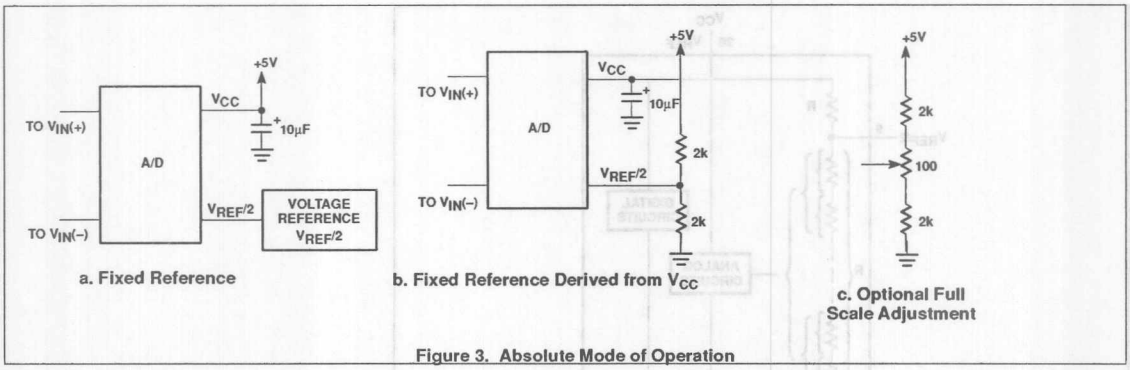


Figure 3. Absolute Mode of Operation

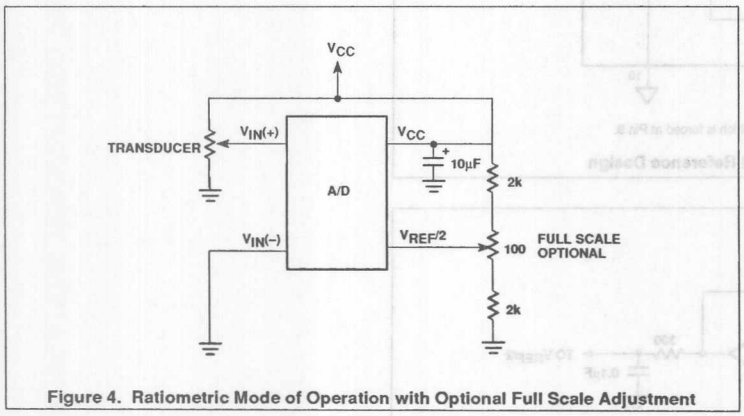


Figure 4. Ratiometric Mode of Operation with Optional Full Scale Adjustment

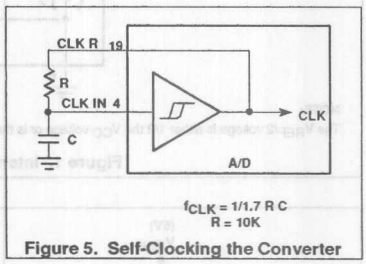


Figure 5. Self-Clocking the Converter

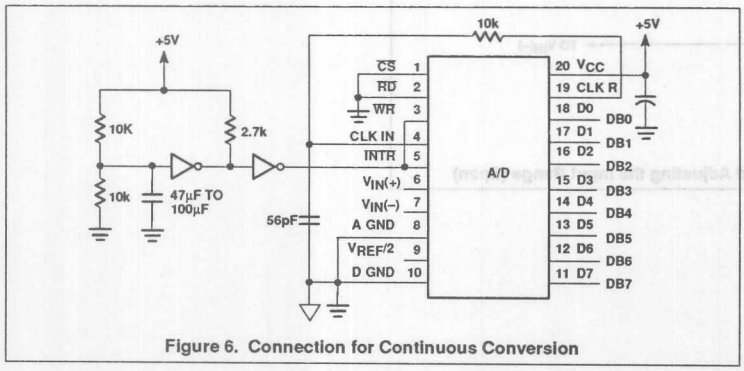


Figure 6. Connection for Continuous Conversion

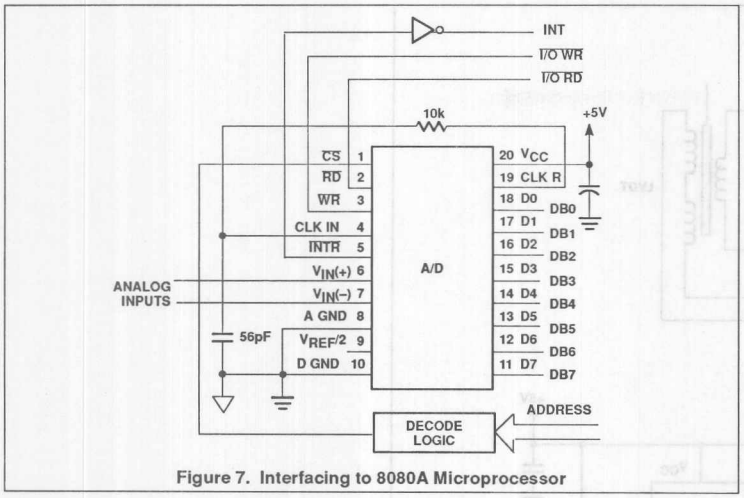


Figure 7. Interfacing to 8080A Microprocessor

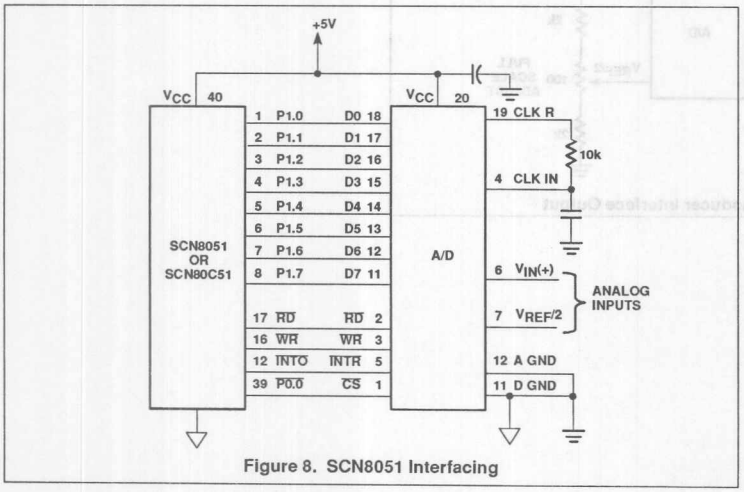


Figure 8. SCN8051 Interfacing

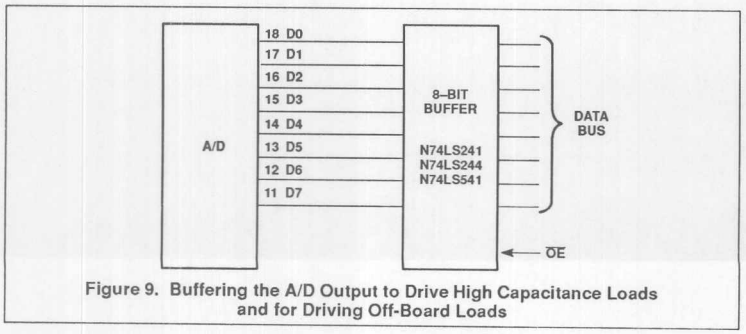


Figure 9. Buffering the A/D Output to Drive High Capacitance Loads and for Driving Off-Board Loads

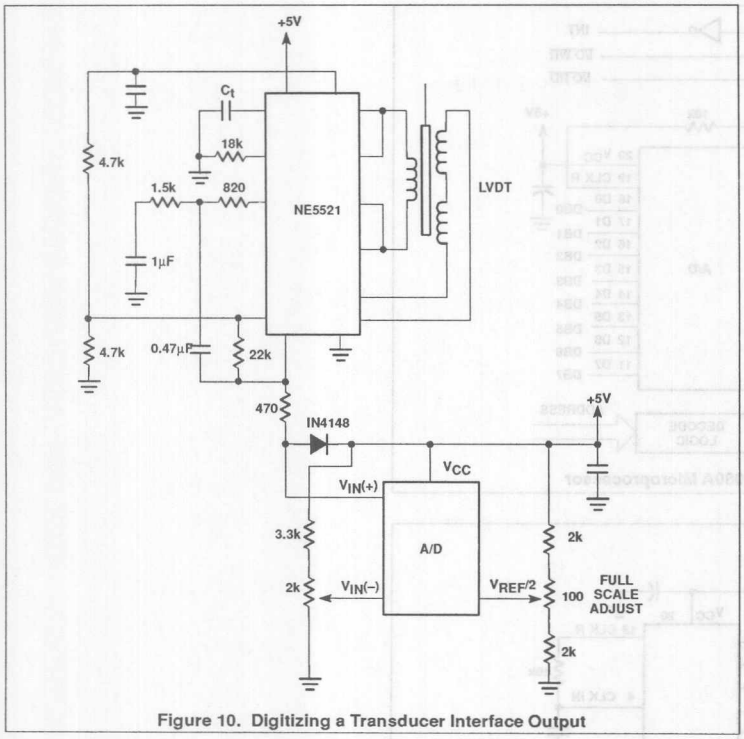


Figure 10. Digitizing a Transducer Interface Output

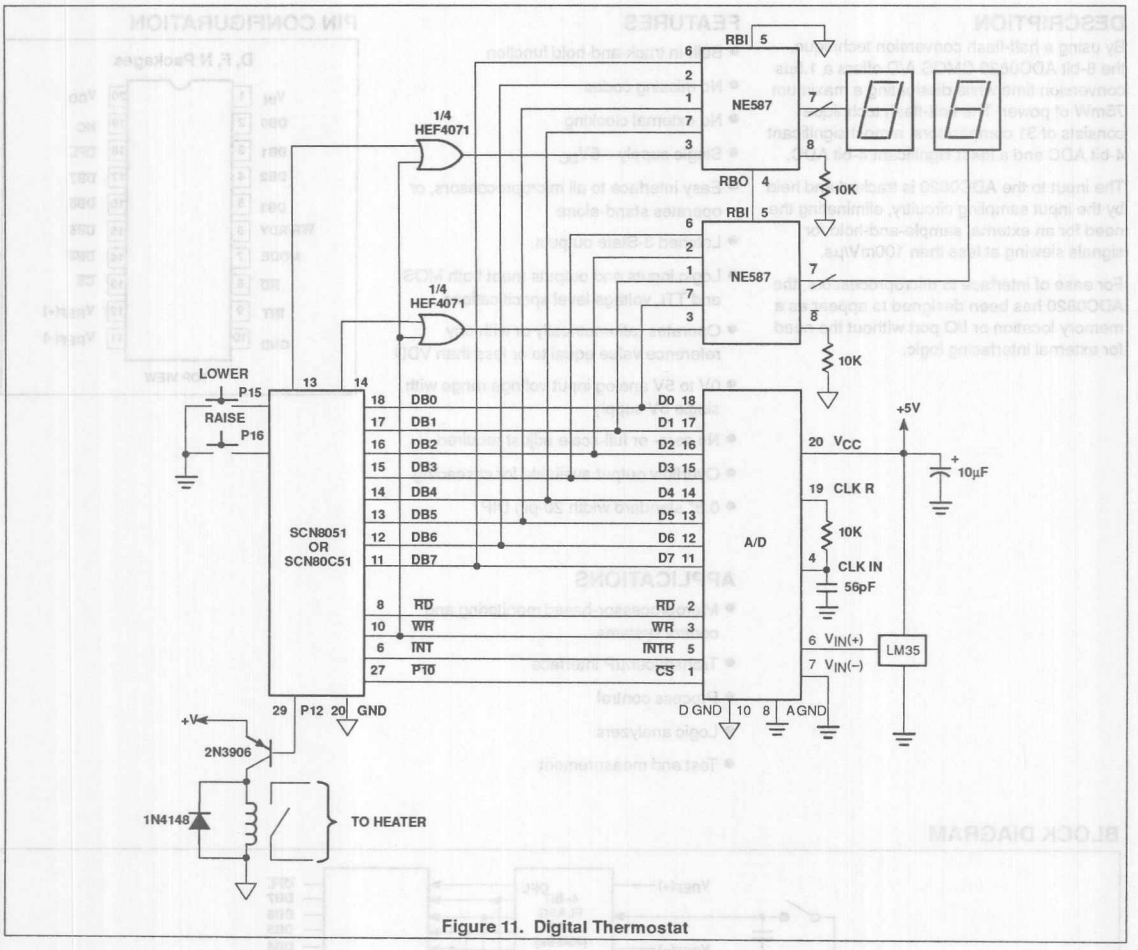


Figure 11. Digital Thermostat

8-Bit, high-speed, μP-compatible A/D converter with track/hold function

ADC0820

DESCRIPTION

By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5μs conversion time while dissipating a maximum 75mW of power. The half-flash technique consists of 31 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820 is tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold for signals slewing at less than 100mV/μs.

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

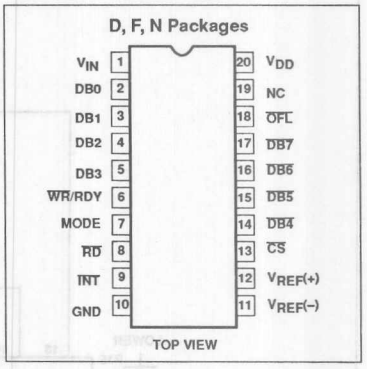
FEATURES

- Built-in track-and-hold function
- No missing codes
- No external clocking
- Single supply—5V_{DC}
- Easy interface to all microprocessors, or operates stand-alone
- Latched 3-State outputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than VDD
- 0V to 5V analog input voltage range with single 5V supply
- No zero- or full-scale adjust required
- Overflow output available for cascading
- 0.3″ standard width 20-pin DIP

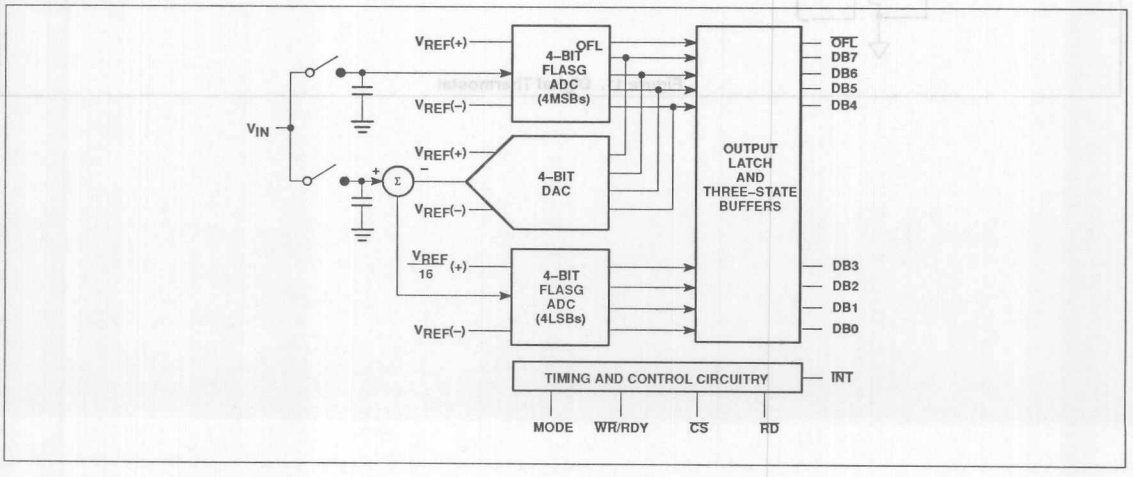
APPLICATIONS

- Microprocessor-based monitoring and control systems
- Transducer/μP interface
- Process control
- Logic analyzers
- Test and measurement

PIN CONFIGURATION



BLOCK DIAGRAM



8-Bit, high-speed, μP-compatible A/D converter with track/hold function

ADC0820

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	ADC0820BNEN
20-Pin Plastic SO package	0 to +70°C	ADC0820BNED
20-Pin Plastic DIP	0 to +70°C	ADC0820CNEN
20-Pin Plastic SO package	0 to +70°C	ADC0820CNED
20-Pin Plastic DIP	-40 to +85°C	ADC0820BSAN
20-Pin Plastic SO package	-40 to +85°C	ADC0820BSAD
20-Pin Plastic DIP	-40 to +85°C	ADC0820CSAN
20-Pin Plastic SO package	-40 to +85°C	ADC0820CSAD
20-Pin Ceramic DIP	-55 to +125°C	ADC0820BSEF
20-Pin Ceramic DIP	-55 to +125°C	ADC0820CSEF

PIN DESCRIPTION

PIN NO	SYMBOL	DESCRIPTION
1	V_{IN}	Analog input; range=GND≤V_{IN}≤V_{DD}
2	DB0	3-state data output—Bit 0 (LSB)
3	DB1	3-state data output—Bit 1
4	DB2	3-state data output—Bit 2
5	DB3	3-state data output—Bit 3
6	$\overline{WR}$/RDY	**WR-RD Mode** $\overline{WR}$: With $\overline{CS}$ Low, the conversion is started on the falling edge of $\overline{WR}$. Approximately 800ns (the preset internal time out, t_I) after the $\overline{WR}$ rising edge, the result of the conversion will be strobed into the output latch, provided that $\overline{RD}$ does not occur prior to this time out (see Figures 3a and 3b). **RD Mode** RDY: This is an open-drain output (no internal pull-up device). RDY will go Low after the falling edge of $\overline{CS}$; RDY will go 3-State when the result of the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system (see Figure 1).
7	Mode	Mode: Mode selection input—it is internally tied to GND through a 30μA current source. RD Mode: When mode is Low. WR-RD Mode: When mode is High.
8	$\overline{RD}$	**WR-RD Mode** With $\overline{CS}$ Low, the 3-State data outputs (DB0-DB7) will be activated when $\overline{RD}$ goes Low. $\overline{RD}$ can also be used to increase the speed of the converter by reading data prior to the preset internal time out (T_I ~ 800ns). If this is done, the data result transferred to output latch is latched after the falling edge of the $\overline{RD}$ (see Figures 3a and 3b). **RD Mode** With $\overline{CS}$ Low, the conversion will start with $\overline{RD}$ going Low; also, $\overline{RD}$ will enable the 3-State data outputs at the completion of the conversion. RDY going 3-State and $\overline{INT}$ going Low indicate the completion of the conversion (see Figure 1).
9	$\overline{INT}$	**WR-RD Mode** $\overline{INT}$ going Low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ will go Low ~ 800ns (the preset internal time out, t_I) after the rising edge of $\overline{WR}$ (see Figure 3a); or $\overline{INT}$ will go Low after the falling edge of $\overline{RD}$, if $\overline{RD}$ goes Low prior to the 800ns time out (see Figure 3b). $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see Figures 3a and 3b). **RD Mode** $\overline{INT}$ going Low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see Figure 1).
10	GND	Ground

PIN DESCRIPTION (Continued)

11	$V_{REF}(-)$	The bottom of resistor ladder, voltage range: $GND \leq V_{REF}(-) \leq V_{REF}(+)$
12	$V_{REF}(+)$	The top of resistor ladder, voltage range: $V_{REF}(-) \leq V_{REF}(+) \leq V_{DD}$.
13	$\overline{CS}$	$\overline{CS}$ must be Low in order for the $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.
14	DB4	3-State data output—Bit 4
15	DB5	3-State data output—Bit 5
16	DB6	3-State data output—Bit 6
17	DB7	3-State data output—Bit 7 (MSB)
18	$\overline{OFL}$	Overflow output—if the analog input is higher than the $V_{REF}(+)$- LSB, $\overline{OFL}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to have more resolution (9, 10-bit).
19	NC	No connection
20	V_{DD}	Power supply voltage

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage	7	V
	Logic control inputs	-0.2 to V_{DD}+0.2	V
	Voltage at other inputs and output	-0.2 to V_{DD}+0.2	V
T_{STG}	Storage temperature range	-65 to +150	°C
P_D	Maximum power dissipation[3] T_A=25°C(still-air)		
	F package	1560	mW
	N package	1690	mW
	D package	1390	mW
T_{SOLD}	Lead temperature (soldering, 10sec)	300	°C
T_A	Operating ambient temperature range	$T_{MIN} \leq T_A \leq T_{MAX}$	
	ADC0820BSEF/CSEF	–55 to +125	°C
	ADC0820BSAN/CSAN/BSAD/CSAD	–40 to +85	°C
	ADC0820BNEN/CNEN/BNED/CNED	0 to +70	°C

NOTES:
1. Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.
2. All voltages are measured with respect to GND, unless otherwise specified.
3. Derate above 25°C at the following rates:
   F package at 12.5mW/°C
   N package at 13.5mW/°C
   D package at 11.1mW/°C

DC ELECTRICAL CHARACTERISTICS

RD mode (Pin 7=0), V_{DD}=5V, $V_{REF}(+)$=5V, and $V_{REF}(-)$=GND, unless otherwise specified. Limits apply from T_{MIN} to T_{MAX}.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Min	Typ[3]	Max	
	Resolution			8	8	8	bits
	Unadjusted error[1]	ADC0820B				±1/2	LSB
		ADC0820C				±1	LSB
R_{REF}	Reference resistance			1	1.6	4	kΩ
$V_{REF}(+)$	Input voltage			$V_{REF}(-)$		V_{DD}	V
$V_{REF}(-)$	Input voltage			GND		$V_{REF}(+)$	V
V_{IN}	Input voltage			GND-0.1		V_{DD}+0.1	V
	Maximum analog input leakage current	$\overline{CS}=V_{DD}$ $V_{IN}=V_{DD}$ V_{IN}=GND		-3		3	μA
	Power supply sensitivity	V_{DD}=5V±5%			±1/16	±1/4	LSB
$V_{IN(1)}$	Logical "1" input voltage	V_{DD}=5.25V	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	2.0		V_{DD}	V
			Mode	3.5		V_{DD}	V
$V_{IN(0)}$	Logical "0" input voltage	V_{DD}=4.75V	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	GND		0.8	V
			Mode	GND		1.5	V
$I_{IN(1)}$	Logical "1" input current	$V_{IN(1)}$=5V; $\overline{CS}$, $\overline{RD}$				1	μA
		$V_{IN(1)}$=5V; $\overline{WR}$				3	μA
		$V_{IN(1)}$=5V; Mode			30	200	μA
$I_{IN(0)}$	Logical "0" input current	$V_{IN(0)}$=0V; $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, Mode		-1			μA
$V_{OUT(1)}$	Logical "1" output voltage	V_{DD}=4.75V, I_{OUT}=-360μA; DB0-DB7, $\overline{OFL}$, $\overline{INT}$		2.4	4.6		V
		V_{DD}=4.75V, I_{OUT}=-10μA DB0-DB7, $\overline{OFL}$, $\overline{INT}$		4.5	4.74		V
$V_{OUT(0)}$	Logical "0" output voltage	V_{DD}=4.75V, I_{OUT}=1.6mA; DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY			0.2	0.4	V
I_{OZ}	3-state output current	V_{OUT}=5V; DB0-DB7, RDY				3	μA
		V_{OUT}=0V; DB0-DB7, RDY		-3			μA
I_{SOURCE}	Output source current	V_{OUT}=0V, DB0-DB7, $\overline{OFL}$		6	12		mA
		$\overline{INT}$		4.5	8		mA
I_{SINK}	Output sink current	V_{OUT}=5V; DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY		7	20		mA
I_{DD}	Supply current	$\overline{CS}$=$\overline{WR}$=$\overline{RD}$=0			6	15	mA
V_{DD}	Range			4.5		5.5	V

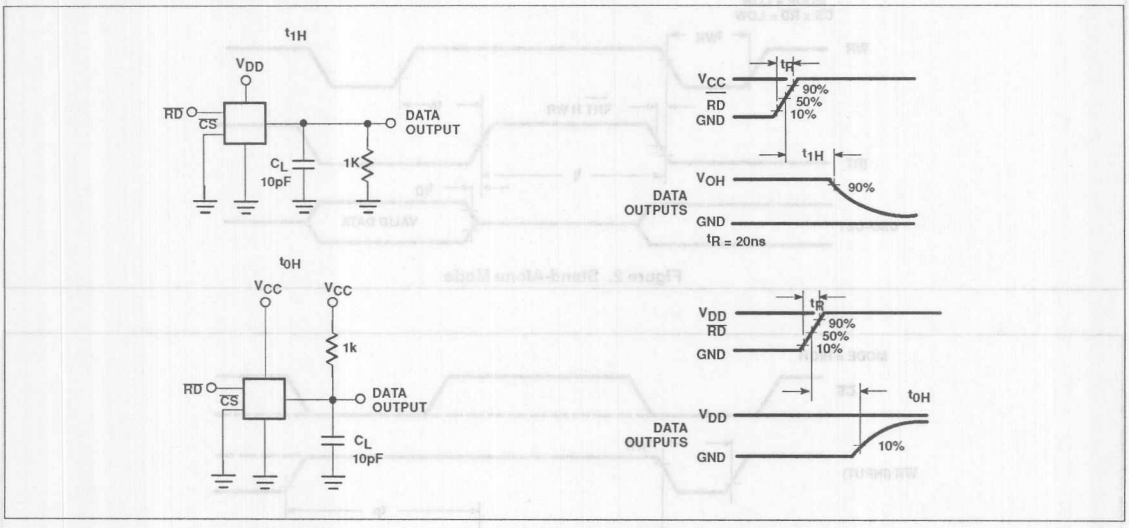
AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, $t_R = t_F$ = 20ns, $V_{REF(+)}$ = 5V, $V_{REF(-)}$ = 0V, and T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS[4]			UNIT
				Min	Typ[3]	Max	
t_{CRD}	Conversion time for RD mode		Mode=0, Figure 1		1.6	2.5	µs
t_{ACCO}	Access time (delay from falling edge of $\overline{RD}$ to output valid)		Mode=0, Figure 1		t_{CRD}+20	t_{CRD}+50	ns
t_{CWR-RD}	Conversion time for WR-RD mode		Mode=V_{DD}, t_{WR}=600ns, t_{RD}=600ns; Figures 3a and 3b			1.52	µs
t_{WR}	Write time	Min	Mode=V_{DD}, Figures 3a and 3b[2]	600			ns
		Max				50	µs
t_{RD}	Read time	Min	Mode=V_{DD}, Figures 3a and 3b[2]	600			ns
t_{ACC1}	Access time (delay from falling edge of $\overline{RD}$ t o output valid)		Mode=V_{DD}, t_{RD}<t_l; Figure 3b, C_L=15pF		190	280	ns
			C_L=100pF		210	320	ns
t_{ACC2}	Access time (delay from falling edge of $\overline{RD}$ t o output valid)		Mode=V_{DD}, t_{RD}>t_l; Figure 3a, C_L=15pF		70	120	ns
			C_L=100pF		90	150	ns
t_l	Internal comparison time		Mode=V_{DD}; Figures 2 and 3a, C_L=50pF		800	1300	ns
t_{1H}, t_{0H}	Three-state control (delay from rising edge of $\overline{RD}$ to Hi-Z state)		R_L=1kΩ, C_L=10pF		100	200	ns
$t_{\overline{INTL}}$	Delay from rising edge of $\overline{WR}$ to falling edge of $\overline{INT}$		Mode=V_{DD}, C_L=50pF t_{RD}>t_l; Figure 3a t_{RD}<t_l; Figure 3b		 t_l t_{RD}+200	 t_l t_{RD}+290	 ns ns
$t_{\overline{INTH}}$	Delay from rising edge of $\overline{RD}$ to rising edge of $\overline{INT}$		Figures 1, 3a, and 3b, C_L=50pF		125	225	ns
$t_{\overline{INTHWR}}$	Delay from rising edge of $\overline{WR}$ to rising edge of $\overline{INT}$		Figure 2, C_L=50pF		175	270	ns
t_{RDY}	Delay from $\overline{CS}$ to RDY		Figure 1, C_L=50pF, Mode=0		50	100	ns
t_{ID}	Delay from $\overline{INT}$ to output valid		Figure 2		20	50	ns
t_{RI}	Delay from $\overline{RD}$ to $\overline{INT}$		Mode=V_{DD}, t_{RD}<t_l; Figure 3b		200	290	ns
t_P	Delay from end of conversion to next conversion		Figures 1, 2, 3a, and 3b[2]	500			ns
SR	Slew rate, tracking				0.1		V/µs
C_{VIN}	Analog input capacitance				45		pF
C_{OUT}	Logic output capacitance				5		pF
C_{IN}	Logic input capacitance				5		pF

NOTES:
1. Unadjusted error includes offset, full-scale, and linearity errors.
2. Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified.
3. Typicals are at 25°C and represent most likely parametric norm.
4. Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

3-STATE TEST CIRCUITS AND WAVEFORMS



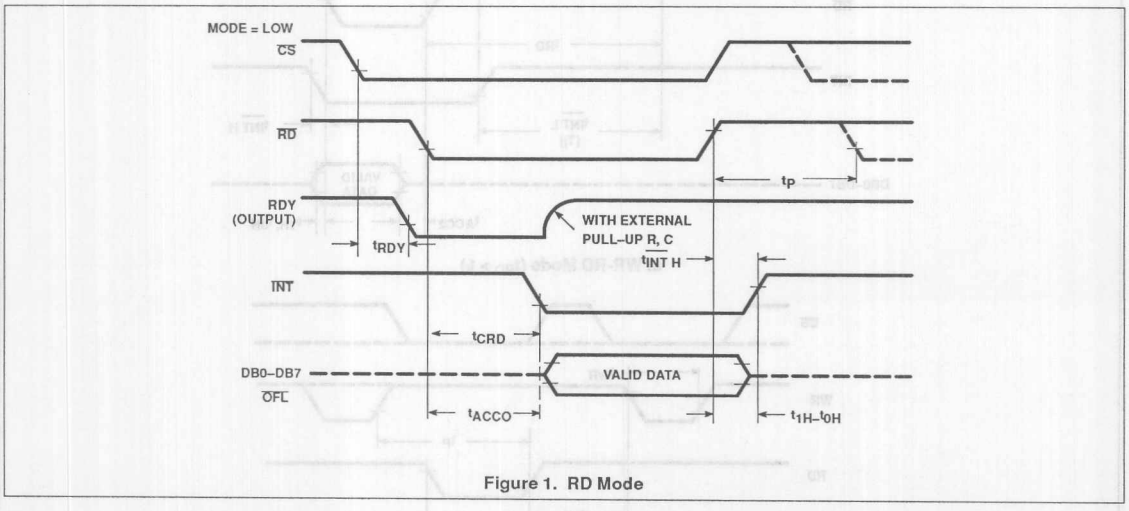


Figure 1. RD Mode

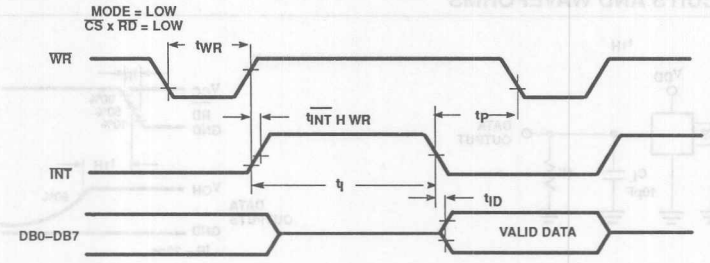
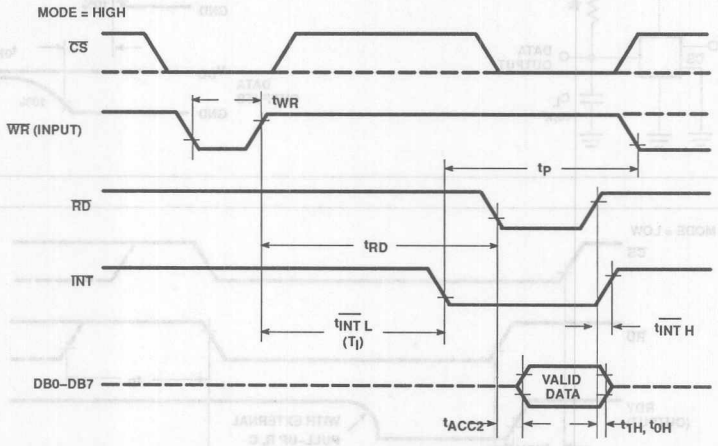
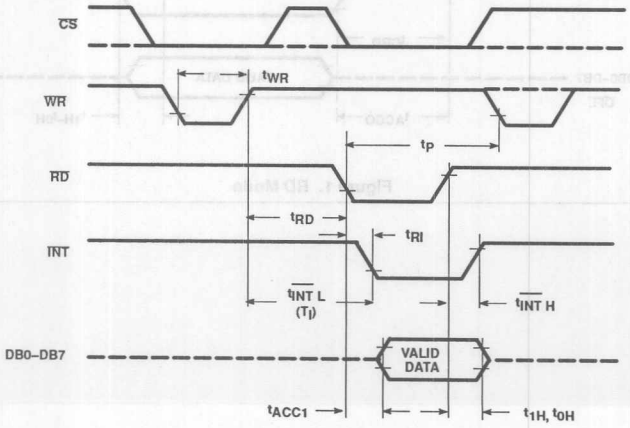


Figure 2. Stand-Alone Mode



a. WR-RD Mode ($t_{RD} > t_I$)



b. WR-RD Mode ($t_{RD} < t_I$)

Figure 3. WR–RD Mode

8-Bit, high-speed, μP-compatible A/D converter with track/hold function

ADC0820

FUNCTIONAL DESCRIPTION

General Operation

The ADC0820 uses two 4-bit flash A/D converters to make an 8-bit measurement (Block Diagram). Each flash ADC is made up of 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. To take a full 8-bit reading, one flash conversion is done to provide the 4 most significant data bits (via the MS flash ADC). Driven by the 4 MSBs, an internal DAC recreates an analog approximation of the input voltage. This analog signal is then subtracted from the input, and the difference voltage is converted by a second 4-bit flash ADC (the LS ADC), providing the 4 least significant bits of the output data word.

The internal DAC is actually a subsection of the MS flash converter. This is accomplished by using the same resistor ladder for the A/D as well as for generating the DAC signal. The DAC output is actually the tap on the resistor ladder which most closely approximates the analog input. In addition, the "sampled data" comparators used in the ADC0820 provide the ability to compare the magnitudes of several analog signals simultaneously, without using input summing amplifiers. This is especially useful in the LS flash ADC, where the signal to be converted is an analog difference.

The Sampled-Data Comparator

Each comparator in the ADC0820 consists of a CMOS inverter with a capacitively-coupled input (Figure 4). Analog switches connect the two comparator inputs to the input capacitor (C) and also connect the inverter's input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator, and another for making the comparison.

In the first cycle, one input switch and the inverter's feedback switch (Figure 4a) are closed. In this interval, C is charged to the connected input (V1) less the inverter's bias voltage (V_S, approximately 1.6V). In the second cycle (Figure 4b), these two switches are opened and the other (V2) input's switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter's open loop gain. The inverter's input ($V_{S'}$) becomes

$$V_{S'} = V_S + (V2 - V1)\frac{C}{C + C_S}$$

and the output will go High or Low depending on the sign of $V_{S'}$-V_S.

The actual circuitry used in the ADC0820 is a simple but important expansion of the basic comparator described above. By adding a second capacitor and another set of switches to the input (Figure 5), the scheme can be expanded to make dual differential comparisons. In this circuit, the feedback switch and one input switch on each capacitor (Z switches) are closed in the zeroing cycle. A comparison is then made by connecting the second input on each capacitor (S switches) and opening all of the other switches. The change in voltage at the inverter's input, as a result of the change in charge on each input capacitor, will now depend on both input signal differences.

Architecture

In the ADC0820, 15 comparators are used in the MS and LS 4-bit flash A/D converters. The MS (most significant) flash ADC also has one additional comparator to detect input overrange. These two sets of comparators operate alternately, with one group in its zeroing cycle while the other is comparing.

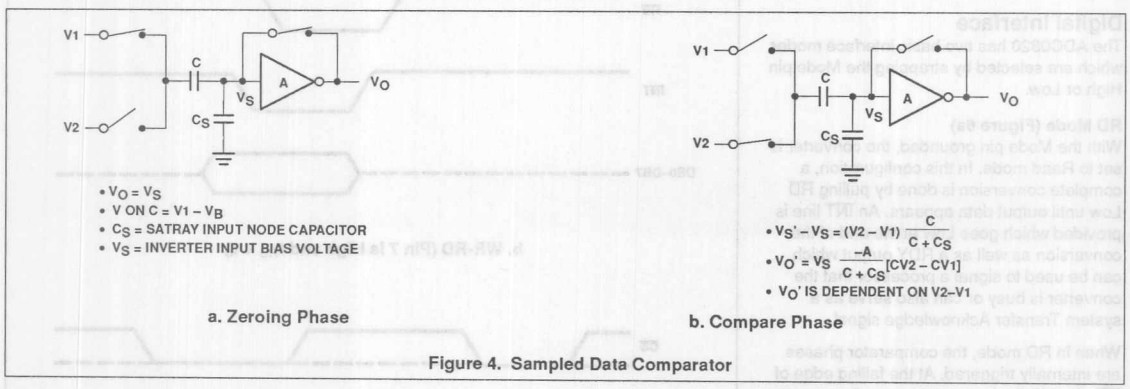


Figure 4. Sampled Data Comparator

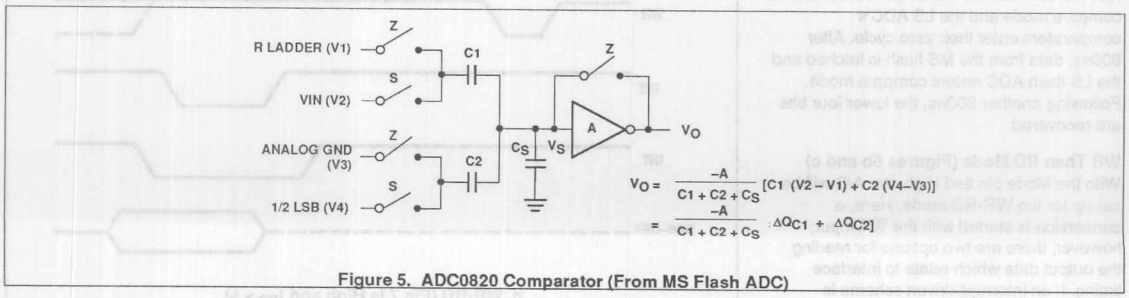


Figure 5. ADC0820 Comparator (From MS Flash ADC)

8-Bit, high-speed, μP-compatible A/D converter with track/hold function

To start a conversion in the WR-RD mode, the $\overline{WR}$ line is brought Low. At this instant the MS comparators go from zeroing to comparison mode (Figure 8). When $\overline{WR}$ is returned High after at least 600ns, the output from the first set of comparators (the first flash) is decoded and latched. At this point the two 4-bit converters change modes and the LS (least significant) flash ADC enters its compare cycle. No less than 600ns later, the $\overline{RD}$ line may be pulled Low to latch the lower four data bits and finish the 8-bit conversion. When $\overline{RD}$ goes Low, the flash A/Ds change state once again in preparation for the next conversion.

Figure 8 also outlines how the converter's interface timing relates to its analog input (V_{IN}). In WR-RD mode, V_{IN} is measured while $\overline{WR}$ is Low. In RD mode, sampling occurs during the first 800ns of $\overline{RD}$. Because of the input connections to the ADC0820's LS and MS comparators, the converter has the ability to sample V_{IN} at one instant, despite the fact that two separate 4-bit conversions are being done. More specifically, when $\overline{WR}$ is Low the MS flash is in compare mode (connected to V_{IN}, and the LS flash is in zero mode (also connected to V_{IN}). Therefore both flash ADCs sample V_{IN} at the same time.

Digital Interface

The ADC0820 has two basic interface modes which are selected by strapping the Mode pin High or Low.

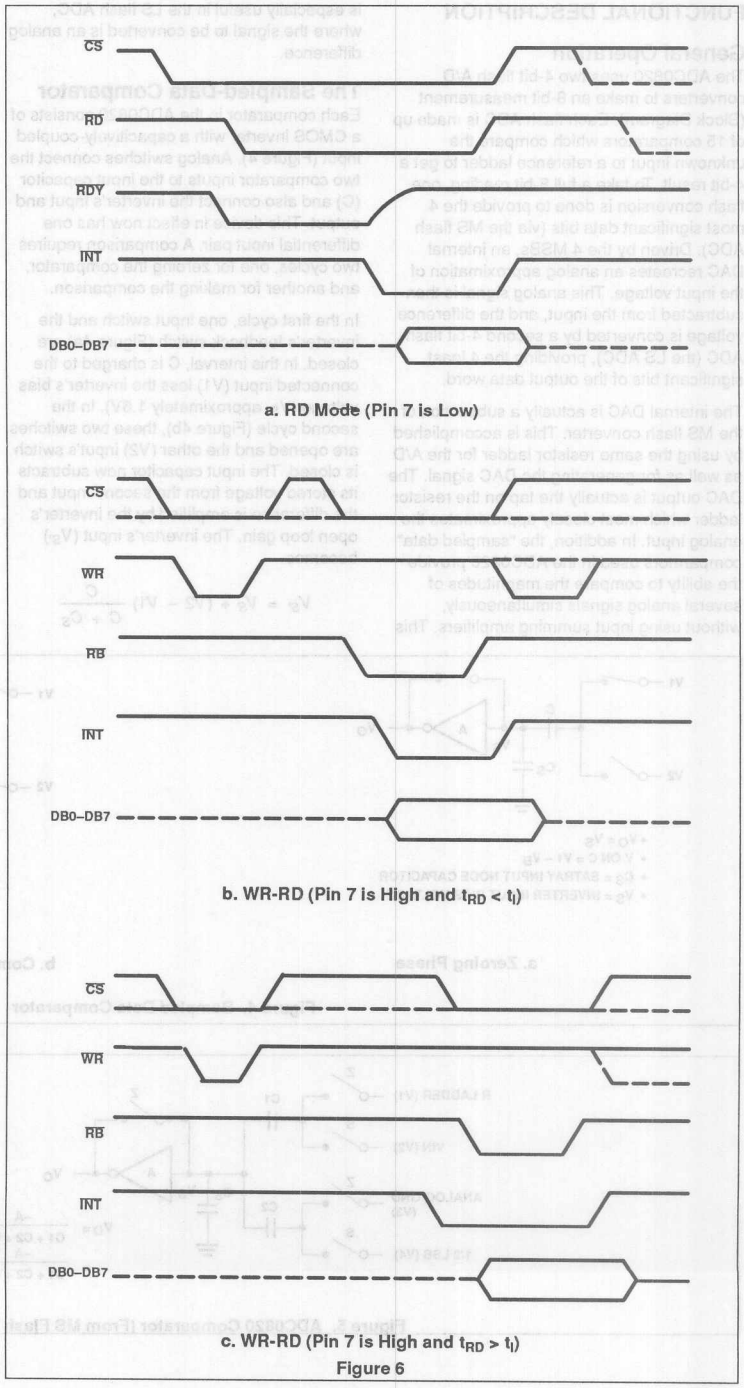
RD Mode (Figure 6a)

With the Mode pin grounded, the converter is set to Read mode. In this configuration, a complete conversion is done by pulling $\overline{RD}$ Low until output data appears. An $\overline{INT}$ line is provided which goes Low at the end of the conversion as well as a RDY output which can be used to signal a processor that the converter is busy or can also serve as a system Transfer Acknowledge signal.

When in RD mode, the comparator phases are internally triggered. At the falling edge of $\overline{RD}$, the MS flash converter goes from zero to compare mode and the LS ADC's comparators enter their zero cycle. After 800ns, data from the MS flash is latched and the LS flash ADC enters compare mode. Following another 800ns, the lower four bits are recovered.

WR Then RD Mode (Figures 6b and c)

With the Mode pin tied High, the A/D will be set up for the WR-RD mode. Here, a conversion is started with the $\overline{WR}$ input; however, there are two options for reading the output data which relate to interface timing. If an interrupt-driven scheme is desired, the user can wait for $\overline{INT}$ to go Low



a. RD Mode (Pin 7 is Low)

b. WR-RD (Pin 7 is High and $t_{RD} < t_I$)

c. WR-RD (Pin 7 is High and $t_{RD} > t_I$)

Figure 6

before reading the conversion result. $\overline{INT}$ will typically go Low 800ns after $\overline{WR}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{INT}$ and can exercise a Read after only 600ns. If this is done, $\overline{INT}$ will immediately go Low and data will appear at the outputs.

Stand-Alone (Figure 7)
For stand-alone operation in WR-RD mode, $\overline{CS}$ and $\overline{RD}$ can be tied Low and a conversion can be started with $\overline{WR}$. Data will be valid approximately 800ns following $\overline{WR}$'s rising edge.

Other Interface Considerations

In order to maintain conversion accuracy, $\overline{WR}$ has a maximum width spec of 50µs. When the MS flash ADC's sampled data comparators are in comparison mode ($\overline{WR}$ is Low), the input capacitors (C, Figure 5) must hold their charge. Switch leakage can cause errors if the comparator is left in this phase for too long.

Since the MS flash ADC enters its zeroing phase at the end of a conversion, a new conversion cannot be started until this phase is complete. The minimum spec for this time is 500ns (t_P in Figure 1, 2, 3a, and 3b).

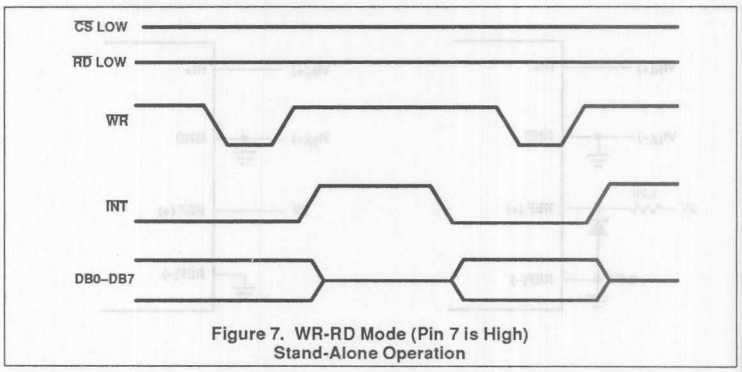


Figure 7. WR-RD Mode (Pin 7 is High) Stand-Alone Operation

ANALOG CONSIDERATIONS

Reference and Input

The two V_{REF} inputs of the ADC0820 are fully differential and define the zero- to full-scale input range of the A/D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing $V_{REF}(V_{REF}=V_{REF}(+) - V_{REF}(-))$ to less than 5V, the sensitivity of the converter can be increased (i.e., if V_{REF}=2V, then 1 LSB=7.8mV). The input/reference arrangement also facilitates ratiometric operation and, in many cases, the chip power supply can be used for transducer power as well as the V_{REF} source.

This reference flexibility lets the input span not only be varied, but also offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes. Though V_{IN} is not itself differential, the reference design affords nearly differential-input capability for most measurement applications. Figure 9 shows some of the configurations that are possible.

Input Current

Due to the unique conversion techniques employed by the ADC0820, the analog input behaves somewhat differently than in conventional devices. The A/D's sampled data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the ADC0820 is shown in Figure 10a. When a conversion starts ($\overline{WR}$ Low, WR-RD mode), all input switches close, connecting V_{IN} to 31 1pF capacitors. Although the two 4-bit flash circuits are not both in their compare cycle at the same time, V_{IN} still sees all input capacitors at once. This is because the MS flash converter is connected to the input during its compare interval and the LS flash is connected to the input during its zeroing phase. In other words, the LS ADC uses V_{IN} as its zero-phase input.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 5kΩ to 10kΩ). In addition, about 12pF of input stray capacitance must also be charged. For large source resistances, the analog input can be modeled as an RC network as shown in Figure 10b. As R_S increases, it will take longer for the input capacitance to charge.

In RD mode, the input switches are closed for approximately 800ns at the start of the conversion. In WR-RD mode, the time that the switches are closed to allow this charging is the time that $\overline{WR}$ is Low. Since other factors force this time to be at least 600ns, input time constants of 100ns can be accommodated without special consideration. Typical total input capacitance values of 45pF allow R_S to be 1.5kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

Input Filtering

It should be made clear that transients in the analog input signal, caused by charging current flowing into V_{IN}, will not degrade the A/D's performance in most cases. In effect, the ADC0820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is Low, so at least 600ns will be provided to charge the ADC's input capacitance. It is

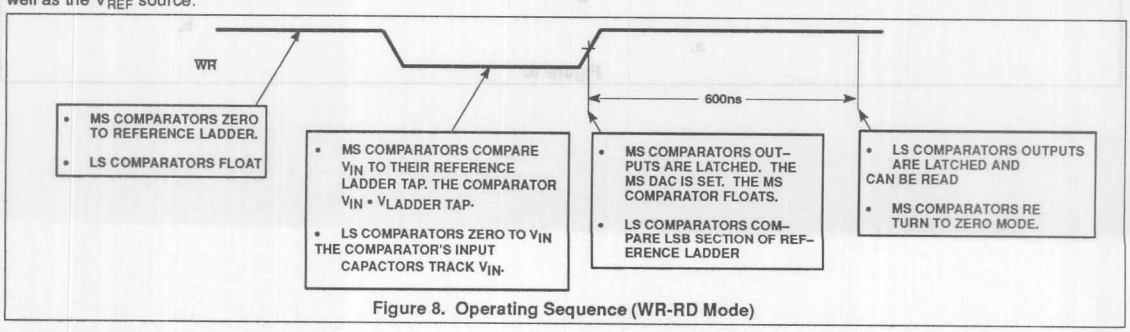
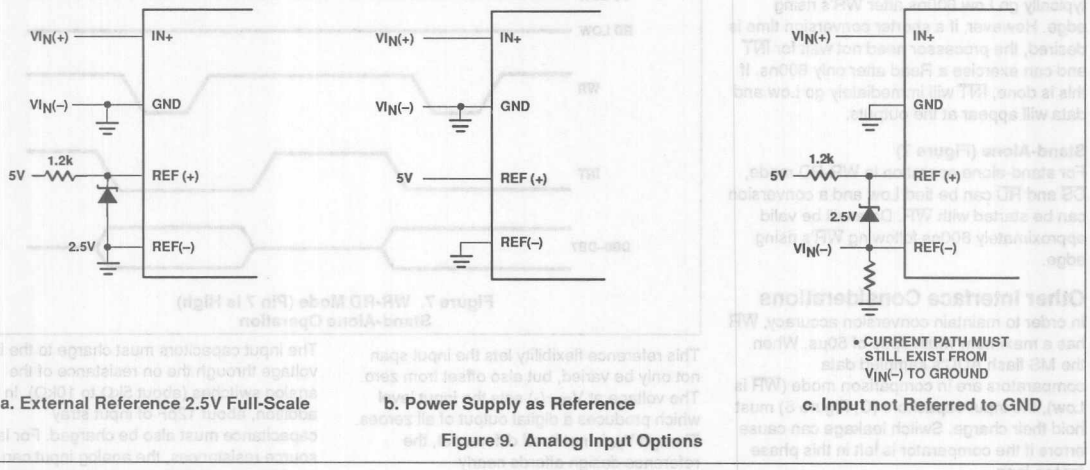


Figure 8. Operating Sequence (WR-RD Mode)

8-Bit, high-speed, μP-compatible A/D converter with track/hold function



a. External Reference 2.5V Full-Scale b. Power Supply as Reference c. Input not Referred to GND

Figure 9. Analog Input Options

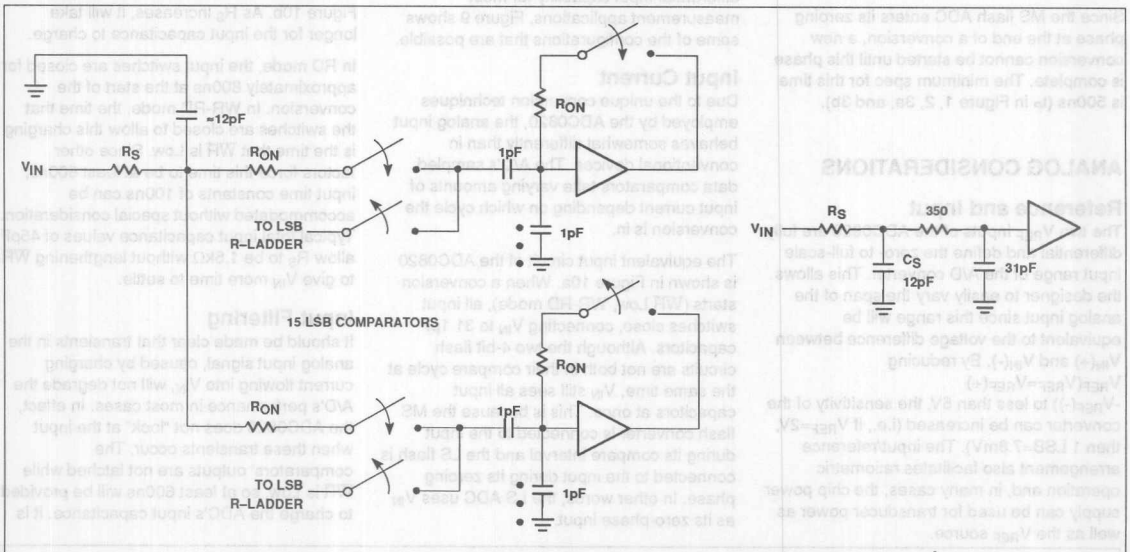


Figure 10

therefore not necessary to filter out these transients by putting an external cap on the V_{IN} terminal, if an input amplifier that can settle within 600ns is used to drive the input. The NE530 is a suitable op amp for driving the input of the ADC0820.

Inherent Sample-Hold

Another benefit of the ADC0820's input mechanism is its ability to measure a variety of high-speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain at least LSB stable throughout the conversion process if full accuracy is to be maintained. Consequently, for many high-speed signals, this signal must be externally sampled, and held stationary during the conversion.

Sampled data comparators, by nature of their input switching, already accomplish this function to a large degree (Section 1.2). Although the conversion time for the ADC0820 is 1.5µs, the time through which V_{IN} must be 1/2LSB stable is much smaller. Since the MS flash ADC uses V_{IN} as its "compare" input and the LS ADC uses V_{IN} as its "zero" input, the ADC0820 only "samples" V_{IN} when $\overline{WR}$ is Low. Even though the two flashes are not done simultaneously, the analog signal is measured at one instant. The value of V_{IN} approximately 100ns after the rising edge of $\overline{WR}$ (100ns due to internal logic propagation delay) will be the measured value.

Input signals with slew rates typically below 100mV/µs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the ADC0820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. An SAR type converter with a conversion time as fast as 1µs would still not be able to measure a 5V, 1kHz sine wave without the aid of an external sample-and-hold. The ADC0820, with no such help, can typically measure 5V, 7kHz waveforms.

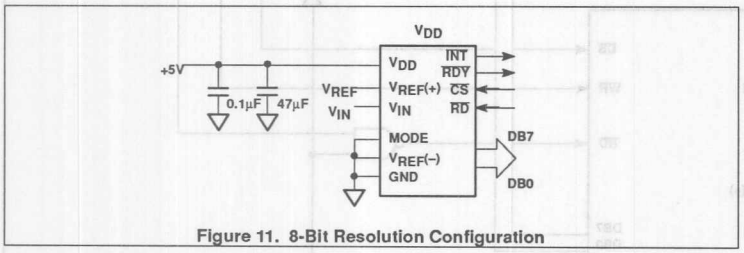


Figure 11. 8-Bit Resolution Configuration

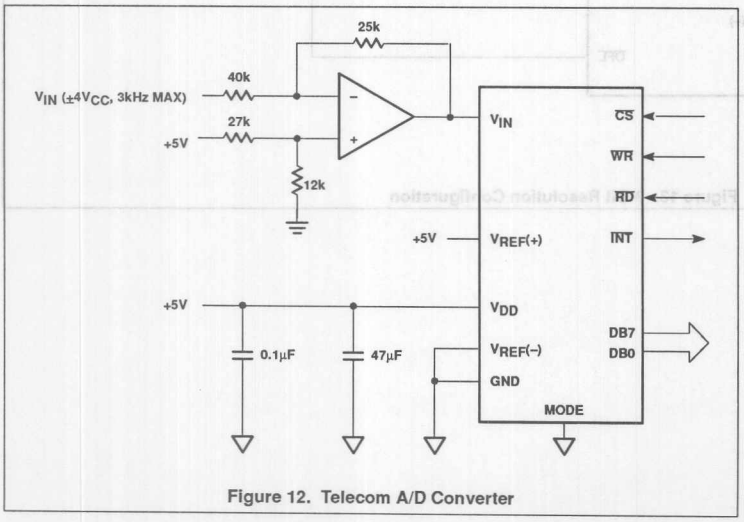


Figure 12. Telecom A/D Converter

8-Bit, high-speed, μP-compatible A/D converter with track/hold function

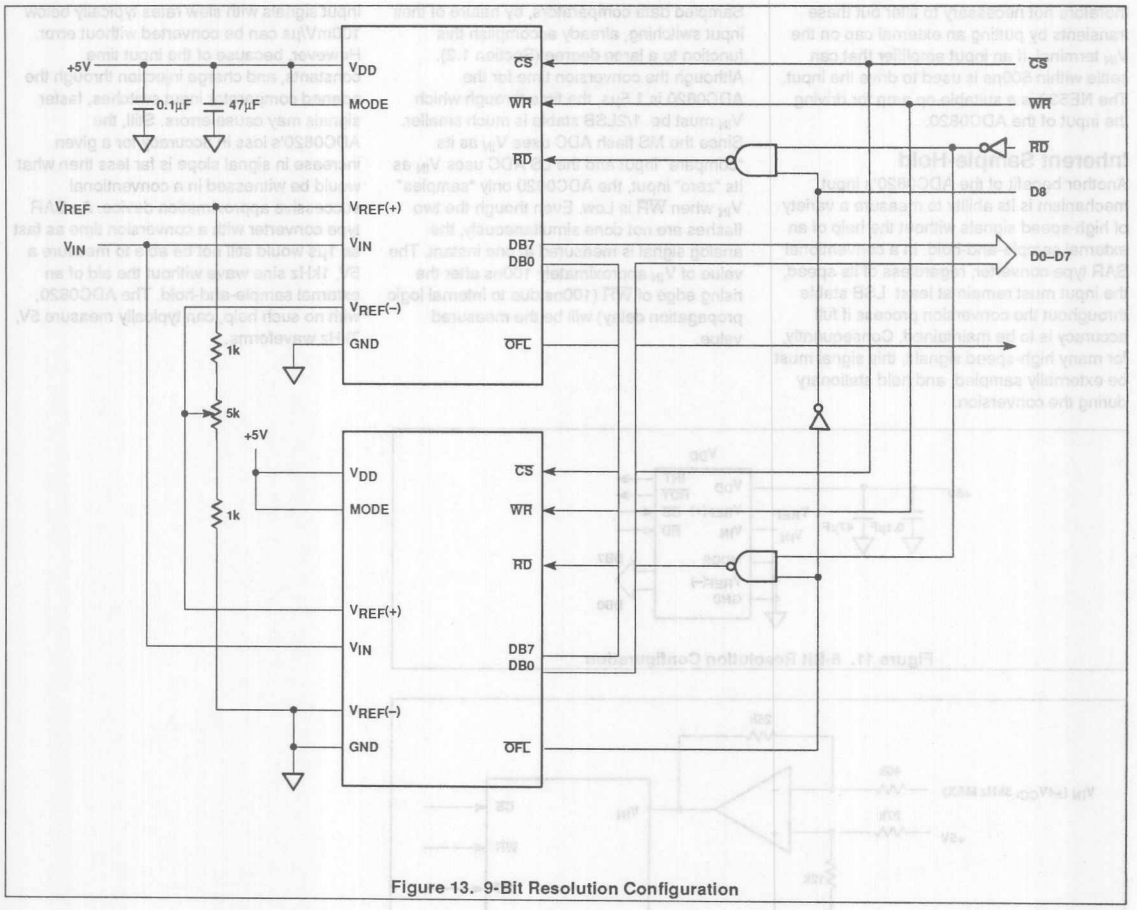


Figure 13. 9-Bit Resolution Configuration

6-Bit A/D converter (parallel outputs) NE5037

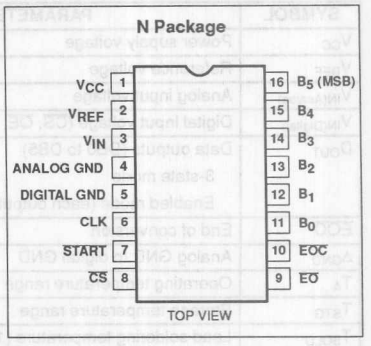
DESCRIPTION

The NE5037 is a low cost, complete successive-approximation analog-to-digital (A/D) converter, fabricated using Bipolar/I^2L technology. With an external reference voltage, the NE5037 will accept input voltages between 0V and V_{REF}. An external $\overline{START}$ pulse of at least 300ns in duration will provide the 6-bit result of the conversion in parallel format. Full conversion with no missing codes occurs in 9µs.

APPLICATIONS

- Temperature control
- µP-based appliances
- Light level monitors
- Head position sensing
- Electronic toys
- Joystick interface

PIN CONFIGURATION



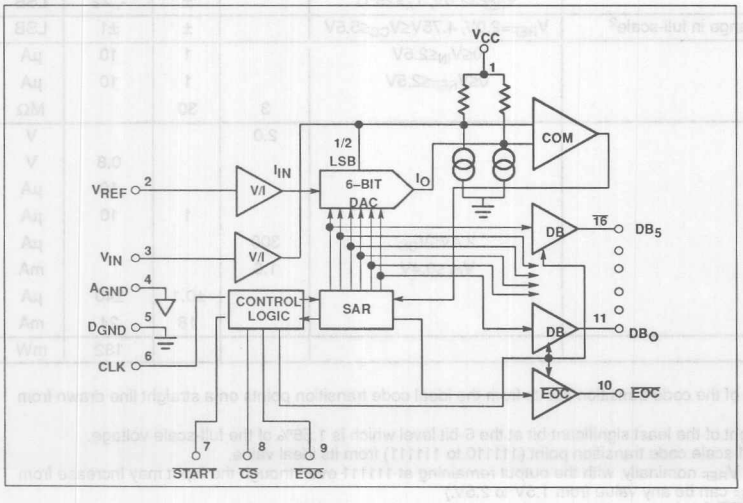
FEATURES

- TTL-compatible inputs and outputs
- 3-State output buffer
- Easy interface to CMOS microprocessors
- Fast conversion—9µs
- Guaranteed no missing codes over full temp range
- Single-supply operation, +5V
- Positive true binary outputs
- High-impedance analog inputs

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE5037N

BLOCK DIAGRAM



6-Bit A/D converter (parallel outputs) NE5037

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN(Analog)}$	Analog input voltage	7	V
$V_{IN(Digital)}$	Digital input voltage ($\overline{CS}$, $\overline{OE}$, $\overline{START}$, CLK)	7	V
D_{OUT}	Data outputs (DB0 to DB5) 3-state mode Enabled mode (each output)	 7 5	 V mA
$\overline{EOC}$	End of conversion	V_{CC}	
Δ_{GND}	Analog GND to digital GND	±1	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C
P_D	Maximum power dissipation, T_A=25°C (still-air)[1] N package	 1450	 mW

NOTES:
1. Derate above 25°C at the following rates:
   F package=9.5mW/°C
   N package=11.6mW/°C
   D package=8.7mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}=5.0V; V_{REF}=2.0V; Clock=1MHz; 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		6	6	6	Bits
	Relative accuracy[1,2]					LSB
V_{CC}	Positive supply voltage		+4.75	+5.0	+5.50	V
ε_{FS}	Full-scale gain error[2,3,4]	V_{REF}=2.0V, T_A=25°C		±1	±2	LSB
ε_{ZS}	Zero-scale offset error[2]	V_{REF}=2.0V, T_A=25°C		±	-, +2	LSB
PSR	Power supply rejection, Max change in full-scale[2]	V_{REF}=2.0V, 4.75V≤V_{CC}≤5.5V		±	±1	LSB
I_{IN}	Analog input bias current	0≤V_{IN}≤2.5V		1	10	µA
I_{REF}	Reference bias current	0≤V_{REF}≤2.5V		1	10	µA
R_{IN}	Analog input resistance		3	30		MΩ
V_{IH}	Logic "1" input voltage		2.0			V
V_{IL}	Logic "0" input voltage				0.8	V
I_{IH}	Logic "1" input current				10	µA
I_{IL}	Logic "0" input current			1	10	µA
I_{OH}	Logic "1" output current[5]	2.4V≤V_{OH}	300			µA
I_{OL}	Logic "0" output current[5]	V_{OL}≤0.4V	1.6			mA
I_{OZ}	3-State leakage current			±0.1	±40	µA
I_{CC}	Positive supply current			18	24	mA
P_D	Power dissipation				132	mW

NOTES:
1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero-scale to full-scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the 6-bit level which is 1.56% of the full-scale voltage.
3. Full-scale gain error is the deviation of the full-scale code transition point (111110 to 111111) from its ideal value.
4. The analog input voltage (V_{IN}) range is 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC}. (For optimum performance, V_{REF} can be any value from 1.5V to 2.5V.)
5. The data outputs have active pull-ups. The $\overline{EOC}$ line is open-collector with a nominal 5kΩ internal pull-up resistor.

6-Bit A/D converter (parallel outputs) NE5037

AC ELECTRICAL CHARACTERISTICS

V_{CC}=5.0V; V_{REF}=2.0V; Clock=1MHz; 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C (Refer to AC test figures.)

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
f_{MAX}	Maximum clock frequency				1			MHz
t_W	Start pulse width				300			ns
	Minimum positive/negative clock pulse width				300			ns
t_{CONV}	Conversion time						9	Clock cycles
$t_{P\ (OUT\ DATA)}$	Propagation delay[1]	Data out	$\overline{OE}$	T_A=25°C t_R=t_F≤20ns			500	ns
$t_{P\ (OUT\ EOC)}$	Propagation delay[2]	$\overline{EOC}$	Clock	T_A=25°C t_R=t_F≤20ns			800	ns
$t_{P\ (3\text{-}STATE)}$	Propagation delay, 3-State	3-State Data	$\overline{OE}$	T_A=25°C t_R=t_F≤20ns			500	ns

NOTES:
1. Propagation delay of data outputs is defined as the delay in the data outputs reading their final value after the low going edge of $\overline{OE}$.
2. Propagation delay of $\overline{EOC}$ is defined as the delay in $\overline{EOC}$ going low, following the low going edge of the 9th clock pulse after the start pulse.

CIRCUIT DESCRIPTION

NE5037 is a complete 6-bit, parallel output, microprocessor compatible, A/D converter which incorporates the successive-approximation method. The chip includes the internal control logic, the successive-approximation register (SAR), 6-bit DAC, comparator and output buffers. An externally-generated clock source (max frequency=1MHz) must be provided to Pin 6. An external reference voltage supplied to Pin 2 sets the full-scale range of the A/D converter.

The $\overline{CS}$ pin must be at a low level prior to the start of the conversion process. Upon receipt of a $\overline{START}$ pulse, the internal control logic resets the SAR. On the first low-going edge of the clock pulse, successive approximation conversion commences. Successive bits beginning with the MSB (D5) are supplied to the input of the internal 6-bit current output DAC by the I^2L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, which is converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to "0' and the corresponding output buffer goes to "0' simultaneously. If it is less, it stays at '1' and the output buffer also stays at '1'. On successive clock pulses, successive bits of the DAC are tried and the corresponding output buffer represents the bits of the DAC. On the eighth low-going edge of the clock pulse (after the receipt of the start pulse), the $\overline{EOC}$ pin goes low, thereby indicating that the conversion is complete. The output data is now valid. In order to access the result of the conversion, the $\overline{OE}$ pin must be set to a low level. $\overline{EOC}$ is reset to a high state when $\overline{OE}$ is low. When $\overline{OE}$ is in a "1' state, the output buffers are in a high impedance state.

Refer to 1 for the timing diagram.

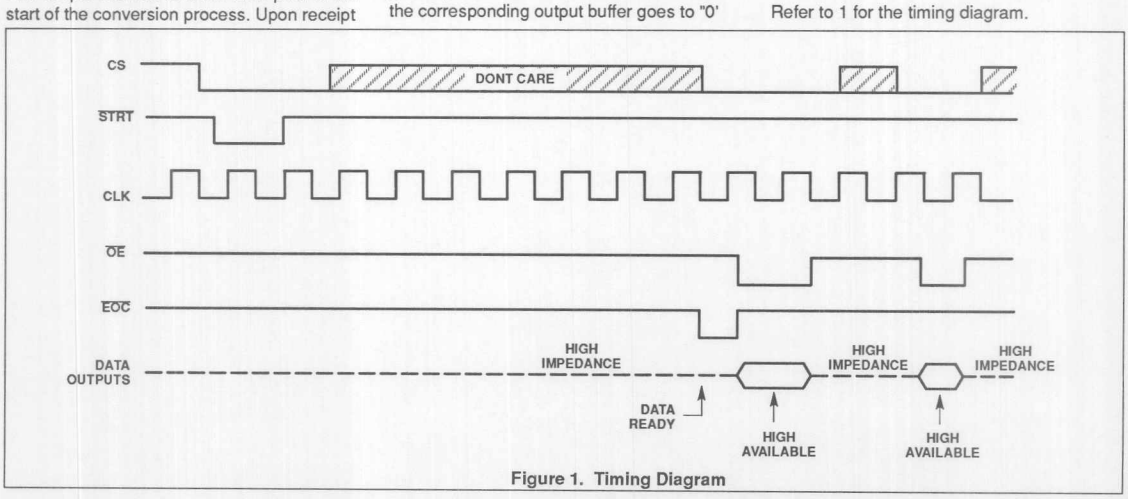


Figure 1. Timing Diagram

6-Bit A/D converter (parallel outputs) NE5037

TRANSFER CHARACTERISTICS

The ideal transfer characteristic of the NE5037 is shown in 2.

The NE5037 is designed to have a nominal LSB offset so that the code transition points are located LSB on either side of the exact analog inputs for a given code.

Thus the first transition (000000 to 000001) will occur at an input of LSB (15.63mV with a V_{REF} of 2.0V). Subsequent transitions will occur at nominal increments of 1 LSB. The last transition (to full-scale—111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

LAYOUT PRECAUTIONS

Analog ground (Pin 4) and digital ground (Pin 5) are not connected internally and should be connected together as close to the device as possible for optimum performance. The circuit will operate with as much as ±200mV between the two grounds but some degradation will occur. The leads to the analog inputs should be kept as short as possible to minimize noise pick-up. Input bypass capacitors from the analog inputs to ground will eliminate noise pick-up. Power supplies should be decoupled with at least 1µF located close to the device to minimize the effects of noise spikes.

The reference input and the analog voltage input must both remain stable during conversion to insure accuracy and proper operation. This can be done by adequately bypassing these inputs and/or keeping the impedance of these inputs at or below 2kΩ.

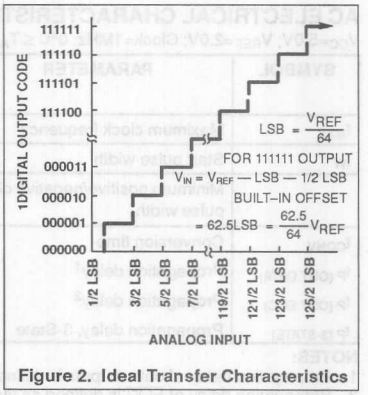
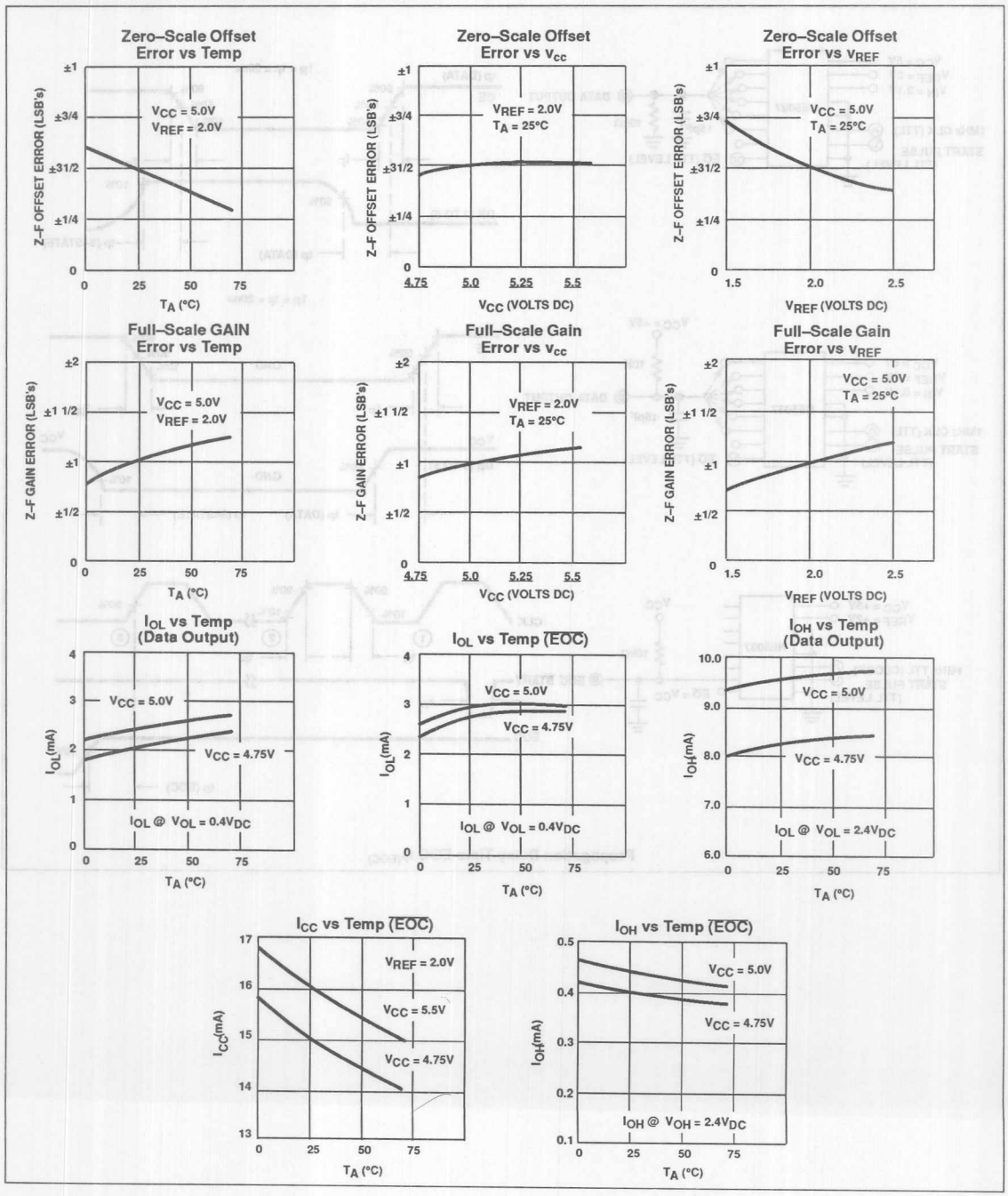
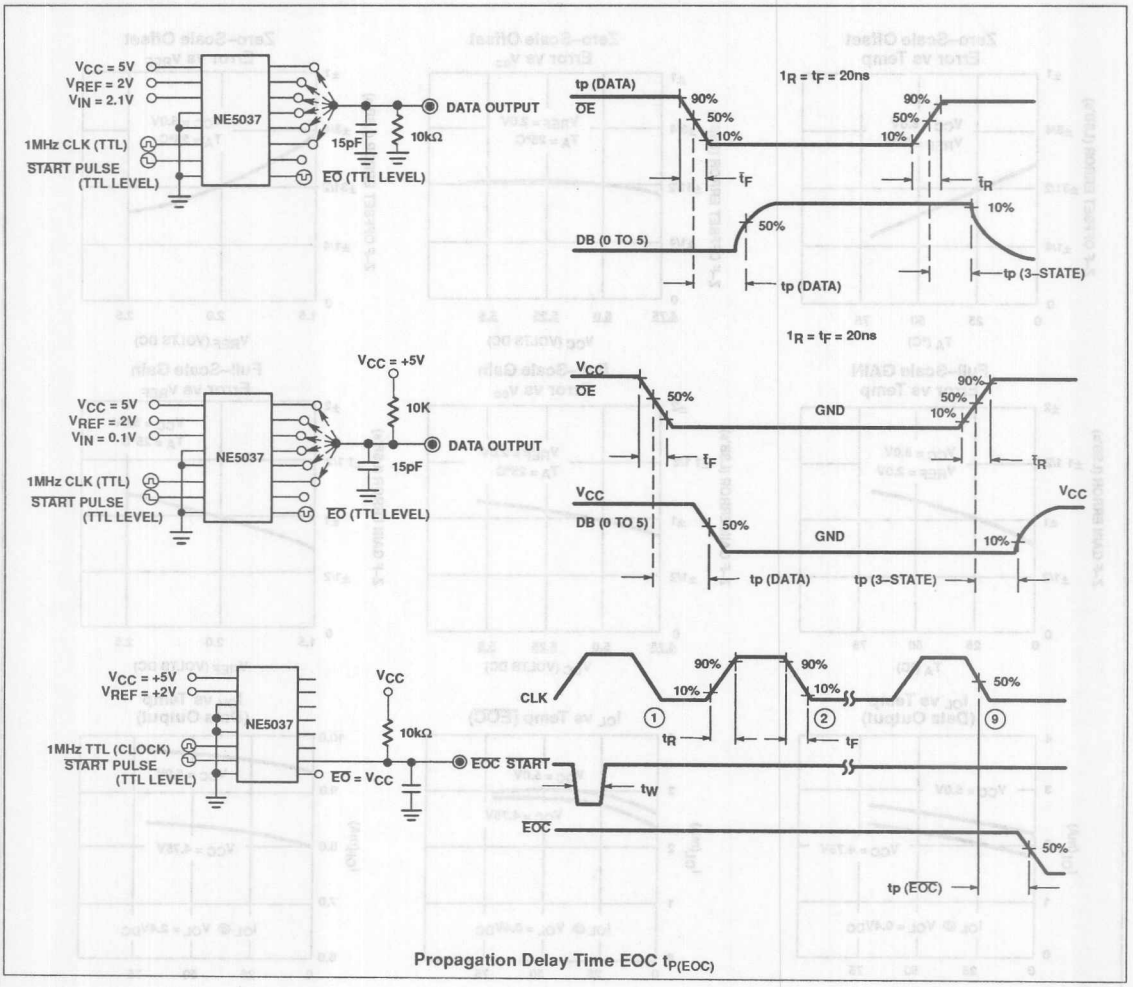


Figure 2. Ideal Transfer Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS



AC TEST CIRCUITS AND WAVEFORMS



Propagation Delay Time EOC $t_{P(EOC)}$

6-Bit A/D converter (parallel outputs) NE5037

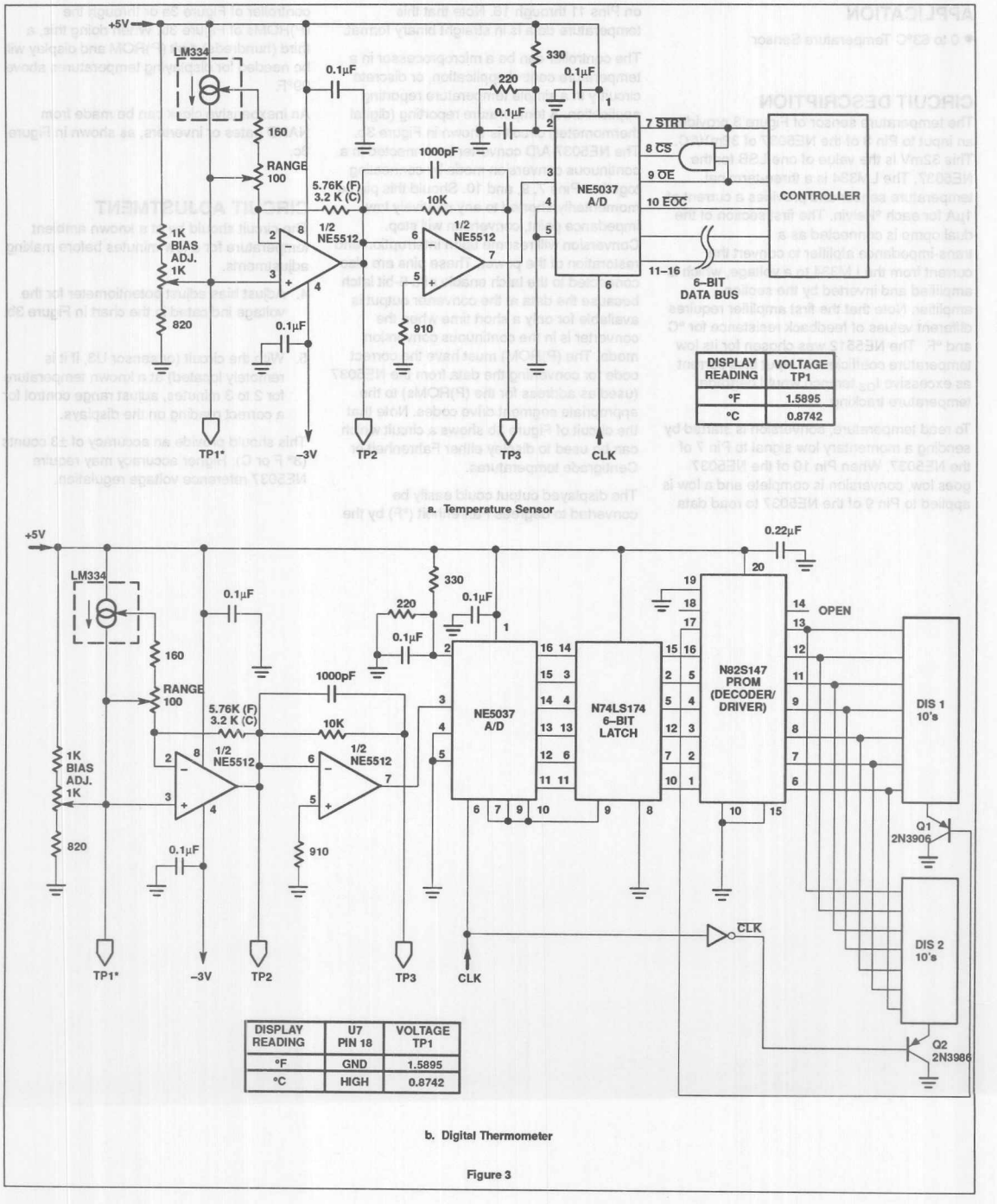


Figure 3

6-Bit A/D converter (parallel outputs) NE5037

APPLICATION

- 0 to 63°C Temperature Sensor

CIRCUIT DESCRIPTION

The temperature sensor of Figure 3 provides an input to Pin 3 of the NE5037 of 32mV/°C. This 32mV is the value of one LSB for the NE5037. The LM334 is a three-terminal temperature sensor and provides a current of 1μA for each °Kelvin. The first section of the dual opmp is connected as a trans-impedance afplifier to convert the current from the LM334 to a voltage, which is amplified and inverted by the section amplifier. Note that the first amplifier requires different values of feedback resistance for °C and °F. The NE5512 was chosen for its low temperature coefficient of input bias current as excessive I_{OS} tempco would degrade temperature tracking.

To read temperature, conversion is started by sending a momentary low signal to Pin 7 of the NE5037. When Pin 10 of the NE5037 goes low, conversion is complete and a low is applied to Pin 9 of the NE5037 to read data on Pins 11 through 16. Note that this temperature data is in straight binary format.

The controller can be a microprocessor in a temperature control application, or discrete circuitry in a simple temperature reporting application. A temperature reporting (digital thermometer) circuit is shown in Figure 3b. The NE5037 A/D converter is connected in a continuous conversion mode by connecting together Pins 7, 9, and 10. Should this pin be momentarily shorted to any relatively low impedance point, conversion will stop. Conversion will resume upon interruption and restoration of the power. These pins are also connected to the latch enable of a 6-bit latch because the data at the converter output is available for only a short time when the converter is in the continuous conversion mode. The (P)ROM) must have the correct code for converting the data from the NE5037 (used as address for the (P)ROMs) to the appropriate segment drive codes. Note that the circuit of Figure 3b shows a circuit which can be used to display either Fahrenheit or Centigrade temperatures.

The displayed output could easily be converted to degrees Fahrenheit (°F) by the controller of Figure 3a or through the (P)ROMs of Figure 3b. When doing this, a third (hundreds) digit (P)ROM and display will be needed for displaying temperatures above 99°F.

An inexpensive clock can be made from NAND gates or inverters, as shown in Figure 3c.

CIRCUIT ADJUSTMENT

The circuit should be at a known ambient temperature for a few minutes before making adjustments.

4. Adjust bias adjust potentiometer for the voltage indicated in the chart in Figure 3b.

5. With the circuit (or sensor U3, if it is remotely located) at a known temperature for 2 to 3 minutes, adjust range control for a correct reading on the displays.

This should provide an accuracy of ±3 counts (3° F or C). Higher accuracy may require NE5037 reference voltage regulation.

8-Bit A/D and D/A converter PCF8591

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

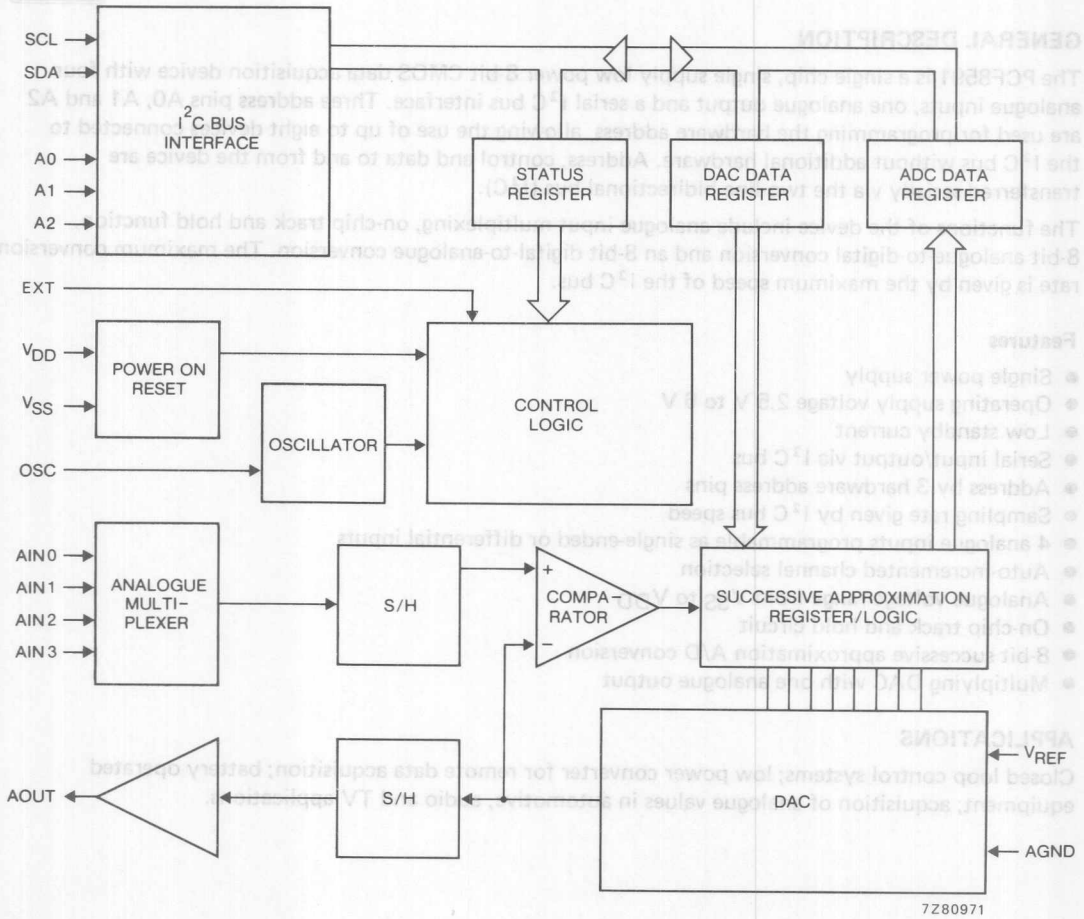


Fig. 1 Block diagram.

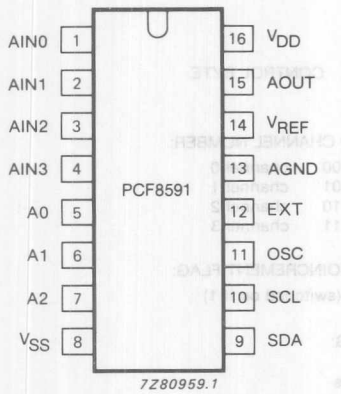


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I^2C bus data input/output
10.	SCL	I^2C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Adressing

Each PCF8591 device in an I^2C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I^2C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

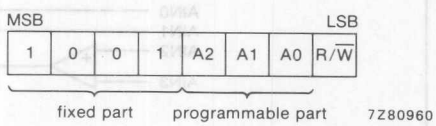


Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

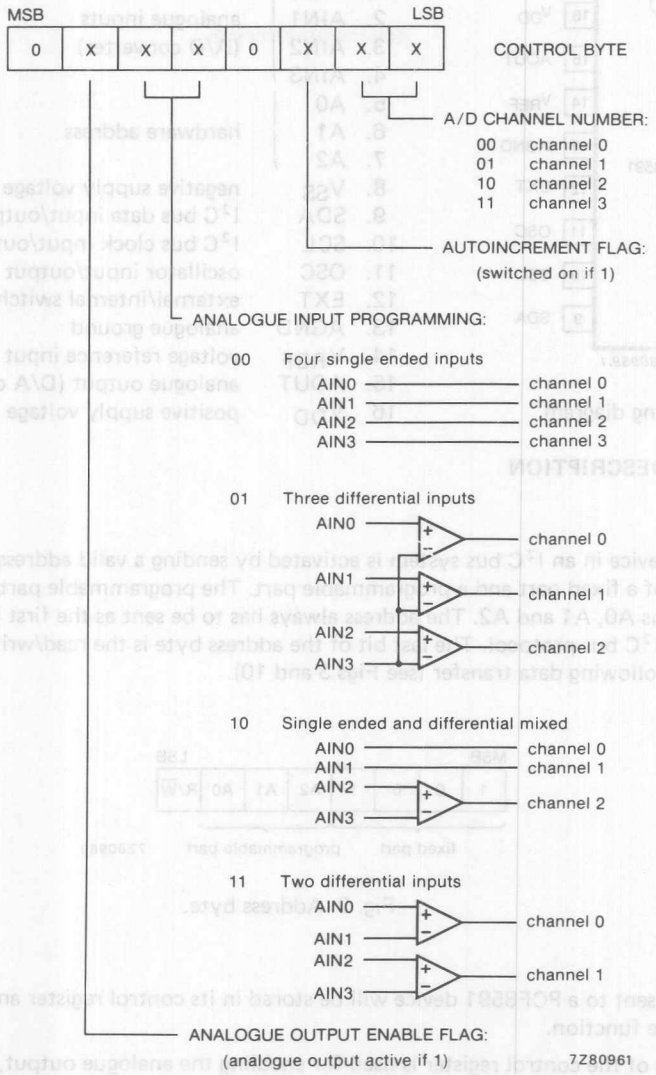


Fig. 4 Control byte.

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

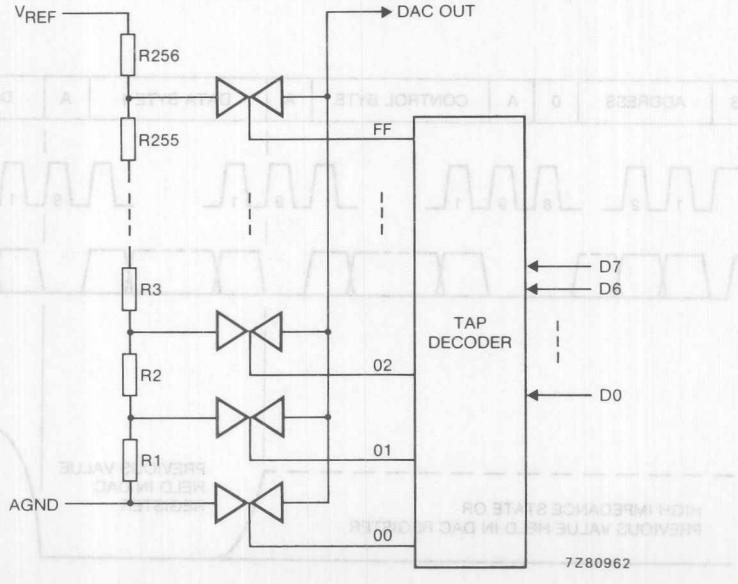


Fig. 5 DAC resistor divider chain.

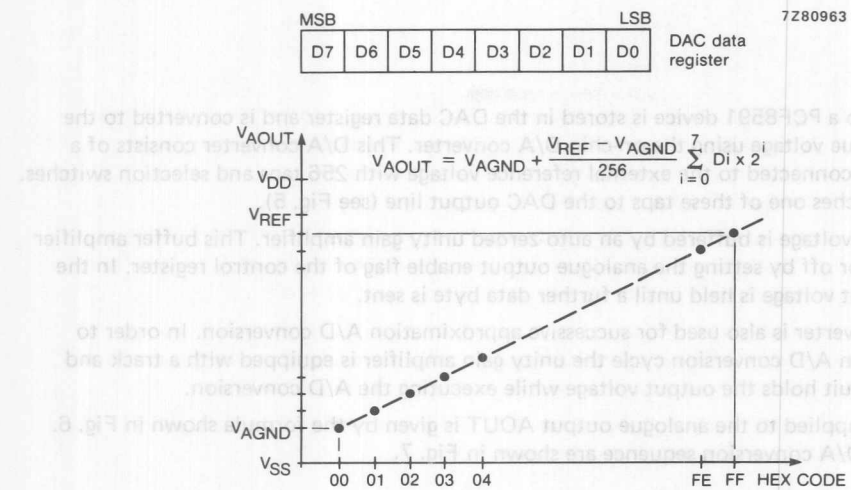


Fig. 6 DAC data and d.c. conversion characteristics.

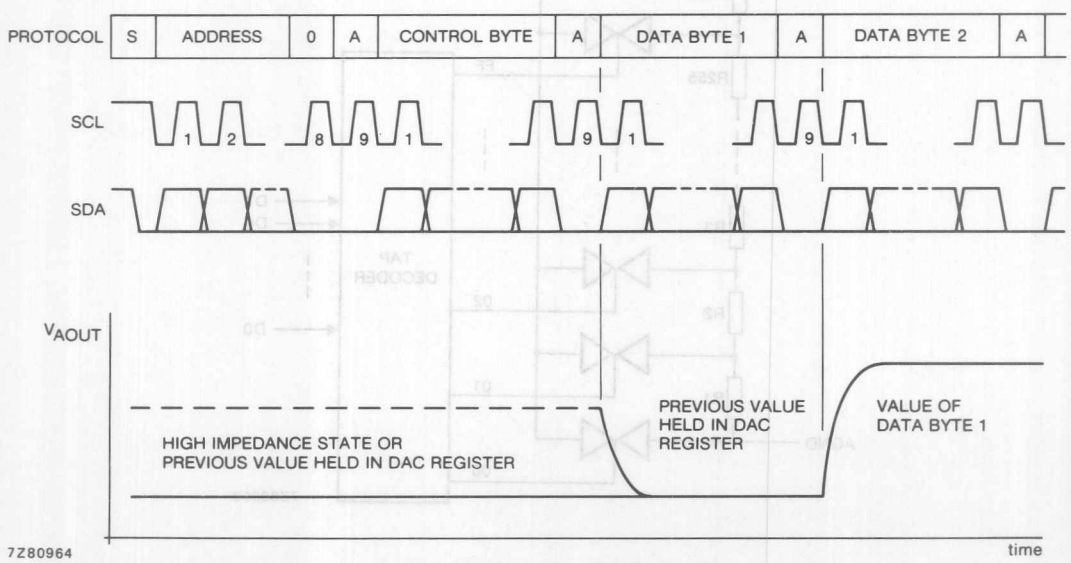


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I^2C bus.

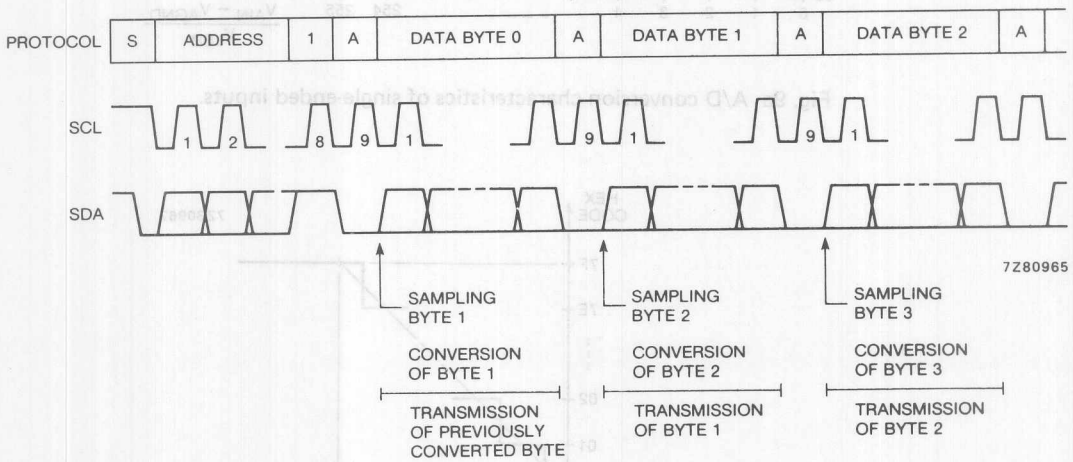


Fig. 8 A/D conversion sequence.

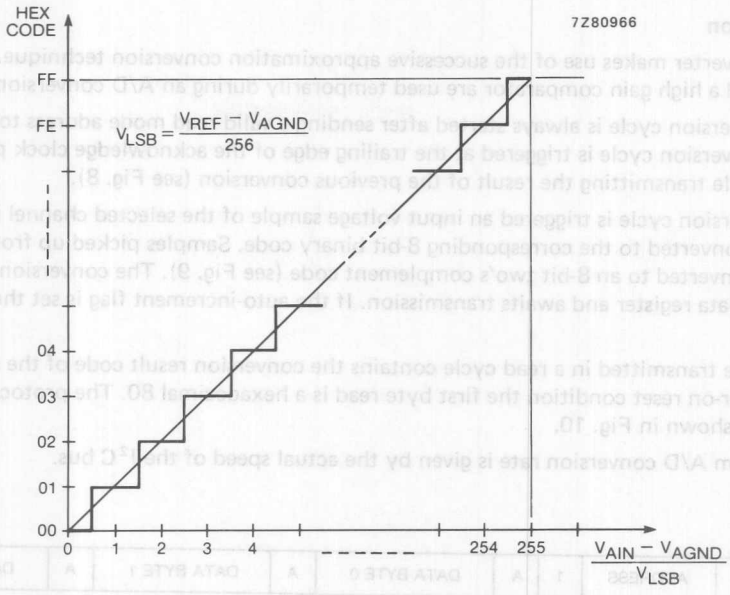


Fig. 9a A/D conversion characteristics of single-ended inputs.

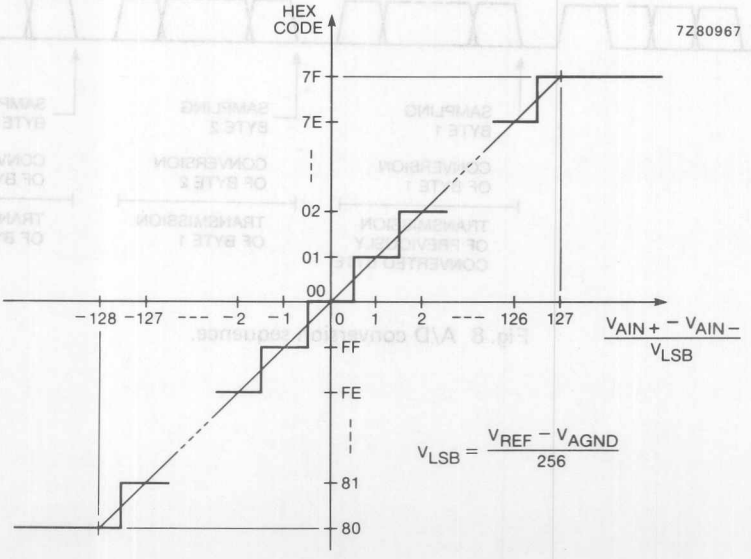


Fig. 9b A/D conversion characteristics of differential inputs.

Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

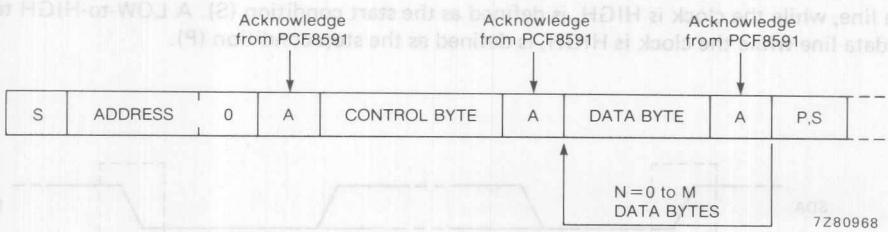


Fig. 10a Bus protocol for write mode, D/A conversion.

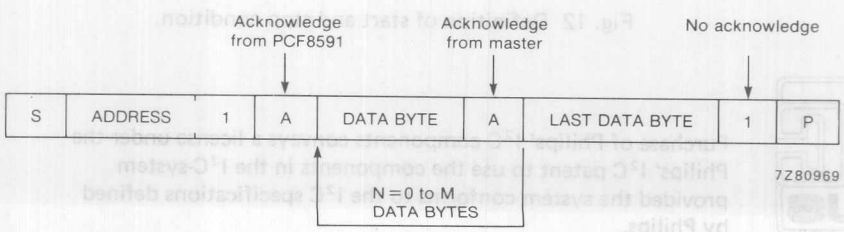


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

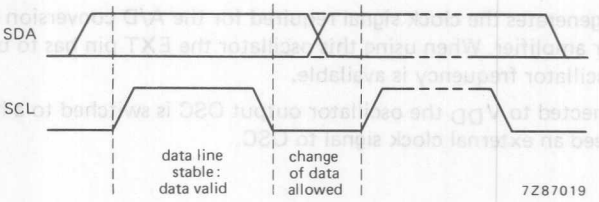


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

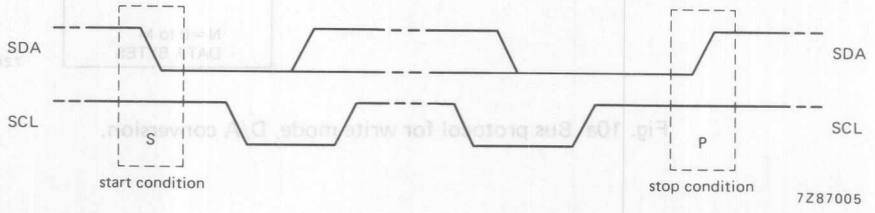


Fig. 12 Definition of start and stop condition.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

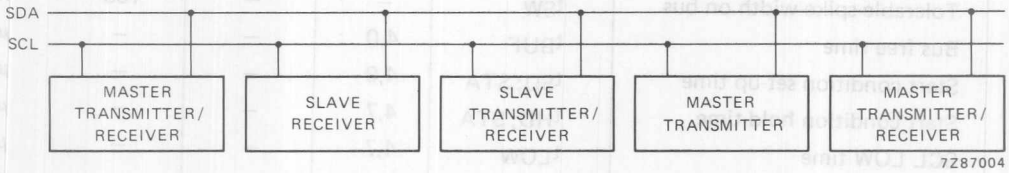


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

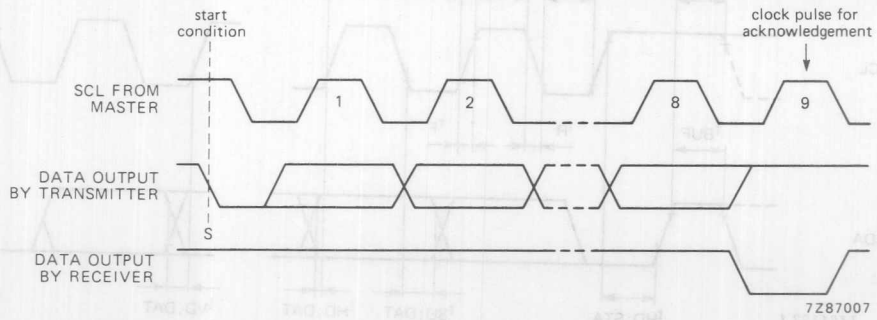


Fig. 14 Acknowledgement on the I^2C bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

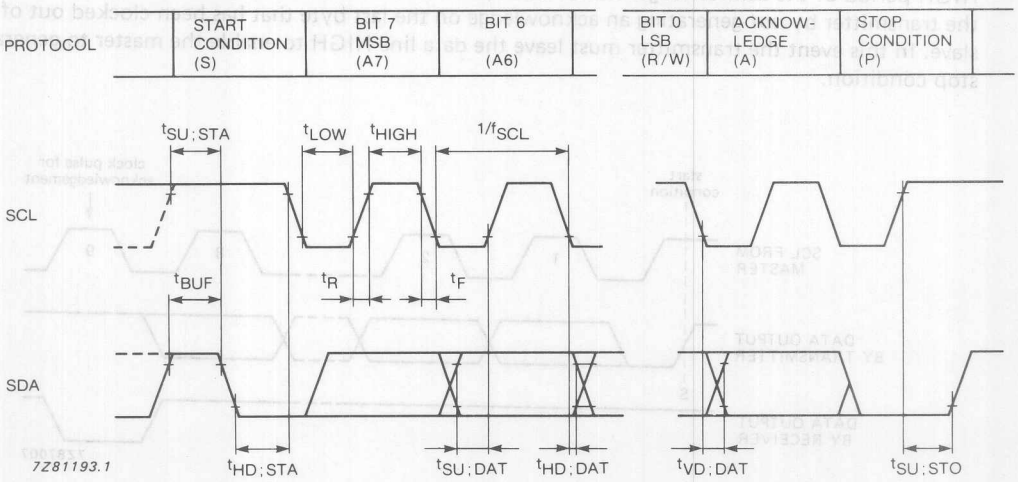


Fig. 15 I^2C bus timing diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby; $V_I = V_{SS}$ or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input current	leakage; $V_I = V_{SS}$ to V_{DD}	I_I	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
SDA output current	leakage; HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs						
Voltage range*	$V_{REF} > V_{AGND}$	V_{REF}	$V_{SS}+1,6$	–	V_{DD}	V
Voltage range*	$V_{REF} > V_{AGND}$	V_{AGND}	V_{SS}	–	$V_{DD}-0,8$	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = –40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	$0,9 \times V_{DD}$	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	μs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

* A further extension of the range is possible, if the following conditions are fulfilled:

$$\frac{V_{REF} + V_{AGND}}{2} \geqslant 0,8\ V \text{ and } V_{DD} - \frac{V_{REF} + V_{AGND}}{2} \geqslant 0,4\ V.$$

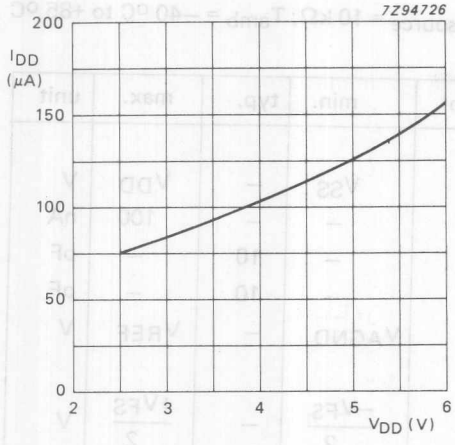
A/D CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

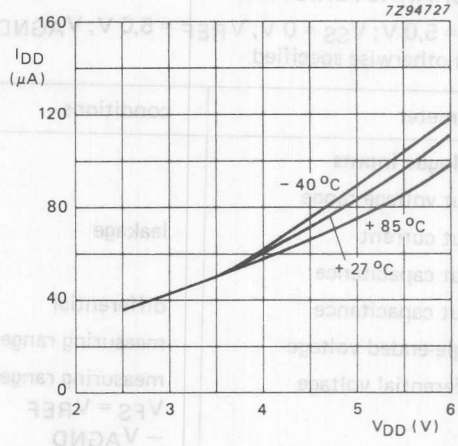
parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; $V_{DDN} = 0{,}1 \times V_{PP}$	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

Note

1. The power on reset circuit resets the I^2C bus logic when V_{DD} is less than V_{POR}.

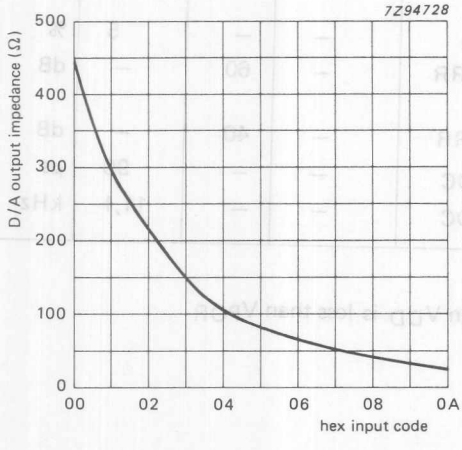


(a) internal oscillator; T_{amb} = + 27 °C.

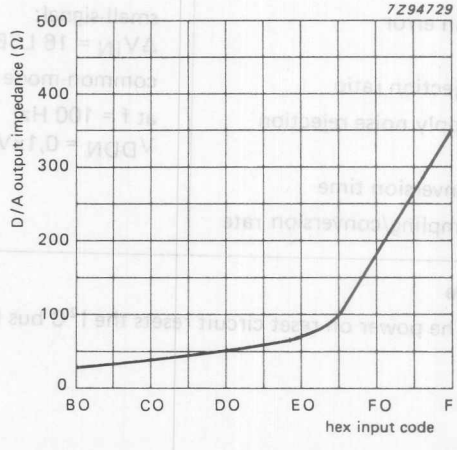


(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).



(a) output impedance near negative power rail; T_{amb} = + 27 °C.



(b) output impedance near positive power rail; T_{amb} = + 27 °C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors ($> 10\ \mu F$) are recommended for power supply and reference voltage inputs.

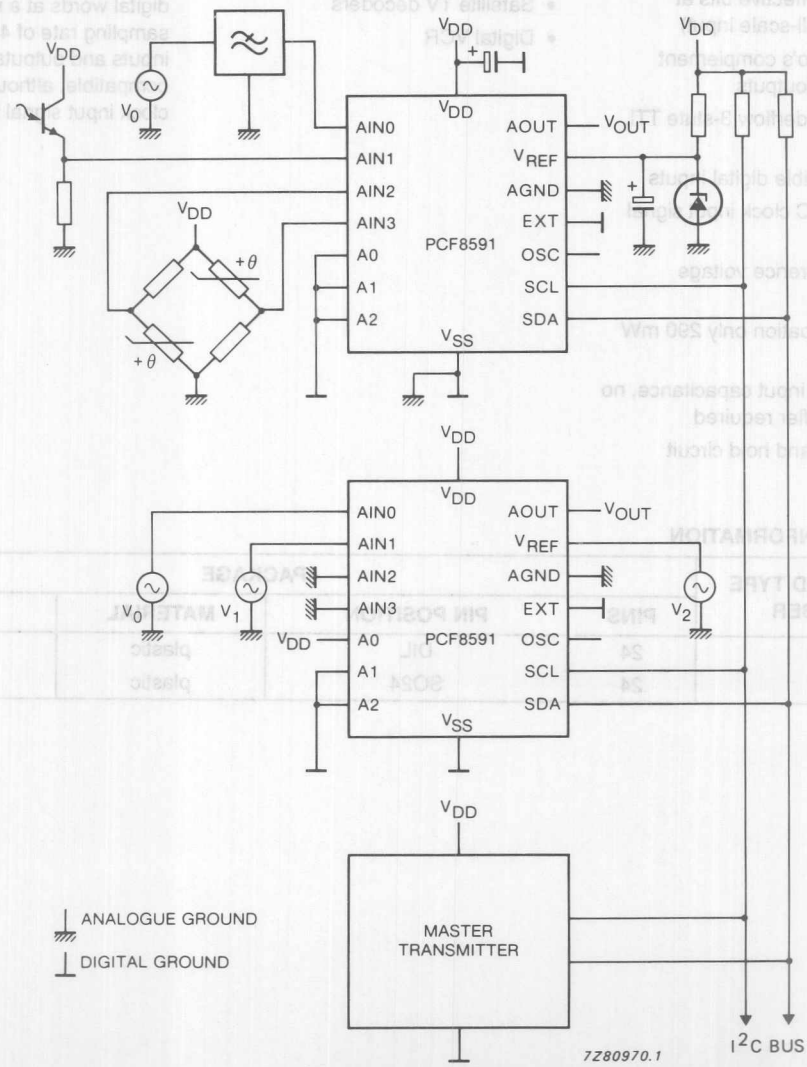


Fig. 18 Application diagram.

8-bit high-speed analog-to-digital converter

TDA8703/8703T

FEATURES

- 8-bit resolution
- Sampling rate up to 40 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.1 effective bits at 4.43 MHz full-scale input)
- Binary or two's complement 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Internal reference voltage generator
- Power dissipation only 290 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- General purpose high-speed analog-to-digital conversion
- Digital TV, IDTV
- Subscriber TV decoder
- Satellite TV decoders
- Digital VCR

GENERAL DESCRIPTION

The TDA8703 is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are TTL compatible, although a low-level AC clock input signal is allowed.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8703	24	DIL	plastic	SOT101
TDA8703T	24	SO24	plastic	SOT137A

8-bit high-speed analog-to-digital converter

TDA8703/8703T

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current		–	28	36	mA
I_{CCD}	digital supply current		–	19	25	mA
I_{CCO}	output stages supply current		–	11	14	mA
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
AILE	AC integral linearity error	note 1	–	–	±2	LSB
B	–3 dB bandwidth	note 2; f_{CLK} = 40 MHz	–	19.5	–	MHz
$f_{CLK}/f_{\overline{CLK}}$	maximum conversion rate	note 3	40	–	–	MHz
P_{tot}	total power dissipation		–	290	415	mW

Notes to the quick reference data

1. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}; $f_{\overline{CLK}}$ = 27 MHz).
2. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at input).
3. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

   If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

8-bit high-speed analog-to-digital converter

TDA8703/8703T

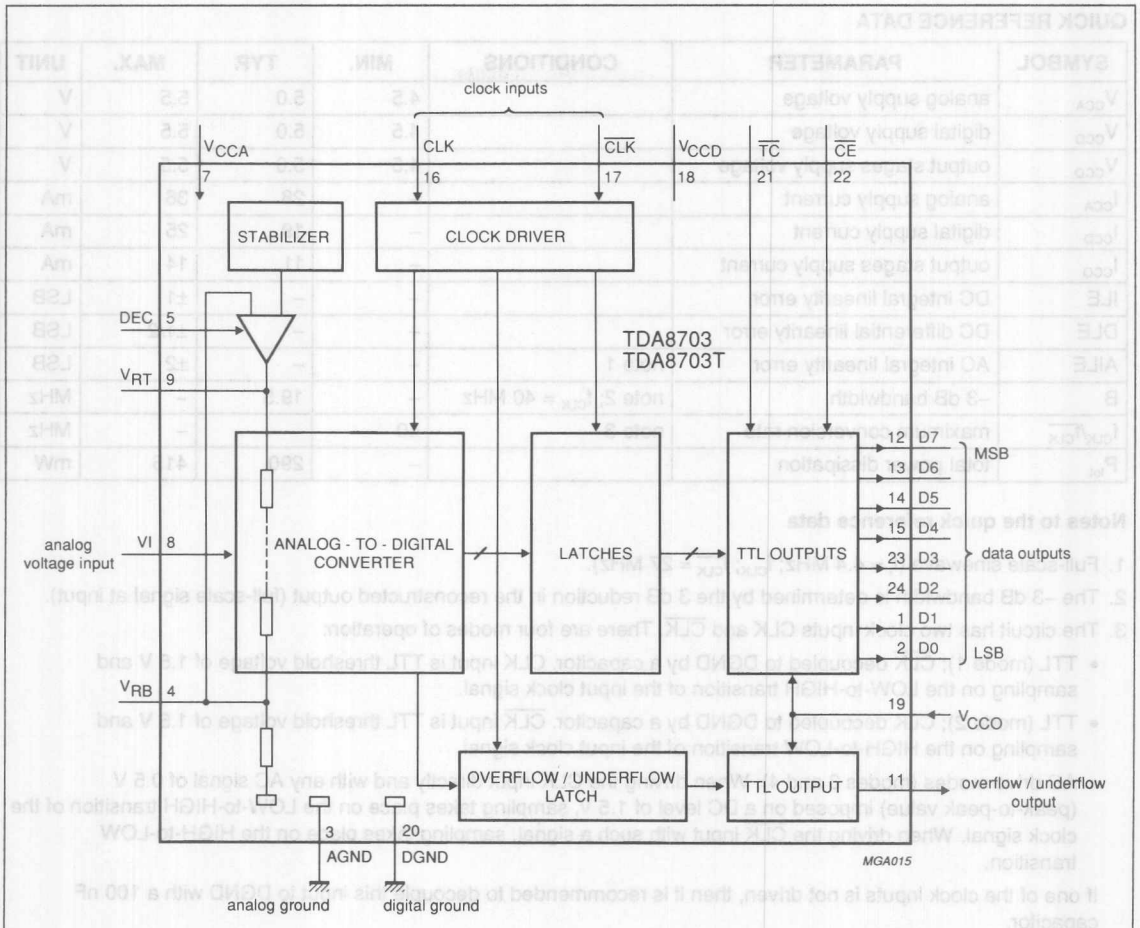


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter

TDA8703/8703T

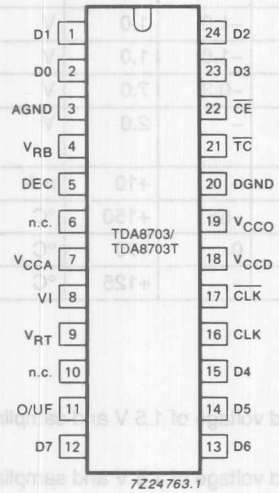


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
AGND	3	analog ground
V_{RB}	4	reference voltage bottom (decoupling)
DEC	5	decoupling input (internal stabilization loop decoupling)
n.c.	6	not connected
V_{CCA}	7	positive supply voltage for analog circuits (+5 V)
VI	8	analog voltage input
V_{RT}	9	reference voltage top (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output, bit 7 (MSB)
D6	13	data output, bit 6
D5	14	data output, bit 5
D4	15	data output, bit 4
CLK	16	clock input
$\overline{CLK}$	17	complementary clock input
V_{CCD}	18	positive supply voltage for digital circuits (+5 V)
V_{CCO}	19	positive supply voltage for output stages (+5 V)
DGND	20	digital ground
$\overline{TC}$	21	input for two's complement output (TTL level input, active LOW)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output, bit 3
D2	24	data output, bit 2

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range		−0.3	7.0	V
V_{CCD}	digital supply voltage range		−0.3	7.0	V
V_{CCO}	output stages supply voltage		−0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage differences		−1.0	1.0	V
V_{VI}	input voltage range	referenced to AGND	−0.3	7.0	V
$V_{CLK(p-p)}/V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)	see note; referenced to DGND	–	2.0	V
I_O	output current		–	+10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		0	+70	°C
T_j	junction temperature		–	+125	°C

Note to the limiting values

The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:

- TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
- TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
- AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air (SOT101)	55 K/W
$R_{th\ j-a}$	from junction to ambient in free air (SOT137A)	75 K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7 - V_3 = 4.5$ V to 5.5 V; $V_{CCD} = V_{18} - V_{20} = 4.5$ V to 5.5 V; $V_{CCO} = V_{19} - V_{20} = 4.5$ V to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; T_{amb} = 0 °C to +70 °C; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current		–	28	36	mA
I_{CCD}	digital supply current		–	19	25	mA
I_{CCO}	output stage supply current	all outputs LOW	–	11	14	mA
Inputs						
CLOCK INPUT $\overline{CLK}$ AND CLK (NOTE 1; REFERENCED TO DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V	–	–	100	µA
		$V_{CLK}/V_{\overline{CLK}} = V_{CCD}$	–	–	300	µA
Z_i	input impedance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	–	4	–	kΩ
C_i	input capacitance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	–	4.5	–	pF
$V_{CLK(p-p)} - V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)	note 1; DC level = 1.5 V	0.5	–	2.0	V
Inputs $\overline{TC}$ and $\overline{CE}$ (referenced to DGND)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_{IL} = 0.4$ V	–400	–	–	µA
I_{IH}	HIGH level input current	$V_{IH} = 2.7$ V	–	–	20	µA
VI (analog input voltage referenced to AGND)						
$V_{VI(B)}$	input voltage (bottom)		1.33	1.41	1.48	V
$V_{VI(0)}$	input voltage	output code = 0	1.455	1.55	1.635	V
$V_{OS(B)}$	offset voltage (bottom)	$V_{VI(0)} - V_{VI(B)}$	0.125	–	0.155	V
$V_{VI(T)}$	input voltage (top)		3.2	3.36	3.5	V
$V_{VI(255)}$	input voltage	output code = 255	3.115	3.26	3.385	V
$V_{OS(T)}$	offset voltage (top)	$V_{VI(T)} - V_{VI(255)}$	0.085	–	0.115	V
$V_{VI(p-p)}$	input voltage amplitude (peak-to-peak value)		1.66	1.71	1.75	V
I_{IL}	LOW level input current	$V_{VI} = 1.4$ V	–	0	–	µA
I_{IH}	HIGH level input current	$V_{VI} = 3.6$ V	60	120	180	µA

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VI (analog input voltage referenced to AGND)						
Z_i	input impedance	f_i = 1 MHz	–	10	–	kΩ
C_i	input capacitance	f_i = 1 MHz	–	14	–	pF
Reference resistance						
R_{ref}	reference resistance	V_{RT} to V_{RB}	–	220	–	Ω
Outputs						
DIGITAL OUTPUTS (D7 - D0) (REFERENCED TO DGND)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_O = –0.4 mA	2.7	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	µA
Switching characteristics (note 2; see Fig.3)						
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		40	–	–	MHz
Analog signal processing (f_{CLK} = 40 MHz)						
B	–3 dB bandwidth	note 3	–	19.5	–	MHz
G_d	differential gain	note 4	–	0.6	–	%
ϕ_d	differential phase	note 4	–	0.8	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz	–	–55	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	–28	–25	dB
SVRR2	supply voltage ripple rejection	note 5	–	1	2.5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
AILE	AC integral linearity error	note 6	–	–	±2	LSB
eff	effective bits	f_i = 4.43 MHz	–	7.1	–	bits
Timing (note 7; see Figs 3 to 6; f_{CLK} = 40 MHz)						
t_{dS}	sampling delay		–	–	2	ns
t_{HD}	output hold time		6	–	–	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	–	8	10	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	–	14	16	ns
t_{dZH}	3-state output delay times	enable-to-HIGH	–	19	25	ns
t_{dZL}	3-state output delay times	enable-to-LOW	–	16	20	ns
t_{dHZ}	3-state output delay times	disable-to-HIGH	–	14	20	ns
t_{dLZ}	3-state output delay times	disable-to-LOW	–	9	12	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

   If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.
2. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 2 ns.
3. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
4. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
5. Supply voltage ripple rejection:
   - SVRR1; variation of the input voltage producing output code 127 for supply voltage variation of 1 V: $SVRR1 = 20 \log (\Delta V_{VI(127)} / \Delta V_{CCA})$
   - SVRR2; relative variation of the full-scale range of analog input for a supply voltage variation of 1 V: $SVR2 = \{\Delta(V_{VI(0)} - V_{VI(255)}) / (V_{VI(0)} - V_{VI(255)})\} + \Delta V_{CCA}$.
6. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}; $f_{\overline{CLK}}$ = 27 MHz).
7. Output data acquisition:
   - Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
   - Output data is fully stable during the low level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; referenced to AGND)

			BINARY OUTPUT BITS								TWO's COMPLEMENT OUTPUT BITS							
STEP	$V_{VI(p-p)}$	O/UF	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow	< 1.55	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1.55	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
254	•	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	3.26	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow	> 3.26	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

Table 2 Mode selection

$\overline{TC}$	$\overline{CE}$	D7 - D0	O/UF
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

Where: X = don't care

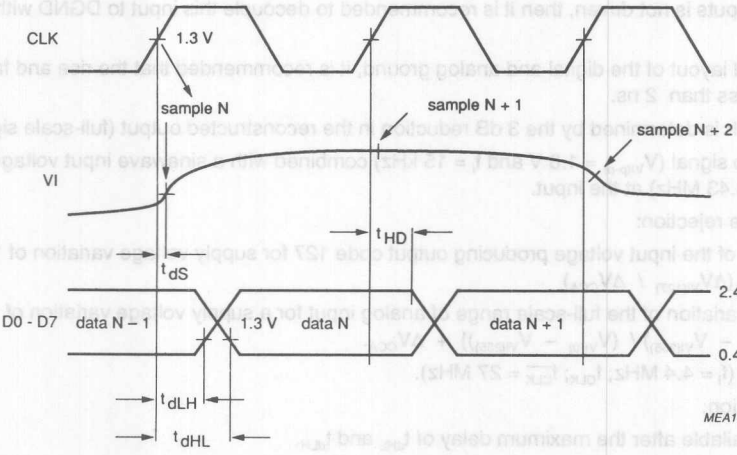


Fig.3 Timing diagram.

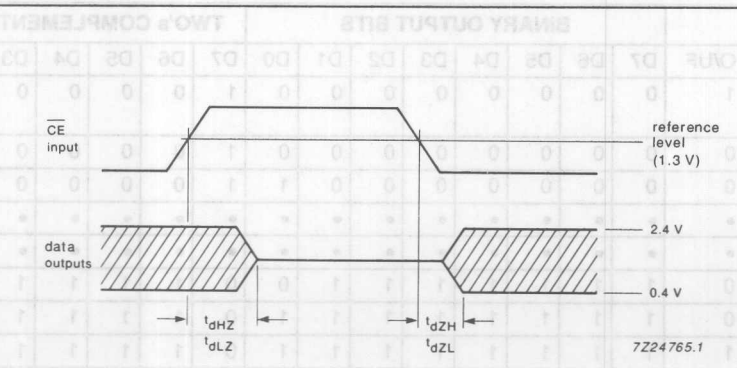


Fig.4 3-state delay timing diagram.

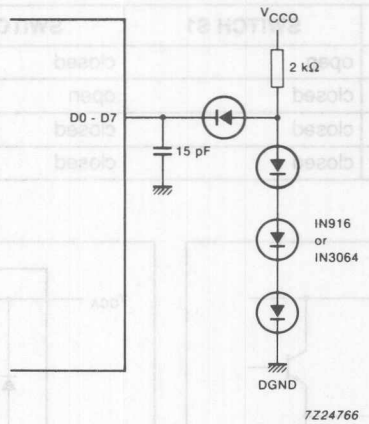


Fig.5 Load circuit for timing measurement; data outputs ($\overline{CE}$ = LOW).

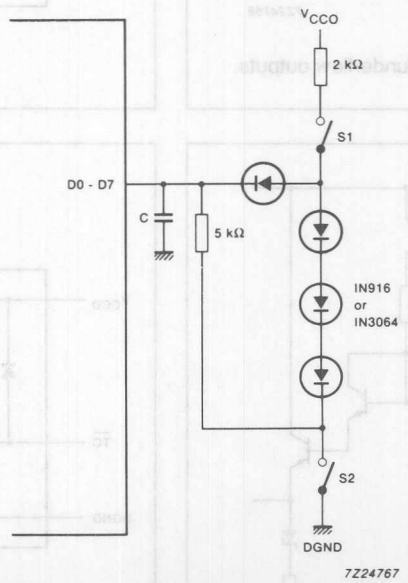


Fig.6 Load circuit for timing measurement; 3-state outputs ($\overline{CE}$: f_i = 1 MHz; V_{VI} = 3 V); see Table 3.

Table 3 Timing measurement for load circuit

TIMING MEASUREMENT	SWITCH S1	SWITCH S2	CAPACITOR
t_{dZH}	open	closed	15 pF
t_{dZL}	closed	open	15 pF
t_{dHZ}	closed	closed	5 pF
t_{dLZ}	closed	closed	5 pF

INTERNAL PIN CONFIGURATIONS

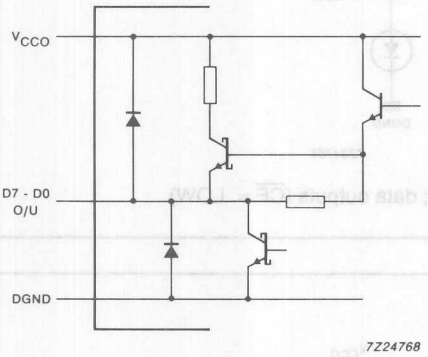


Fig.7 TTL data and overflow/underflow outputs.

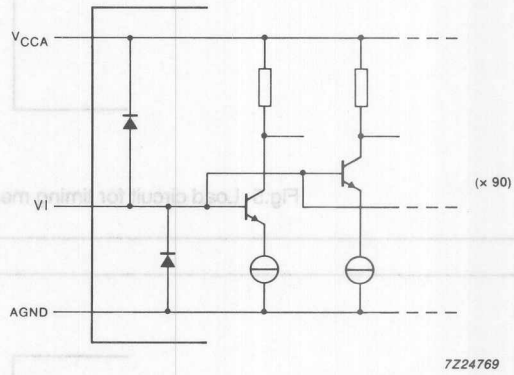


Fig.8 Analog inputs.

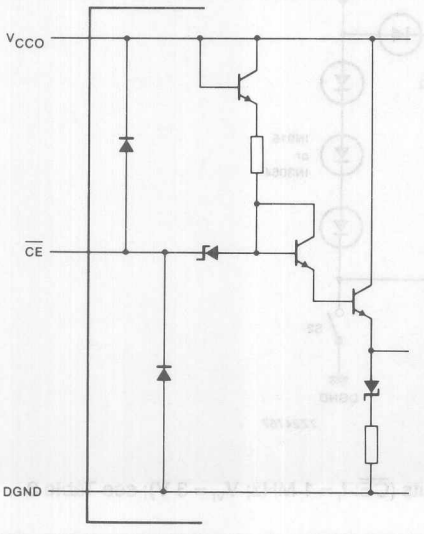


Fig.9 $\overline{CE}$ (3-state) input.

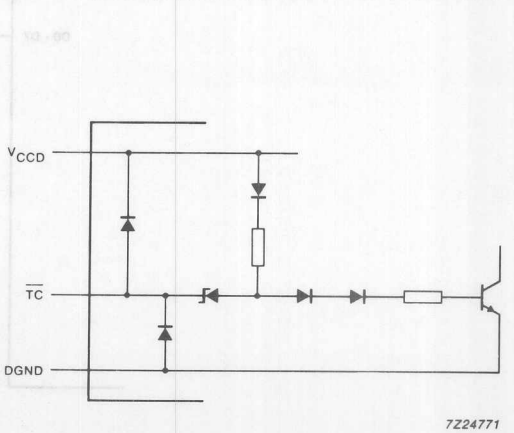


Fig.10 $\overline{TC}$ (two's complement) input.

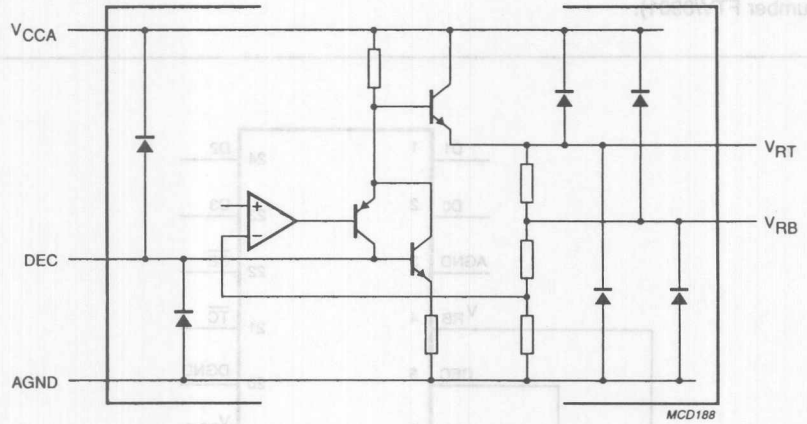


Fig.11 V_{RB}, V_{RT} and DEC.

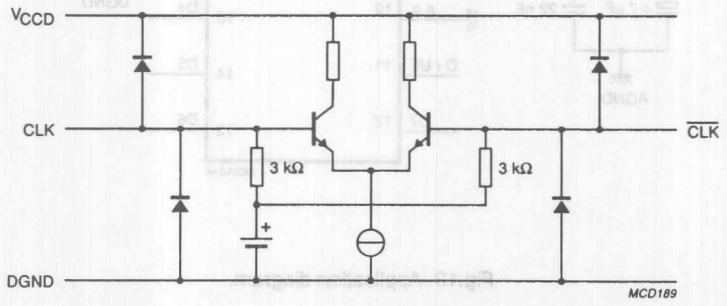


Fig.12 CLK and $\overline{CLK}$ inputs.

APPLICATION INFORMATION

Additional application information
will be supplied upon request
(please quote number FTV/8901).

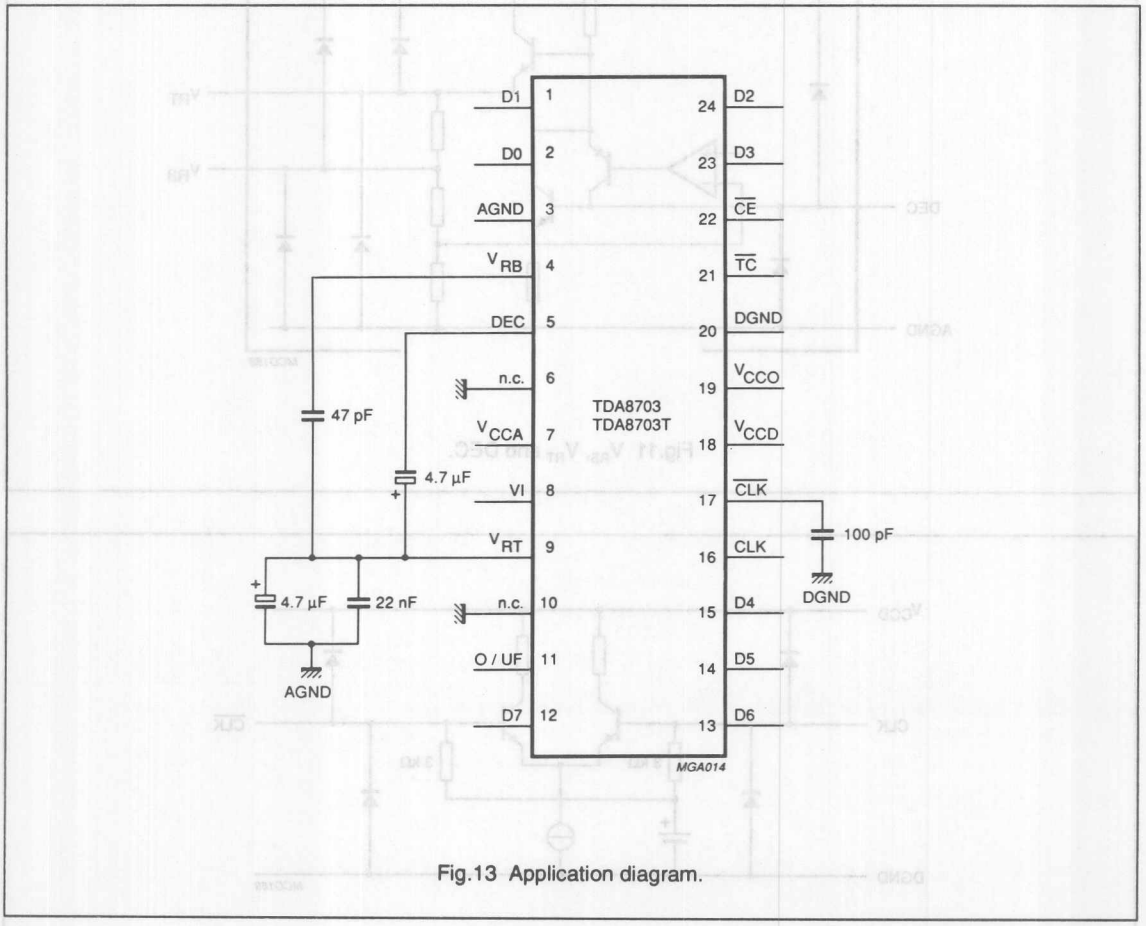


Fig.13 Application diagram.

Notes to Fig.13

1. CLK should be decoupled to the DGND with a 100 nF capacitor, if a TTL signal is used on CLK (see 'Notes to the characteristics', note 1).
2. CLK and $\overline{CLK}$ can be used in a differential mode (see 'Notes to the characteristics', note 1).
3. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder; do not draw current from these pins in order to achieve good linearity.
4. Analog and digital supplies should be separated and decoupled.
5. Pins 6 and 10 should be connected to AGND in order to prevent noise influence.

6-bit analog-to-digital converter with multiplexer and clamp

TDA8706

FEATURES

- 6-bit resolution
- Binary 3-state TTL outputs
- TTL compatible digital inputs
- 3 multiplexed video inputs
- Luminance and colour difference clamps
- Internal reference
- 300 mW power dissipation
- 20-pin plastic package

APPLICATIONS

- General purpose video applications
- Y, U and V signals
- Colour Picture-in-Picture (PIPCO) for TV
- Videophone
- Frame grabber

GENERAL DESCRIPTION

The TDA8706 is a monolithic bipolar 6-bit analog-to-digital converter (ADC) with a 3 analog input multiplexer and a clamp. All digital inputs and outputs are TTL compatible. Regulator with good temperature compensation.

FUNCTIONAL DESCRIPTION

The TDA8706 is a "like-flash" converter which produces an output code in one clock period. The device can withstand a duty clock cycle of 50 to 66.6% (clock HIGH).
Luminance clamping level is fitted with 00 hex. code (output 000000).
Chrominance clamping level is fitted with 20 Hex. code (output 100000).

QUICK REFERENCE DATA

Measured over full voltage and temperature ranges

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage (pin 2)		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage (pin 10)		4.5	5.0	5.5	V
I_{CCA}	analog supply current (pin 20)		–	32	39	mA
I_{CCD}	digital supply current (pin 10)		–	28	37	mA
ILE	integral linearity error		–	–	±0.75	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
f_{CLK}	maximum clock frequency		20	–	–	MHz
P_{tot}	total power dissipation		–	300	418	mW
T_{amb}	operating ambient temperature range		0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8706	20	DIL	plastic	SOT146EF4
TDA8706T	20	SO20L	plastic	SOT163AG7

6-bit analog-to-digital converter with multiplexer and clamp

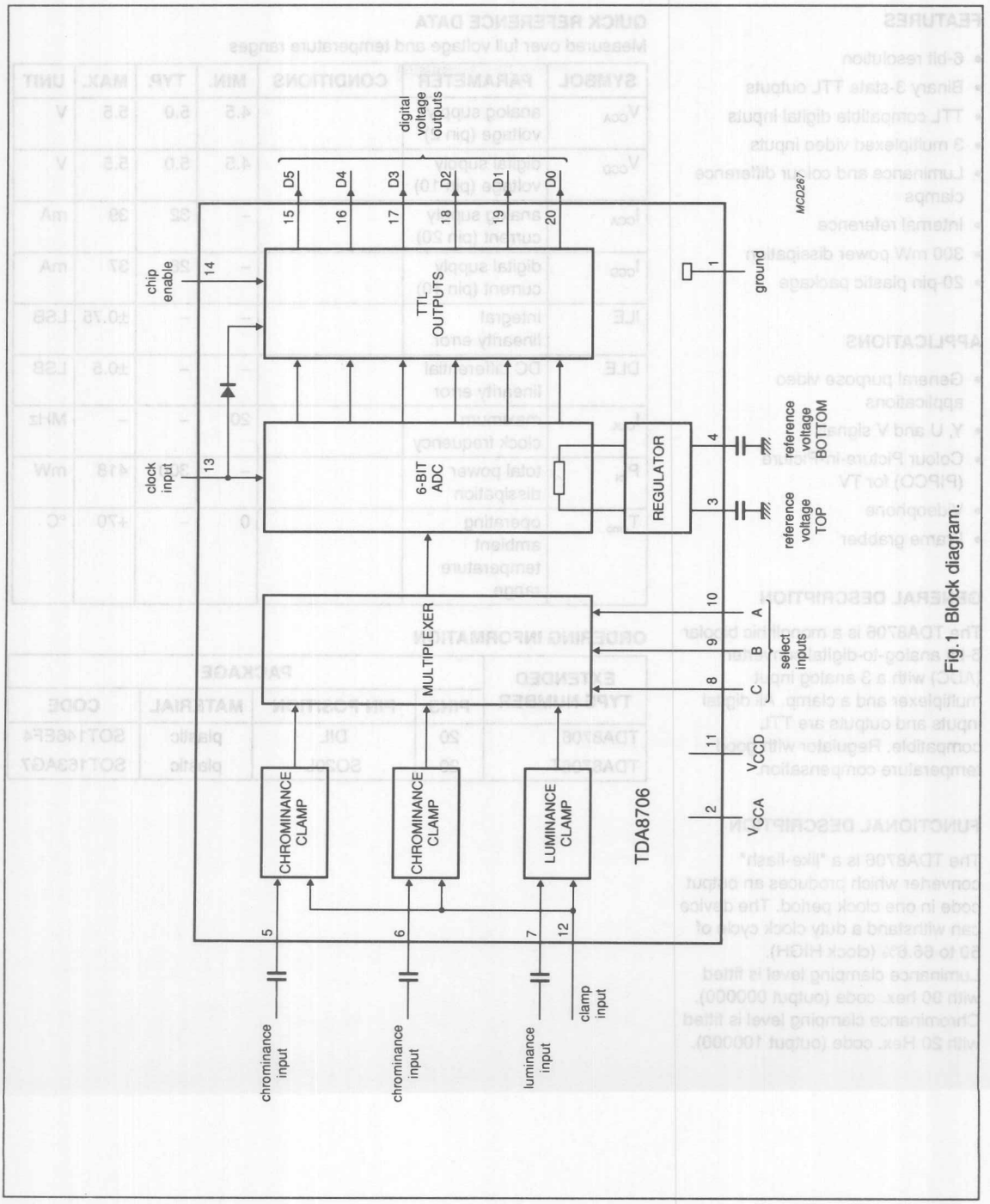


Fig. 1 Block diagram.

6-bit analog-to-digital converter with multiplexer and clamp

TDA8706



Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1	ground
V_{CCA}	2	analog positive supply (+5 V)
V_{RT}	3	reference voltage TOP decoupling
V_{RB}	4	reference voltage BOTTOM decoupling
INC	5	chrominance input
INB	6	chrominance input
INA	7	luminance input
C	8	select input
B	9	select input
A	10	select input
V_{CCD}	11	digital positive supply voltage (+5 V)
CLAMP	12	clamp pulse input (positive pulse)
CLK	13	clock input
$\overline{CE}$	14	chip enable (active LOW)
D5	15	digital voltage output: most significant bit (MSB)
D4	16	digital voltage output
D3	17	digital voltage output
D2	18	digital voltage output
D1	19	digital voltage output
D0	20	digital voltage input: least significant bit (LSB)

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range (pin 2)	−0.3	7.0	V
V_{CCD}	digital supply voltage range (pin 10)	−0.3	7.0	V
V_{CCA}-V_{CCD}	supply voltage difference	1.0	–	V
V_I	input voltage range	−0.3	7.0	V
I_O	output current	–	10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C

CHARACTERISTICS (see Tables 1 and 2)

V_{CCA} = 4.5 V to 5.5 V; V_{CCD} = 4.5 V to 5.5 V = V_{CCD}; T_{amb} = 0 °C to +70°C; C_{VRB} = C_{VR1} = 100 nF; Typical values measured at V_{CCA} = V_{CCD} = 5 V and T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage (pin 2)		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage (pin 10)		4.5	5.0	5.5	V
I_{CCA}	analog supply current (pin 2)		–	32	39	mA
I_{CCD}	digital supply current (pin 10)	all outputs at LOW level	–	28	37	mA
Inputs						
CLOCK INPUT (PIN 13)						
V_{IL}	LOW level input voltage		0	-	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	100	µA
Z_I	input impedance	f_{CLK} = 20 MHz	–	4	–	kΩ
C_i	input capacitance	f_{CLK} = 20 MHz	–	2	–	pF
A, B, C, CLAMP AND CEN INPUTS (PINS 8, 9, 10, 12 AND 14)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{CLK} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{CLK} = 2.7 V	–	–	20	µA
Reference voltage (pins 3 and 4)						
V_{RT}	reference voltage TOP decoupling		3.22	3.35	3.44	V
V_{RB}	reference voltage BOTTOM decoupling		1.84	1.9	1.96	V
$V_{RT} - V_{RB}$	reference voltage TOP – BOTTOM decoupling		1.36	1.435	1.48	V
Analog inputs INA, INB, INC (pins 7, 6 and 5)						
$V_{I(p-p)}$	input voltage amplitude (peak-to-peak value)		840	900	940	mV
Z_I	input impedance	f_i = 4.43 MHz	100	–	–	kΩ
C_{clamp}	coupling clamp capacitance		1	10	1000	nF
Analog signal processing (pins 5, 6 and 7) (f_{CLK} = 20 MHz)						
f_1	fundamental harmonics (full scale)	f_i = 4.43 MHz	–	–	0	dB
f_{all}	harmonics (full scale); all components	f_i = 4.43 MHz	-	–45	-	dB
G_{diff}	differential gain	note 1	–	0.4	–	%
ϕ_{diff}	differential phase	note 1	–	1.0	–	deg
SVRR	supply voltage ripple rejection	note 2	–	–30	–	dB
Outputs						
DIGITAL VOLTAGE OUTPUTS (PINS 15 TO 20) (SEE TABLE 2)						
V_{OL}	LOW level output voltage	I_O = 1 mA	0	–	0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OH}	HIGH level ouptut voltage	I_O = 0.5 mA	2.7	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	–	20	µA
Switching characteristics						
CLOCK TIMING (SEE FIG.3)						
f_{CLK}	maximum clock frequency		20	–	–	MHz
f_{mux}	maximum multiplexing frequency		10	–	–	MHz
t_{CLK}	period		50	–	–	ns
	duty cycle	CLK = V_{IH}	45	50	66.6	%
t_{LOW}	LOW time	at 50%	16	–	–	ns
t_{HIGH}	HIGH time	at 50%	22.5	–	–	ns
t_{CLR}	rise time	at 10% to 90%	4	6	–	ns
t_{CLF}	fall time	at 90% to 10%	4	6	–	ns
Select signals, Clamp, Data (see Figs 4 and 5)						
t_S	set-up time select A, B and C		35	–	–	ns
t_r	rise time (A, B and C)	at 10% to 90%	4	6	–	ns
t_f	fall time (A, B and C)	at 90% to 10%	4	6	–	ns
t_{CLPS}	set-up time clamp asynchronous		0	–	–	
t_{CLPH}	hold time clamp asynchronous		0	–	–	
t_{CLPP}	clamp pulse	C_{CLP} = 10 nF	–	3	–	µs
t_d	data output delay time		–	15	24	ns
t_{DH}	data hold time		12	–	–	ns
Transfer function						
ILE	DC integral linearity error		–	–	±0.75	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
AILE	AC integral linearity error	note 3	–	–	±2	LSB
EB	effective bits	note 3	–	5.7	–	bits
Timing						
DIGITAL OUTPUTS						
T_{dl}	3-state delay time	see Fig.6	–	16	25	ns
T_{sto}	sampling time offset		–	2	–	ns

Notes to the characteristics

1. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V and f_i = 4.43 MHz) at the input.
2. Supply voltage ripple rejection (SVRR): variation of the input voltage produces output code 31 for a supply voltage variation of 1 V.

$$SVRR = 20 \log \frac{\Delta V_{VI(31)}}{\Delta V_{CCA}}$$

3. Full-scale sinewave; f_i = 4.43 MHz, f_{CLK} = 20 MHz.

Table 1 Output coding

STEP	V_I (note 1) (TYP. value)	BINARY OUTPUTS D5 to D0
Underflow	< 2.2 V	000000
0	2.2 V	000000
1	2.215 V	000001
.		.....
.		.....
.		.....
62	3.072 V	111110
63	3.086 V	111111
Overflow	> 3.1 V	111111

Note

1. With clamping capacitance.

Table 2 Mode selection

CEN	D0 to D5
1	high impedance
0	active. Binary

Table 3 Clamp input A

A	CLAMP	DIGITAL OUTPUTS	$V_{in}A$
0	1	X	2.2
1	1	0	2.2

Note

X = don't care.

Table 4 Clamp input B and C

B/C	CLAMP	DIGITAL OUTPUTS	$V_{in}B/V_{in}C$
0	1	X	2.65
1	1	32	2.65

Note

X = don't care.

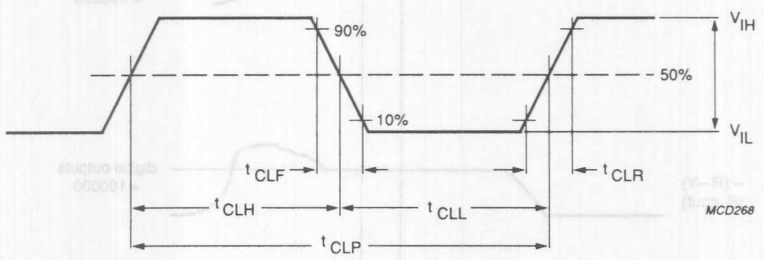


Fig.3 AC clock characteristics.

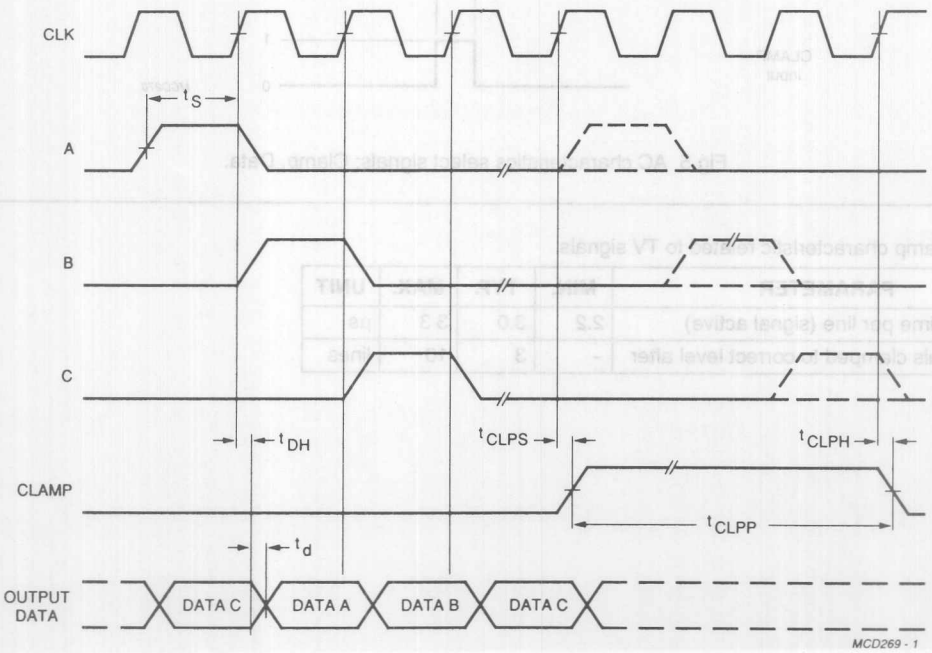


Fig.4 AC characteristics select signals; Clamp, Data.

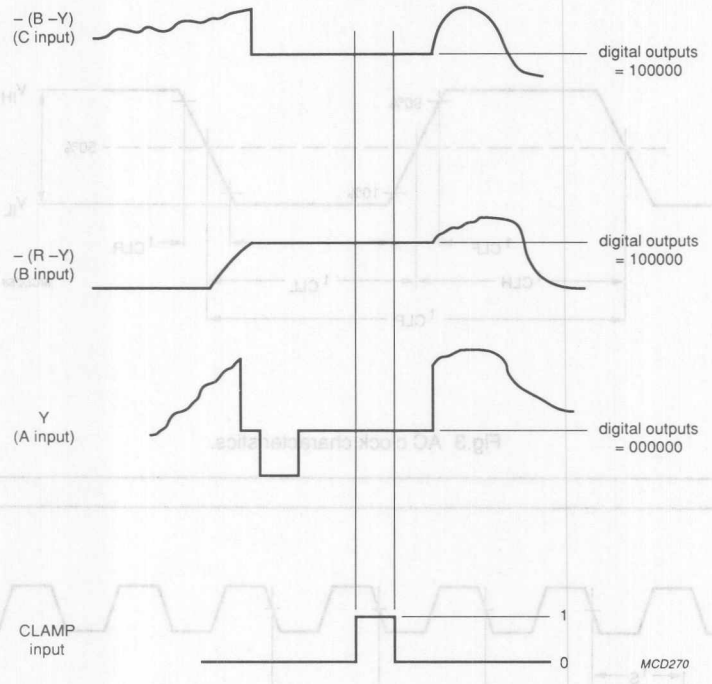


Fig.5 AC characteristics select signals; Clamp, Data.

Table 5 Clamp characteristic related to TV signals

PARAMETER	MIN.	TYP.	MAX.	UNIT
clamping time per line (signal active)	2.2	3.0	3.3	µs
input signals clamped to correct level after	–	3	10	lines

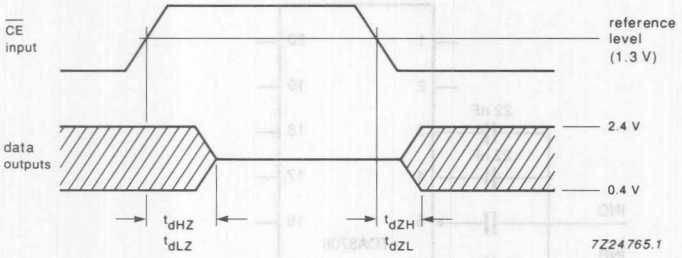


Fig.6 Timing diagram of 3-state delay.

Application information

Additional application information will be supplied on request (please quote reference number FTV/9112).

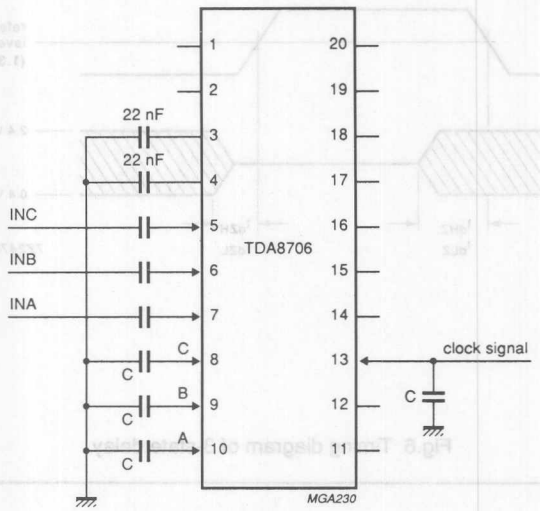


Fig.7 Application diagram.

Notes to figure 7

1. 'C' capacitors must be determined on the output capacitance of the circuits driving A, B and C or CLK pins
2. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder. Do not draw current from these pins in order to achieve good linearity
3. Analog and digital supplies should be separated and decoupled.

14-bit analog-to-digital converter — TDA1534

An integrated 14-bit analogue to digital converter (ADC) which uses the successive approximation conversion technique and includes the comparator, reference source and clock on the same chip.
The high linearity makes it very suitable for signal processing while the accurate, temperature-compensated reference source makes it applicable for instrumentation purposes.
The ADC accepts unipolar or bipolar input signals.
Digital output data is in serial form.
All digital outputs are fully TTL compatible.

QUICK REFERENCE DATA

Positive supply voltage (pin 5)	V_P	typ.	5	V
Negative supplu voltage 1 (pin 6)	$-V_{N1}$	typ.	5	V
Negative supply voltage 2 (pin 9)	$-V_{N2}$	typ.	17	V
Signal-to-noise ratio	S/N	typ.	84	dB
Linearity error		typ.	± ½	LSB
Total power dissipation	P_{tot}	typ.	500	mW
Operating ambient temperature range	T_{amb}	−20 to + 70		°C
Storage temperature range	T_{stg}	−55 to + 150		°C
Resolution			14	bits
Full scale input current	I_{FS}	typ.	4	mA

14-bit analog-to-digital converter TDA1534

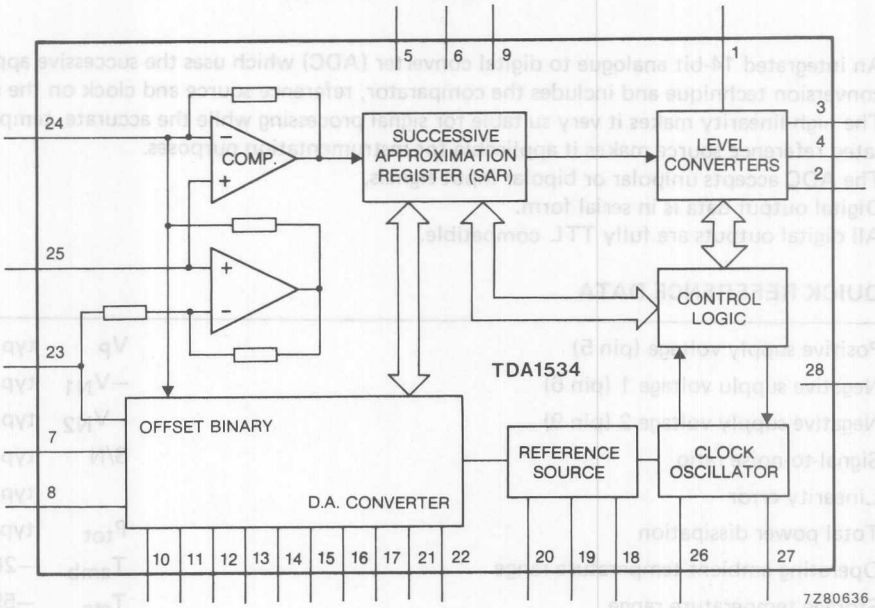


Fig. 1 Block diagram.

PIN DESIGNATION

1	start conversion
2	status out
3	data out
4	data strobe
5	positive supply voltage
6	negative supply voltage 1
7	oscillator input
8	oscillator input
9	negative supply voltage 2
10, 11, 12, 13, 14	decoupling binary weighted current sources
15, 16, 17	decoupling binary weighted current sources
18	I_{ref1}
19	I_{ref2}
20	I_{ref3}
21, 22	decoupling binary weighted current sources
23	offset binary input
24	analogue signal input
25	analogue ground
26	oscillator
27	oscillator
28	digital ground

FUNCTIONAL DESCRIPTION

The circuit consists of the following parts:

14-bit D/A converter

Using "dynamic element matching", which results in high accuracy, linearity and longterm stability, without the need of trimming. The main parts of the DAC are the binary wieghted current sources and the bit switches. The DAC also delivers an offset binary current for bipolar operation of the ADC.

Fast settling comparator/substractor

Consisting of a high speed, clamped operational amplifier with special frequency compensation system.

Successive approximation register (SAR)

This register is an array of fourteen addressable latches, with the outputs connected to the bit switches of the D/A converter.

Logic-level converters

Converting the internally used current-mode-logic (CML) levels to TTL levels, for easy interface of the ADC with standard logic families.

Clock oscillator and control logic

Delivering the pulses and timing for the SAR and takes care of the communication with the peripheral circuits.

Reference source

Based on the bandgap voltage of silicon, with extra temperature compensation circuit.

For the timing of the output signals see Fig. 3. At the leading edge of the start conversion (SC) pulse the ADC starts converting the input voltage. During the conversion cycle the following signals appear at the output pins:

Status (pin 2)

This signal can be used to force the Sample-Hold-Circuit, in front of the ADC, in hold mode.

Data strobe (pin 4)

This signal is used to clock the data-out signal into the peripheral devices.

Data out (pin 3)

The 14 bits serial, binary, output code of the A/D converter starting with the most significant bit (MSB). The data must be considered valid at the trailing edge of the data-strobe signal.

14-bit analog-to-digital converter | TDA1534

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Positive supply (pin 5)	V_P	0 to 7 V
Negative supply voltage (pin 6)	$-V_{N1}$	0 to 7 V
Negative supply voltage (pin 9)	$-V_{N2}$	0 to 20 V
Storage temperature	T_{stg}	−55 to + 150 °C
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Total power dissipation	P_{tot}	derating curve (Fig. 2)

CHARACTERISTICS (see application circuit Fig. 4)

V_P = 5 V; $-V_{N1}$ = 5 V; $-V_{N2}$ = 17 V; T_{amb} = + 25 °C, unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Positive supply voltage (pin 5)	V_P	4	5	6	V
Negative supply voltage 1 (pin 6)	$-V_{N1}$	–	5	–	V
Negative supply voltage 2 (pin 9)	$-V_{N2}$	16,5	17	18	V
Positive supply current	I_P	–	30	40	mA
Negative supply current	$-I_{N1}$	–	37	45	mA
Negative supply current	$-I_{N2}$	–	10	13	mA
Total power dissipation	P_{tot}	–	500	–	mW
Resolution		–	14	–	bits
Analogue input					
Full scale input current offset-binary current switched off	I_{FS}	3,8	4,0	4,2	mA
Temperature coefficient pin 23 short-circuited	TC	–	t.b.f.	–	10^{-6}/K
Zero-offset offset-binary current switched off					
Offset voltage	$-V_o$	10	20	30	mV
Temperature coefficient	TC	–	t.b.f.	–	μV/K
Offset current	I_o	–	500	–	nA
Temperature coefficient	TC	–	t.b.f.	–	nA/K
Linearity					
Linearity error		–	± ¼	–	LSB
Linearity from −20 to + 70 °C		–	± ½	–	LSB
Offset binary current	I_{BO}	$0{,}45 \cdot I_{FS}$	$0{,}50 \cdot I_{FS}$	$0{,}55 \cdot I_{FS}$	mA
Temperature coefficient	TC	–	t.b.f.	–	10^{-6}/K
Signal to noise ratio*	S/N	80	84	–	dB

parameter	symbol	min.	typ.	max.	unit
Start conversion (pin 1)					
Input current					
V_{IL} (< 0,8 V)	$-I_1$	–	–	1,6	mA
V_{IH} (> 2,0 V)	I_1	–	–	40	μA
Data, strobe, status (pins 3, 4 and 2)					
Output current					
V_{OL} (< 0,6 V)	$I_{3, 4, 2}$	6,4	16	–	mA
V_{OH} (> 2,4 V)	$-I_{3, 4, 2}$	160	400	–	μA
Conversion time					
$C_{26\text{-}27}$ = 220 pF ± 1%	t_C	–	8,5	–	μs
Signal width (pin 1)					
start conversion	t_{SC}	0,2	–	t_C	μs
Delay time (pin 2)					
status out	t_{SD}	–	60	–	ns
Set-up time (pin 3)					
data out	t_{DS}	–	25	–	ns
Pulse duration (pin 4)					
data strobe high	t_{DSH}	–	125	–	ns

* Signal-to-noise ratio within 10 Hz and 20 kHz bandwidth of a 1 kHz full scale sinewave, generated at a sample rate of 44 kHz.

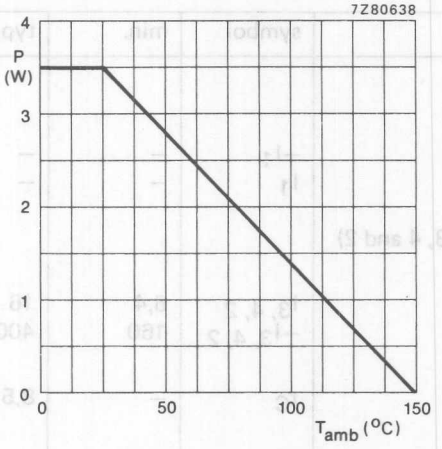


Fig. 2 Power derating curve.

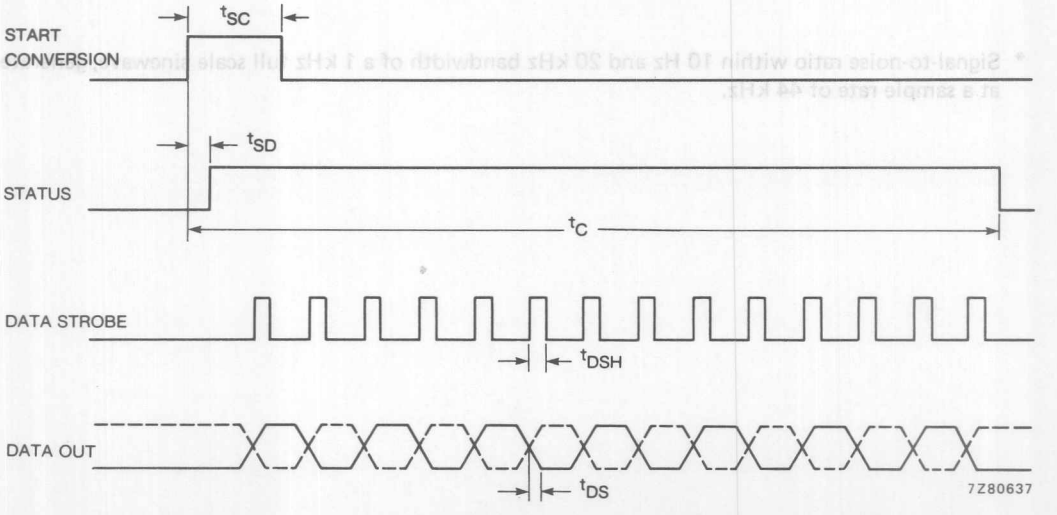


Fig. 3 Switching times waveforms.

14-bit analog-to-digital converter TDA1534

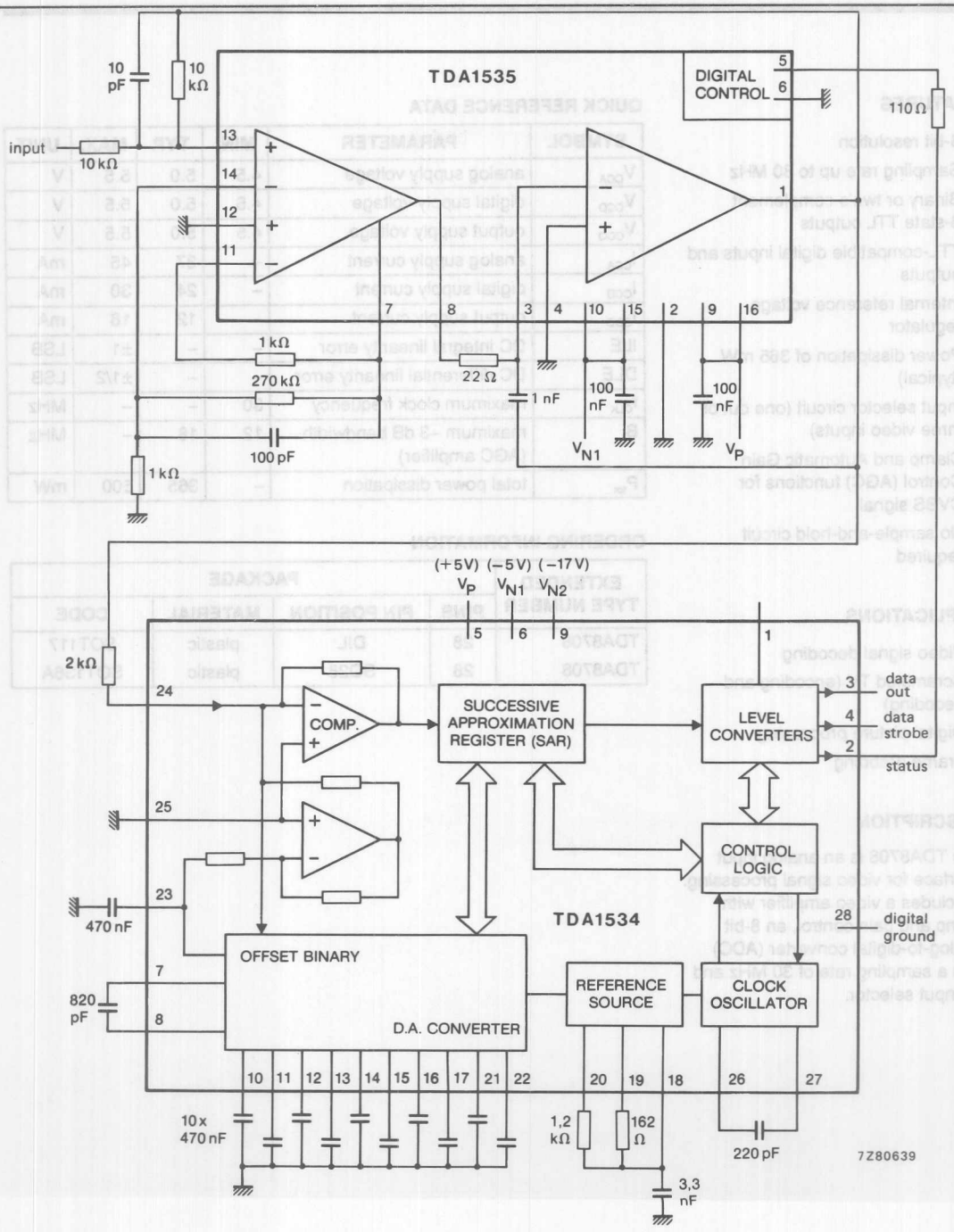


Fig. 4 Application and test circuit.

All earthed components connected to analogue ground (pin 25).

Video analog interface for composite luminance TDA8708

FEATURES

- 8-bit resolution
- Sampling rate up to 30 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS signal
- No sample-and-hold circuit required

APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing

DESCRIPTION

The TDA8708 is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 30 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	output supply voltage	4.5	5.0	5.5	V
I_{CCA}	analog supply current	–	37	45	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±1/2	LSB
f_{CLK}	maximum clock frequency	30	–	–	MHz
B	maximum –3 dB bandwidth (AGC amplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	365	500	mW

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8708	28	DIL	plastic	SOT117
TDA8708	28	SO28	plastic	SOT136A

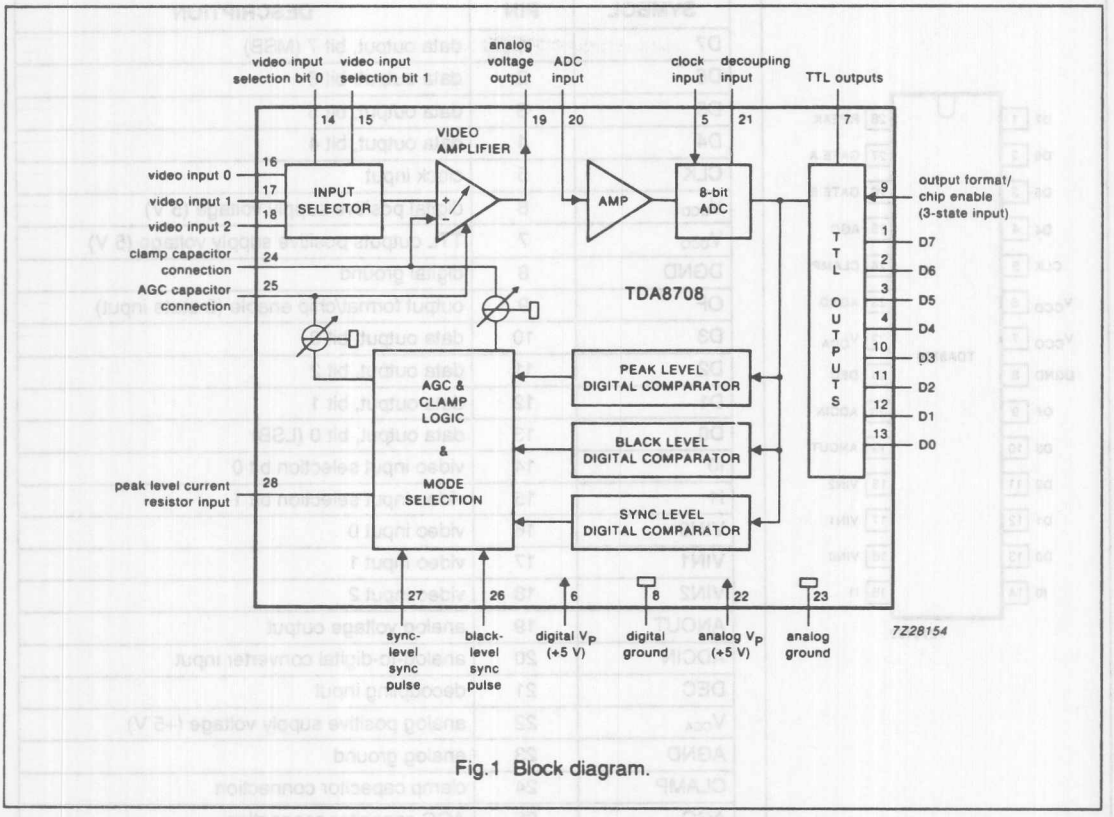


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

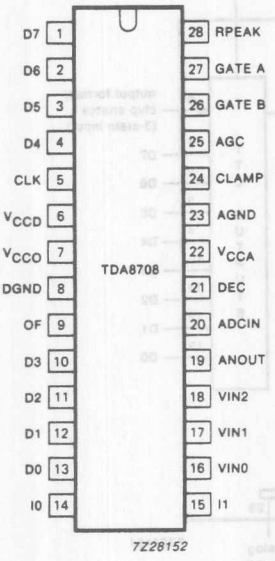


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output, bit 7 (MSB)
D6	2	data output, bit 6
D5	3	data output, bit 5
D4	4	data output, bit 4
CLK	5	clock input
V_{CCD}	6	digital positive supply voltage (5 V)
V_{CCO}	7	TTL outputs positive supply voltage (5 V)
DGND	8	digital ground
OF	9	output format/chip enable (3-state input)
D3	10	data output, bit 3
D2	11	data output, bit 2
D1	12	data output, bit 1
D0	13	data output, bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog positive supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
AGC	25	AGC capacitor connection
GATE B	26	black level synchronization pulse
GATE A	27	sync level synchronization pulse
RPEAK	28	peak level current resistor input

The TDA8708 provides a simple interface for decoding video signals.

The TDA8708 operates in configuration mode 1 (see Fig.4) when the video signals are weak (i.e. when the gain of the AGC amplifier has not yet reached its optimum value). This enables a fast recovery of the synchronization pulses in the decoder circuit. When the pulses at the GATE A and GATE B inputs become distinct (GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively) the TDA8708 automatically switches to configuration mode 2.

When the TDA8708 is in configuration mode 1, the gain of the AGC amplifier will be roughly adjusted (sync level to a digital output level of 0 and the peak level to a digital output level of 255).

In configuration mode 2 the digital output of the ADC is compared to internal digital reference levels. The resultant outputs control the charge or discharge current of a capacitor connected to the AGC pin. The voltage across this capacitor controls the gain of the video amplifier. This is the gain control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that the sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 0 at the converter output. As the black level is at digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The peak-white control loop is always active. If the video signal tends to exceed the digital code of 240, the gain will be limited to avoid any over-range of the converter.

The use of nominal signals will prevent the output from exceeding a digital code of 213 and the peak-white control loop will be non-active.

The clamp level control is accomplished by using the same techniques as used for the gain control. The black-level digital comparator is active during a positive-going pulse at the GATE B input. The clamp capacitor will be charged or discharged to adjust the digital output to code 64.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	+7.0	V
V_{CCD}	digital supply voltage range	−0.3	+7.0	V
V_{CCO}	output supply voltage range	−0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage difference	−1.0	+1.0	V
$V_{CCO} - V_{CCD}$	supply voltage difference	−1.0	+1.0	V
$V_{CCA} - V_{CCO}$	supply voltage difference	−1.0	+1.0	V
V_I	input voltage range	−0.3	V_{CCA}	V
I_O	output current	0	+10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
T_j	junction temperature	125	–	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT117)	55	-	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT136A)	70	-	K/W

CHARACTERISTICS

$V_{CCA} = V_{22} - V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6 - V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7 - V_8 = 4.5$ to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ to +0.5 V; $V_{CCA} - V_{CCO} = -0.5$ to +0.5 V; $T_{amb} = 0$ to +70 °C; Typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current		–	37	45	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	output supply current		–	12	16	mA
Video amplifier inputs						
VIN(0-2) INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)		0.45	1.0	1.6	V
$\|Z_I\|$	input impedance	f = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	input voltage LOW		0	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	input current HIGH	$V_I = 2.7$ V	–	–	20	µA
GATE A AND GATE B TTL INPUTS (SEE FIGS 4 AND 5)						
V_{IL}	input voltage LOW		0	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	–400	–	–	µA
I_{IH}	input current HIGH	$V_I = 2.7$ V	–	–	20	µA
RPEAK INPUT (PIN 28)						
I_{28}	minimum peak level current	$R_{28} = 0$ Ω	–	80	150	µA
AGC INPUT (PIN 25)						
V_{25}	AGC voltage for minimum gain		–	2.8	–	V
V_{25}	AGC voltage for maximum gain		–	4.0	–	V
	AGC output current	see Table 2	–	–	–	
CLAMP INPUT (PIN 24)						
V_{24}	CLAMP voltage for code 128 output		–	3.5	–	V
I_{24}	CLAMP output current	see Table 3	–	–	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	output AC voltage (peak-to-peak value)	V_{VIN} = 1 $V_{(p-p)}$; V_{25} = 3.6 V	–	V_{CCA} –2.95	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	V_{ANOUT} = 1 $V_{(p-p)}$; note 1	-	-	1.0	mA
V_{19}	output DC voltage for black level	note 2	–	V_{CCA} –2.95	–	V
Z_{19}	output impedance		–	20	–	Ω
Video amplifier dynamic characteristics						
α	crosstalk between VIN inputs		–	–60	–55	dB
G_d	differential gain	V_{VIN} = 1 $V_{(p-p)}$; V_{25} = 3.6 V	–	2	–	%
ϕ_d	differential phase		–	2	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 3	60	–	–	dB
SVRR	supply voltage ripple rejection	note 4	–	45	–	dB
ΔG	gain range		–4.5	–	6.0	dB
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	input voltage LOW		0	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{CCD}	V
I_{IL}	input current LOW	V_{CLK} = 0.4 V	–400	–	–	μA
I_{IH}	input current HIGH	V_{CLK} = 2.7 V	–	–	100	μA
$\|Z_i\|$	input impedance	f_{CLK} = 10 MHz	–	4	–	kΩ
C_i	input capacitance	f_{CLK} = 10 MHz	–	4.5	–	pF
OF input (3-state) (see Table 4)						
V_{IL}	input voltage LOW		0	–	0.2	V
V_{IH}	input voltage HIGH		2.6	–	V_{CCD}	V
V_9	input voltage in HIGH-Z state		–	1.15	–	V
I_{IL}	input current LOW		–370	–300	–	μA
I_{IH}	input current HIGH		–	360	450	μA
ADCIN INPUT (PIN 20) (SEE TABLE 5)						
V_{20}	input voltage	digital out = 00	–	V_{CCA} –1.6	–	V
V_{20}	input voltage	digital out = 255	–	V_{CCA} –1.1	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	0.5	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f = 6 MHz	–	50	–	MΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN INPUT (PIN 20) (SEE TABLE 5)						
C_I	input capacitance	f = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D(0-7)						
V_L	output voltage LOW	I_O = 2 mA	0	–	0.6	V
V_{OH}	output voltage HIGH	I_O = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	µA
Switching characteristics						
f_{CLK}	CLK input maximum frequency	see Fig.6; note 5	30	–	–	MHz
Analog signal processing (f_{CLK} = 30 MHz)						
G_d	differential gain	V_{VIN} = 1 $V_{(p-p)}$; note 6; Fig.3	–	2	–	%
ϕ_d	differential phase	note 6; Fig.3	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 6	–	–	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43MHz; note 6	–	–55	–	dB
SVRR	supply voltage ripple rejection	note 7	–	1	5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 8	–	–	±2	LSB
Timing (f_{CLK} = 30 MHz) (see Fig.6)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA)						
t_{dS}	sampling delay		–	2	–	ns
t_{HD}	output hold time		6	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time - output enable	see Fig.7	–	19	25	ns
t_{dDZ}	3-state delay time - output disable	see Fig.7	–	14	20	ns

Notes to the characteristics

1. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referred to V_{CC} and defined as:

   AC impedance ≥ 1 kΩ and the DC impedance > 2.7 kΩ.

   The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
2. Control mode 2 is selected.

Notes to the characteristics

3. Signal-to-noise ratio measured with 5 MHz bandwidth

$$SN = 20 \log \frac{V_{ANNOUT}\,(p\text{-}p)}{V_{ANNOUT}\ noise\ RMS\ (B = 5\ MHz)}$$

4. The voltage ratio is expressed as:

$$SVRR = 20 \log \frac{\Delta V_{CCA}}{\Delta G/G}$$

for V_i = 1 V (peak-to-peak), 100 kHz gain = 1 and 1 V supply variation.

5. It is recommended that the rise and fall times of the clock are not less than 2 ns. In addition, a 'good lay-out' for the digital and analog grounds is recommended.
6. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
7. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

$$SVRR = \frac{\Delta[V_{IN(00)} - V_{IN(FF)}] + [V_{IN(00)} - V_{IN(FF)}]}{\Delta V_{CCA}}$$

8. Full-scale sinewave (f_i = 4.4 MHz; f_{CLK}, $\overline{f_{CLK}}$ = 27 MHz).

Table 1 Video input selection (CVBS)

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 2 AGC output current

GATE A	GATE B	DIGITAL OUTPUT	I_{AGC}	MODE
1	1	output < 255 output > 255	−2.5 µA I_{PEAK}	1
0	X	output < 240 output > 240	0 I_{PEAK}	2
1	0	output < 0 0 < output < 240 output > 240	+2.5 µA −2.5 µA I_{PEAK}	2

Note

Where; X = don't care

Table 3 CLAMP output current

GATE A	GATE B	DIGITAL OUTPUT	I_{CLAMP}	MODE
1	1	output < 0 output > 0	I_{PEAK} −2.5 µA	1
X	0	X	0	2
0	1	output < 64 64 < output	+50 µA −50 µA	2

Note

Where; X = don't care

Table 4 OF input coding

OF	D0 TO D7
0	active, two's complement
1	high impedance
open (see note)	active, binary

Note

Use C ≥ 10 pF to DGND

Table 5 ADC output current

		BINARY OUTPUTS								TWO'S COMPLEMENT							
STEP	V_{ADCIN}	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} - 1.6 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1		0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
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.		.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254		1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} - 1.1 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow		1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

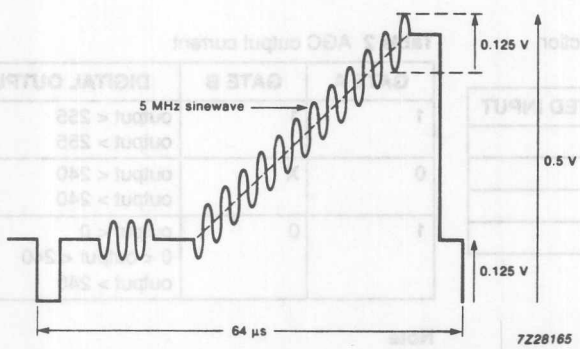


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

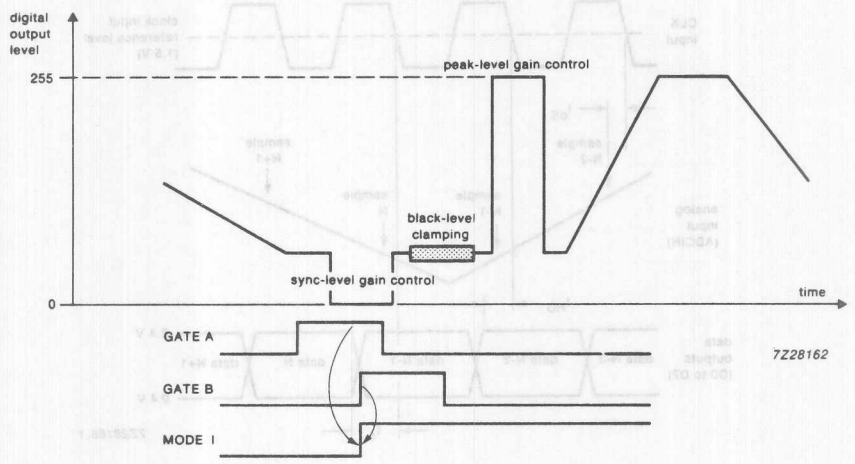


Fig.4 Control mode 1.

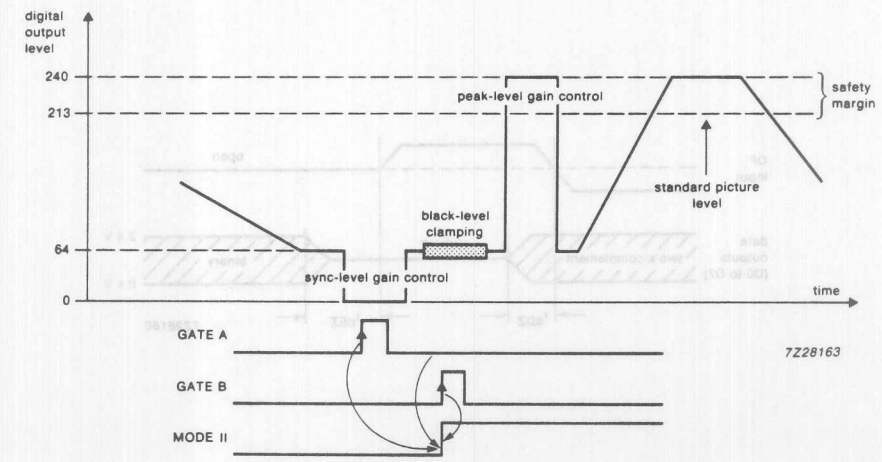


Fig.5 Control mode 2.

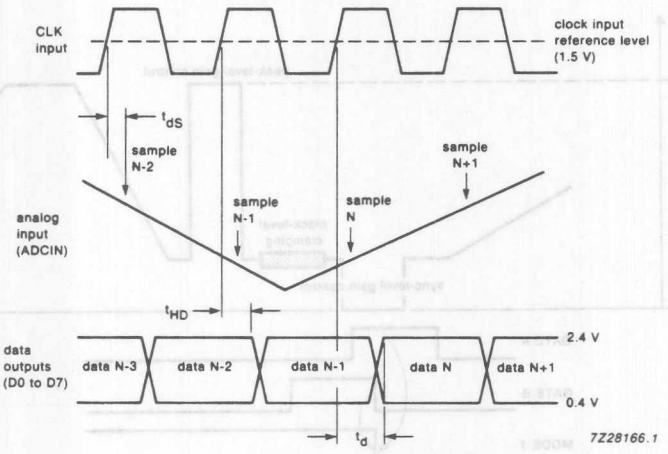


Fig.6 Timing diagram.

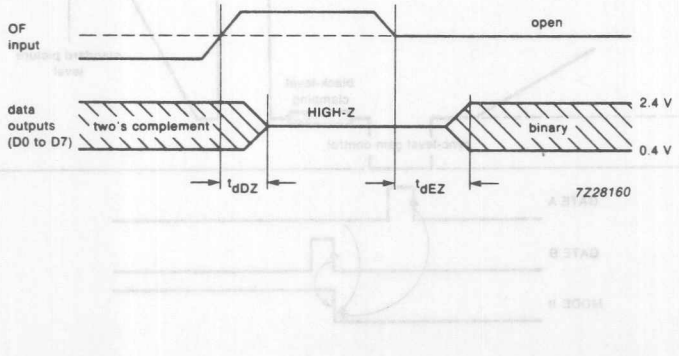


Fig.7 Output format timing diagram.

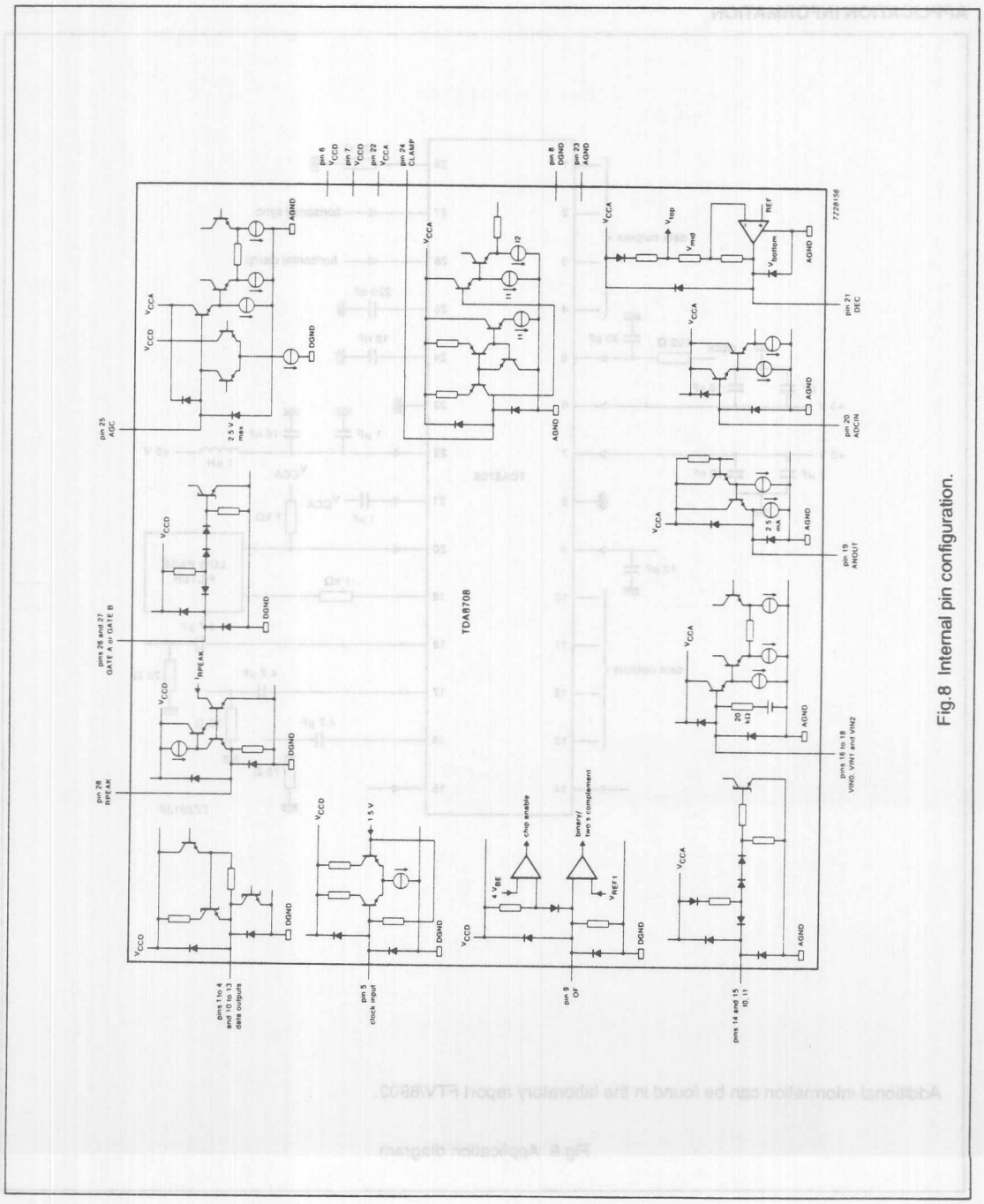
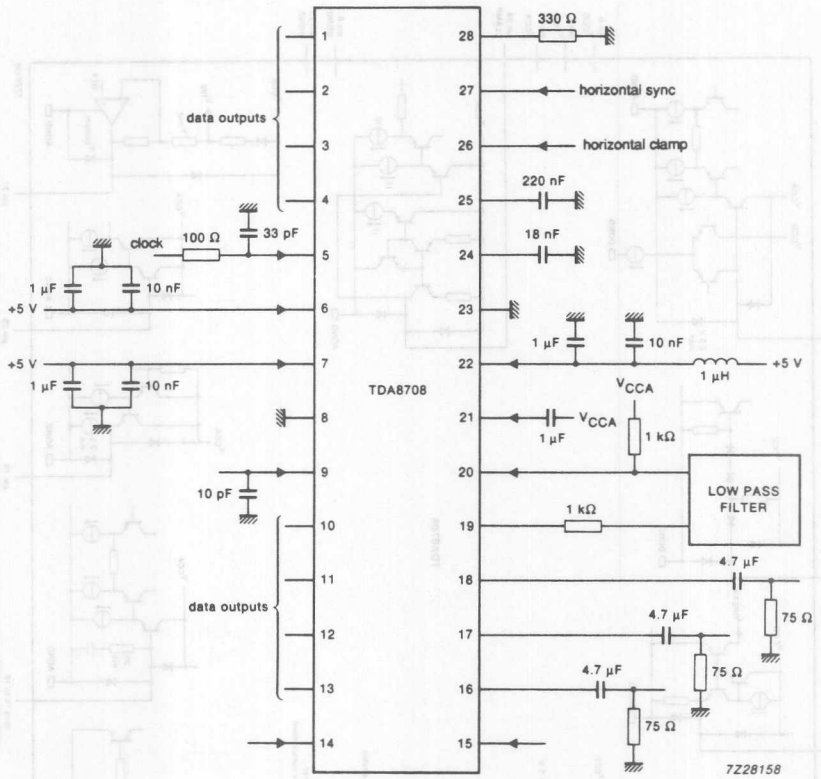


Fig.8 Internal pin configuration.

APPLICATION INFORMATION



Additional information can be found in the laboratory report FTV/8902.

Fig.9 Application diagram.

Video analog interface for chroma input

TDA8709

FEATURES

- 8-bit resolution
- Sampling rate up to 30 MHz
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- low level AC clock inputs and outputs
- Clamp function with selection for "16" or "128"
- No sample-and-hold circuit required
- three selectable video inputs

APPLICATIONS

- Video signal processing
- Digital picture processing
- Frame grabbing
- Colour difference signals (U, V)
- Y, R, G, B signals
- Chrominance signal (C)

GENERAL DESCRIPTION

The TDA8709 is a bipolar analog input interface for video signal processing. It includes an input selector (1 out of three video signals), video amplifier with clamp and external gain control, and an 8-bit analog-to-digital converter (ADC) with a sampling rate of 30 MHz.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	-	5.5	V
V_{CCD}	digital supply voltage		4.5	-	5.5	V
V_{CCO}	output supply voltage		4.5	-	5.5	V
I_{CCA}	analog supply current		-	-	45	mA
I_{CCD}	digital supply current		-	-	30	mA
I_{CCO}	output supply current		-	-	15	mA
ILE	DC integral linearity error		-	-	±1	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
f_{CLK}	maximum clock frequency		30	-	-	MHz
B	–3 dB bandwidth (preamplifier)		12	18	-	MHz
P_{tot}	total power dissipation		-	365	495	mW

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8709	28	DIL	plastic	SOT117
TDA8709	28	SO28	plastic	SOT136A

Video analog interface for chroma input TDA8709

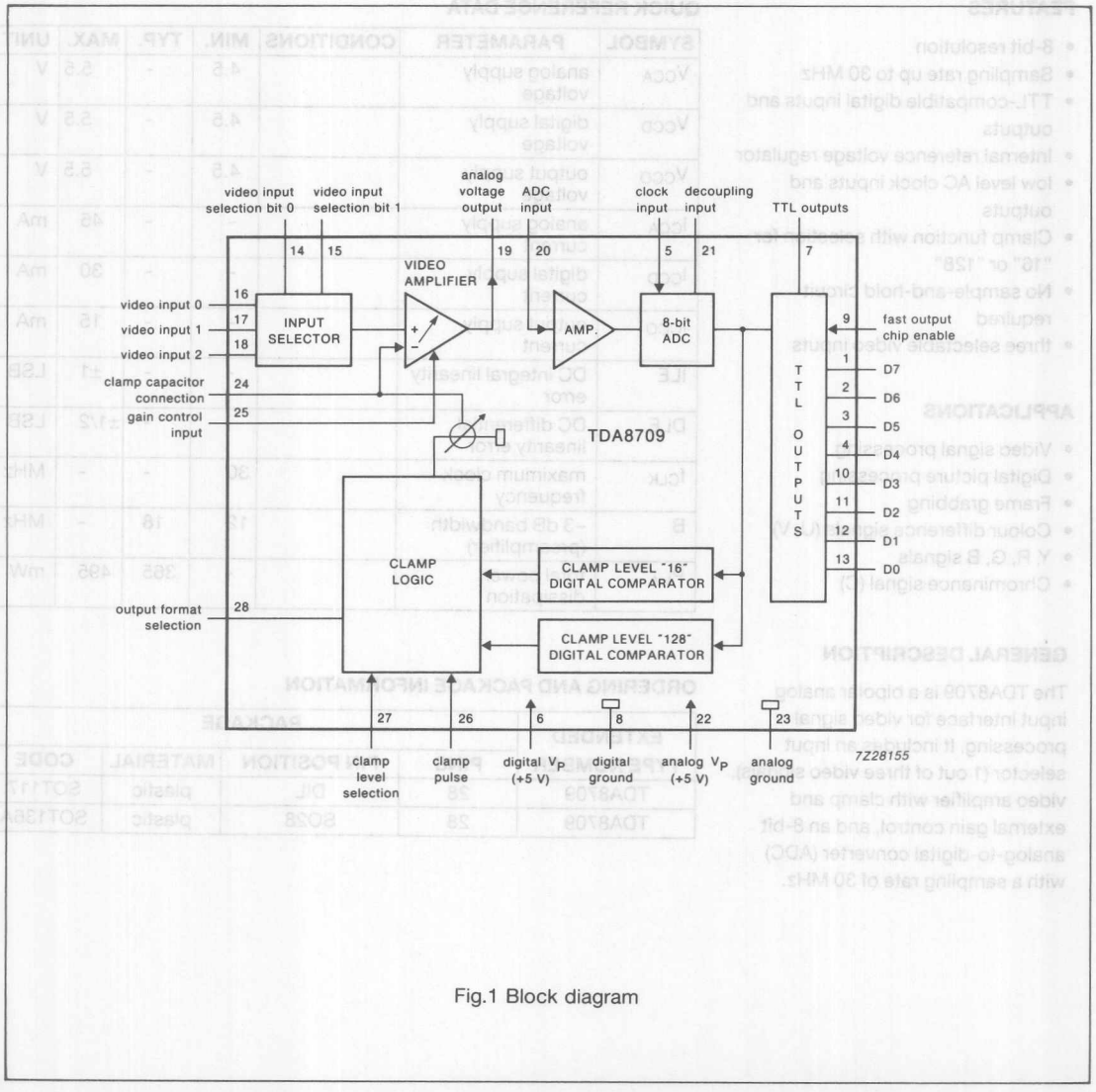


Fig.1 Block diagram

PIN CONFIGURATION

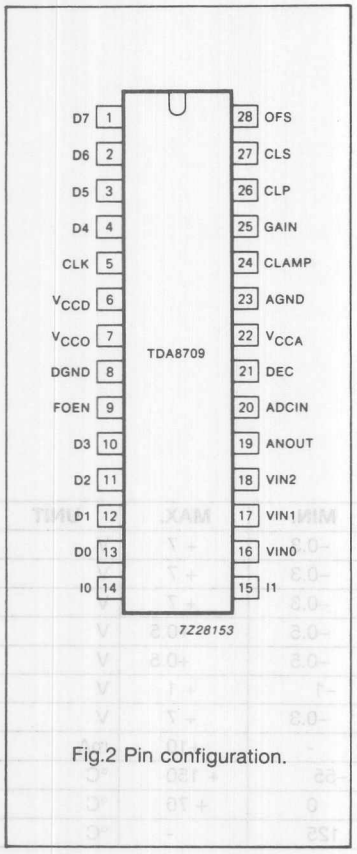


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output, bit 7 (MSB)
D6	2	data output, bit 6
D5	3	data output, bit 5
D4	4	data output, bit 4
CLK	5	clock input
V_{CCD}	6	digital positive supply voltage (+ 5 V)
V_{CCO}	7	TTL outputs positive supply voltage (+ 5 V)
DGND	8	digital ground
FOEN	9	fast output chip enable
D3	10	data output, bit 3
D2	11	data output, bit 2
D1	12	data output, bit 1
D0	13	data output, bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog positive supply voltage (+ 5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
GAIN	25	gain control input
CLP	26	clamp pulse
CLS	27	clamp level selection
OFS	28	output format selection

FUNCTIONAL DESCRIPTION

The TDA8709 is an 8-bit ADC with internal clamping and a preamplifier with adjustable gain.

The clamping value is switched via pin 27 between digital 16 (for luminance or R, G, B signals) and digital 128 (for chrominance or colour difference signals). While clamping pulse at pin 27 is logic 1, the device will adjust the clamp level to the chosen value. The output format can be selected between binary and two's complement at pin 28.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	–0.3	+ 7	V
V_{CCD}	digital supply voltage range	–0.3	+ 7	V
V_{CCO}	output supply voltage range	–0.3	+ 7	V
$VCCA - V_{CCD}$	supply voltage difference	–0.5	+0.5	V
$V_{CCO} - V_{CCD}$	supply voltage difference	–0.5	+0.5	V
$V_{CCA} - V_{CCO}$	supply voltage difference	–1	+ 1	V
V_I	input voltage range	–0.3	+ 7	V
I_O	output current	-	+10	mA
T_{stg}	storage temperature range	–55	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
T_j	junction temperature	125	-	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT117)	55	-	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air (SOT136)	70	-	K/W

CHARACTERISTICS

$V_{CCA} = V_{22} - V_{23} = 4.5$ to 5.5 V; $V_{CCD} = V_6 - V_8 = 4.5$ to 5.5 V; $V_{CCO} = V_7 - V_8 = 4.5$ to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ to + 0.5 V; $V_{CCO} - V_{CCD} = -0.5$ to + 0.5 V; $V_{CCA} - V_{CCO} = -0.5$ to + 0.5 V, $T_{amb} = 0$ to + 70 °C; Typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5	5.5	V
V_{CCD}	digital supply voltage		4.5	5	5.5	V
V_{CCO}	output supply voltage		4.5	5	5.5	V
I_{CCA}	analog supply current		-	37	45	mA
I_{CCD}	digital supply current		-	24	30	mA
I_{CCO}	output supply current		-	12	16	mA
Preamplifier inputs						
VIN(0-2) inputs						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	note 1	*	1	1.6	V
$\|Z_i\|$	input impedance	f = 6 MHz	10	20	-	kΩ
C_I	input capacitance	f = 6 MHz	-	1	-	pF
I0 and I1 TTL inputs (see Table 1)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2	-	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	–400	-	-	µA
I_{IH}	input current HIGH	$V_I = 2.7$ V	-	-	20	µA
CLS, OFS, CLP, TTL inputs (see Fig 3)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2	-	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	–400	-	-	µA
I_{IH}	input current HIGH	$V_I = 2.7$ V	-	-	20	µA
GAIN input (pin 25)						
V_{25}	voltage for minimum gain		-	*	-	V
V_{25}	voltage for maximum gain		-	*	-	V
I_I	input current		-	*	-	µA
	stability gain/temperature		-	*	-	%
CLAMP input (pin 24)						
V_{24}	CLAMP voltage for ADC output = 128 V		-	3.5	-	V
I_{24}	CLAMP output current	see Table 2	-	-	-	
Video amplifier outputs						
ANOUT output (pin 19)						
I_{19}	internal current source		2	2.5	-	mA
V_{19}	output DC voltage for black level	CLS = logic 1	-	*	-	V
V_{19}	output DC voltage for black level	CLS = logic 0	-	*	-	V
$V_{19(p-p)}$	output AC voltage (peak-to-peak value)	$V_{VIN} = 1$ V(p-p); $V_{25} = 3.6$ V	-	1	-	V
Z_{19}	output impedance		-	20	-	Ω

* Value to be fixed.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Preamplifier dynamic characteristics						
	crosstalk between VIN inputs		-	–60	–55	dB
G_d	differential gain		-	2	-	%
ϕ_d	differential phase		-	2	-	deg
B	–3 dB bandwidth		12	-	-	MHz
S/N	signal-to-noise ratio	note 2	60	-	-	dB
SVRR	supply voltage ripple rejection	note 3	-	45	-	dB
ΔG	gain range		–4.5	-	10	dB
Analog-to-digital converter inputs CLK input (pin 5)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2	-	V_{CCD}	V
I_{IL}	input current LOW	V_{CLK} = 0.4 V	–400	-	-	μA
I_{IH}	input current HIGH	V_{CLK} = 2.7 V	-	-	100	μA
$\|Z_i\|$	input impedance	f_{CLK} = 10 MHz	-	4	-	kΩ
C_I	input capacitance	f_{CLK} = 10 MHz	-	4.5	-	pF
FOEN input (see Table 3)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	V_9 = 0.4 V	*	-	-	μA
I_{IH}	input current HIGH	V_9 = 2.7 V	-	-	*	μA
ADCIN input (pin 20) (see Table 4)						
V_{20}	input voltage	digital out = 00	-	V_{CCA} – 1.6	-	V
V_{20}	input voltage	digital out = 255	-	V_{CCA} – 1.1	-	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		-	0.5	-	V
I_{20}	input current		-	1	10	μA
$\|Z_i\|$	input impedance	f = 6 MHz	-	50	-	MΩ
C_I	input capacitance	f = 6 MHz	-	1	-	pF
Analog-to-digital converter outputs Digital outputs D(0-7)						
V_{OL}	output voltage LOW	I_O = 2 mA	0	-	0.6	V
V_{OH}	output voltage HIGH	I_O = –0.4 mA	2.4	-	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	-	+ 20	μA
Switching characteristics						
f_{CLK}	CLK input maximum frequency	see Fig.4		-	30	MHz

* Value to be fixed.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog signal processing (f_{CLK} = 30 MHz)						
B	–3 dB bandwidth		-	12	-	MHz
G_d	differential gain	note 4; Fig.3	-	2	-	%
ϕ_d	differential phase	note 4; Fig.3	-	2	-	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 4	-	-	0	dB
f_{all}	harmonics (full-scale), all components	f_i = 4.43 MHz; note 4	-	–55	-	dB
SVRR	supply voltage ripple rejection	note 5	-	1	5	%/V
Transfer function (f_{CLK} = 30 MHz)						
ILE	DC integral linearity error		-	-	±1	LSB
DLE	DC differential linearity error		-	-	±0.5	LSB
ILE	AC integral linearity error	note 6	-	-	±2	LSB
Timing (f_{CLK} = 30 MHz) Digital outputs (C_L = 15 pF; I_{OL} = 2 mA)						
t_{dS}	sampling delay		-	2	-	ns
t_{HD}	output hold time		-	8	-	ns
t_d	output delay time		-	16	20	ns
t_{dEZ}	3-state delay time - output enable	see Fig.5	-	*	*	ns
t_{dDZ}	3-state delay time - output disable	see Fig.5	-	*	*	ns

Notes to the characteristics

1. Signal-to-noise ratio measured with 5 MHz bandwidth

$$SN = 20 \log \frac{V_{ANOUT(p\text{-}p)}}{V_{ANOUT} \text{ noise RMS (B = 5 MHz)}}$$

2. The voltage ratio is expressed as:

$$SVRR = 20 \log \frac{\Delta V_{CCA}}{\Delta G/G}$$

for V_I = 1 V (peak-to-peak), 100 kHz gain = 1 and 1 V supply variation.

3. It is recommended that the rise and fall times of the clock are not less than 2 ns. In addition, a 'good lay-out' for the digital and analog grounds is recommended.

4. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).

5. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

$$SVRR = \frac{\Delta V_{IN(00)} - V_{IN(FF)}/V_{IN(00)} - V_{IN(FF)}}{\Delta V_{CCA}}$$

6. Full-scale sinewave (f_i = 4.4 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 27 MHz.

* Value to be fixed.

Table 1 Video input selection (CVBS)

I1	I0	SELECTED INPUT
0	0	VIN0
1	0	VIN2
0	1	VIN1
1	1	VIN1

Table 2 CLAMP output current

CLS	CLP	DIGITAL OUTPUT	I_{CLAMP}
1	1	output < 128	+ 50 μA
		output > 128	−50 μA
X	0	X	0
0	1	output < 16	+ 50 μA
		16 < output	−50 μA

Where: X = don't care

Table 3 FOEN input coding

FOEN	D0 TO D7
0	active
1	high impedance

Table 4 ADC output coding

		OFS = 0 BINARY OUTPUTS								OFS = 1 TWO'S COMPLEMENT							
STEP	V_{ADCIN}	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} - 1.6 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1		0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
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254		1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} - 1.1 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow		1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

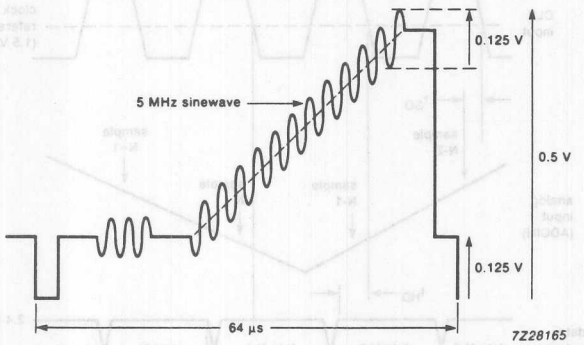


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

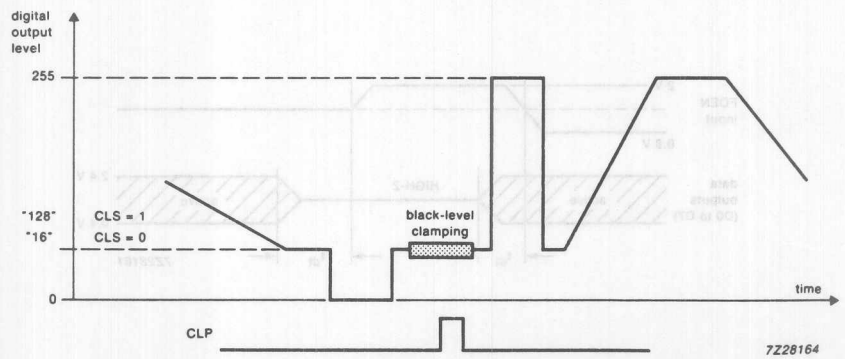


Fig.4 Control mode selection.

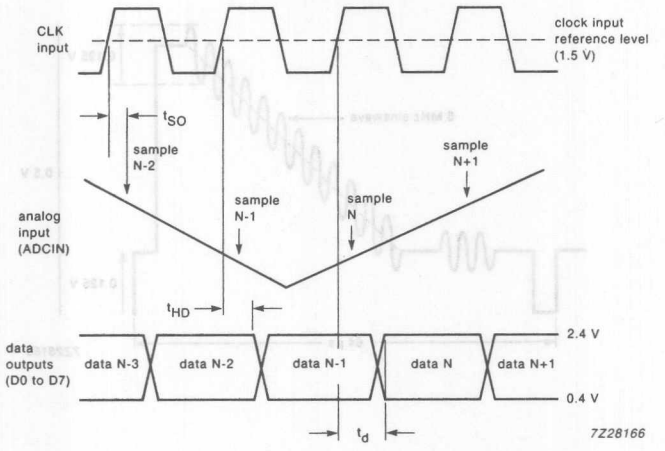


Fig.5 Timing diagram.

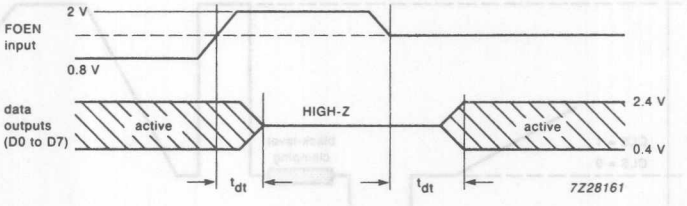


Fig.6 Output format timing diagram.

INTERNAL PIN CONFIGURATIONS

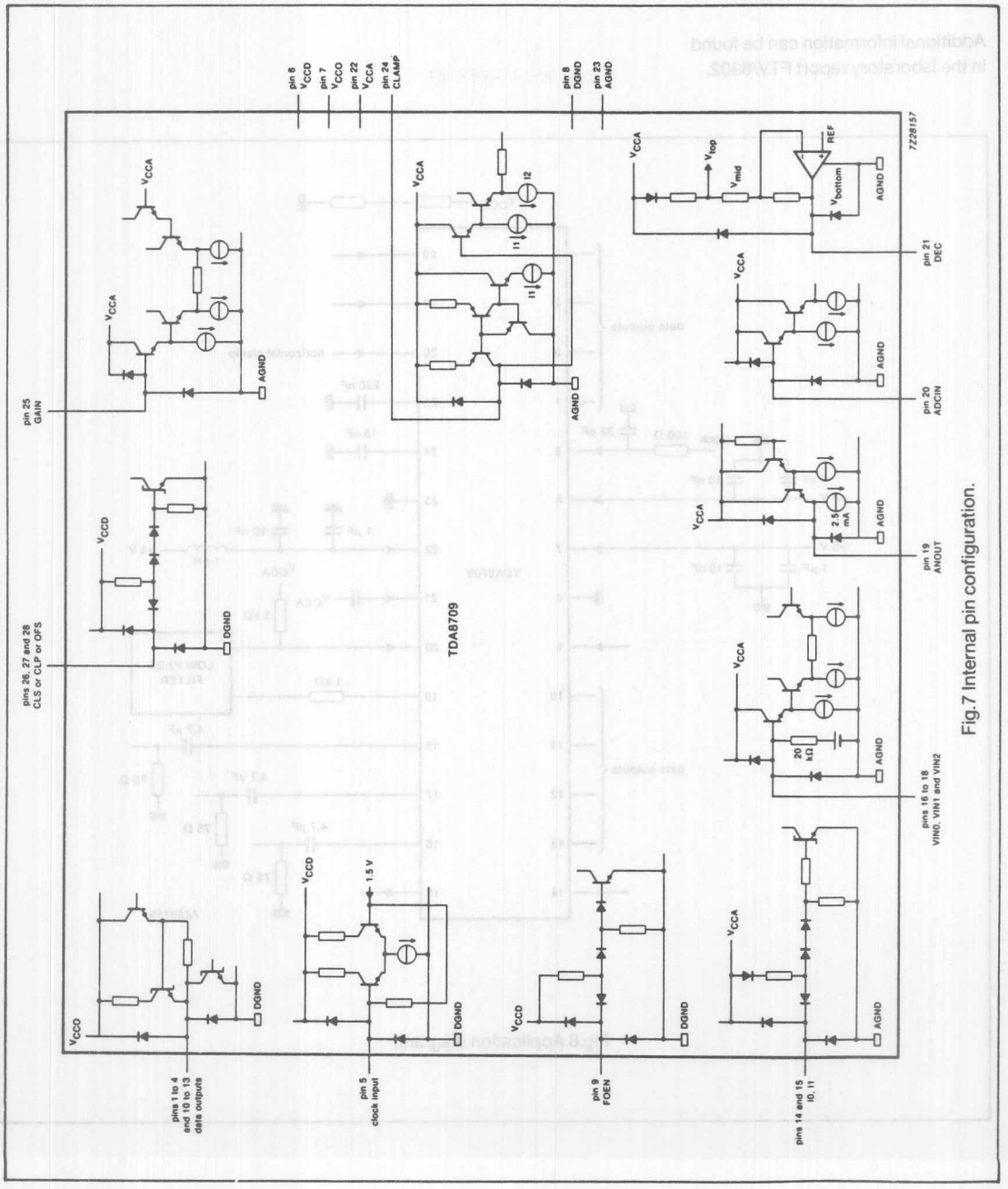


Fig.7 Internal pin configuration.

APPLICATION INFORMATION

Additional information can be found in the laboratory report FTV/8902.

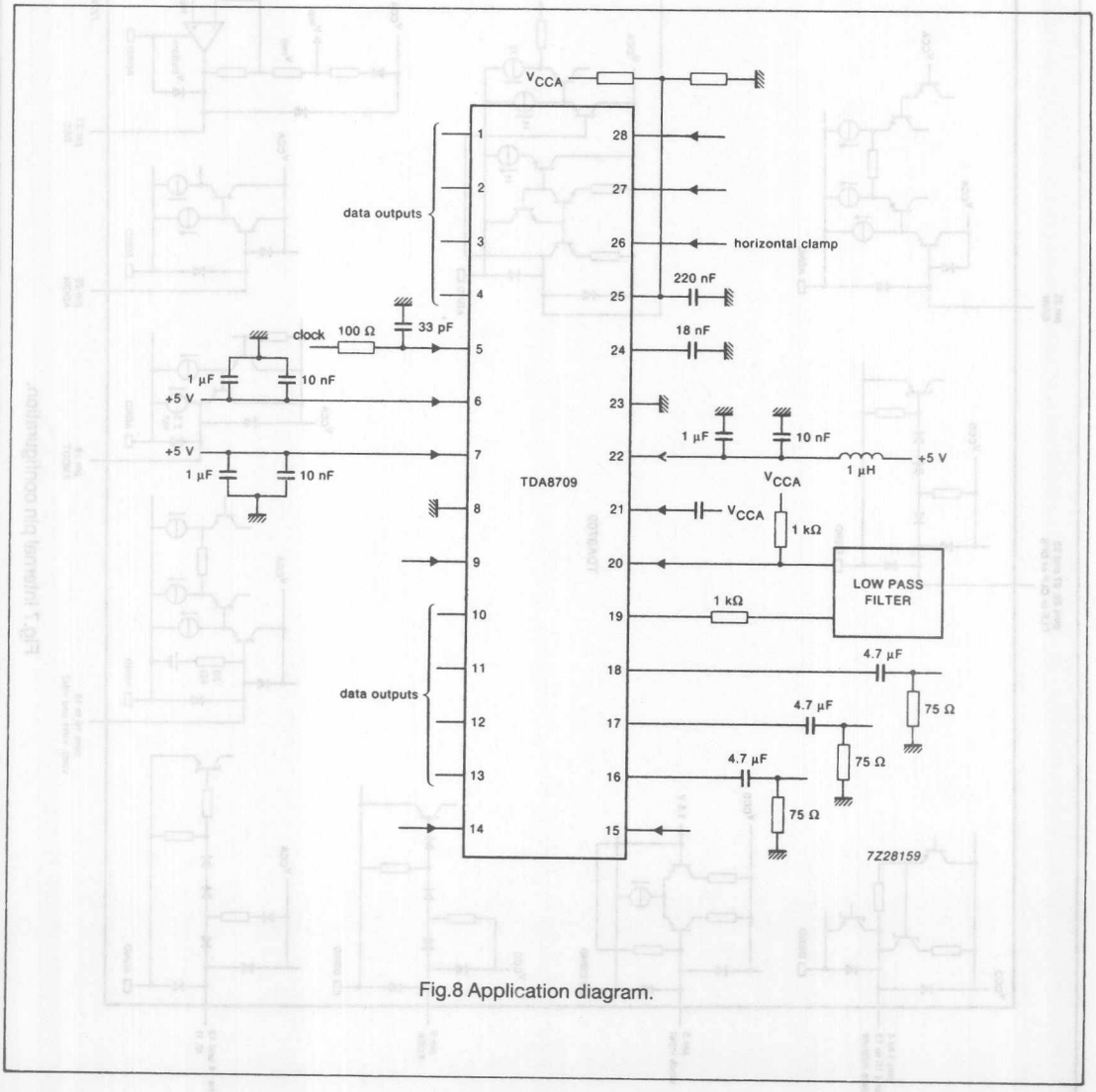


Fig.8 Application diagram.

8-bit high-speed analog-to-digital converter

TDA8713

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.5 effective bits at 4.43 MHz full-scale input at a 40 MHz clock frequency
- Binary or two's complement 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- External reference voltage generator
- Power dissipation only 290 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - video data digitizing
  - radar pulse analysis
  - transient signal analysis
  - high energy physics research
  - Z3 modulators
  - medical imaging

DESCRIPTION

The TDA8713 is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are TTL compatible, although a low-level sine wave clock input signal is allowed.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8713	24	DIL	plastic	SOT101
TDA8713T	24	SO24	plastic	SOT137A

8-bit high-speed analog-to-digital converter

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		-	18	26	mA
I_{CCD}	digital supply current		-	19	25	mA
I_{CCO}	output stages supply current		-	11	14	V
ILE	DC integral linearity error		-	-	± 0.75	LSB
DLE	DC differential linearity error		-	-	± 1/2	LSB
AILE	AC integral linearity error	note 1	-	-	± 2	LSB
B	−3 dB bandwidth	note 2; f_{CLK} = 40 MHz	-	19.5	-	MHz
$f_{CLK}/f_{\overline{CLK}}$	maximum clock frequency	note 3	50	-	-	MHz
P_{tot}	total power dissipation		-	290	415	mW

Notes to the Quick Reference Data

1. Full-scale sinewave (f_i = 4.4 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 27 MHz).

2. The −3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at input).

3. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:

   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak- to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

     If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

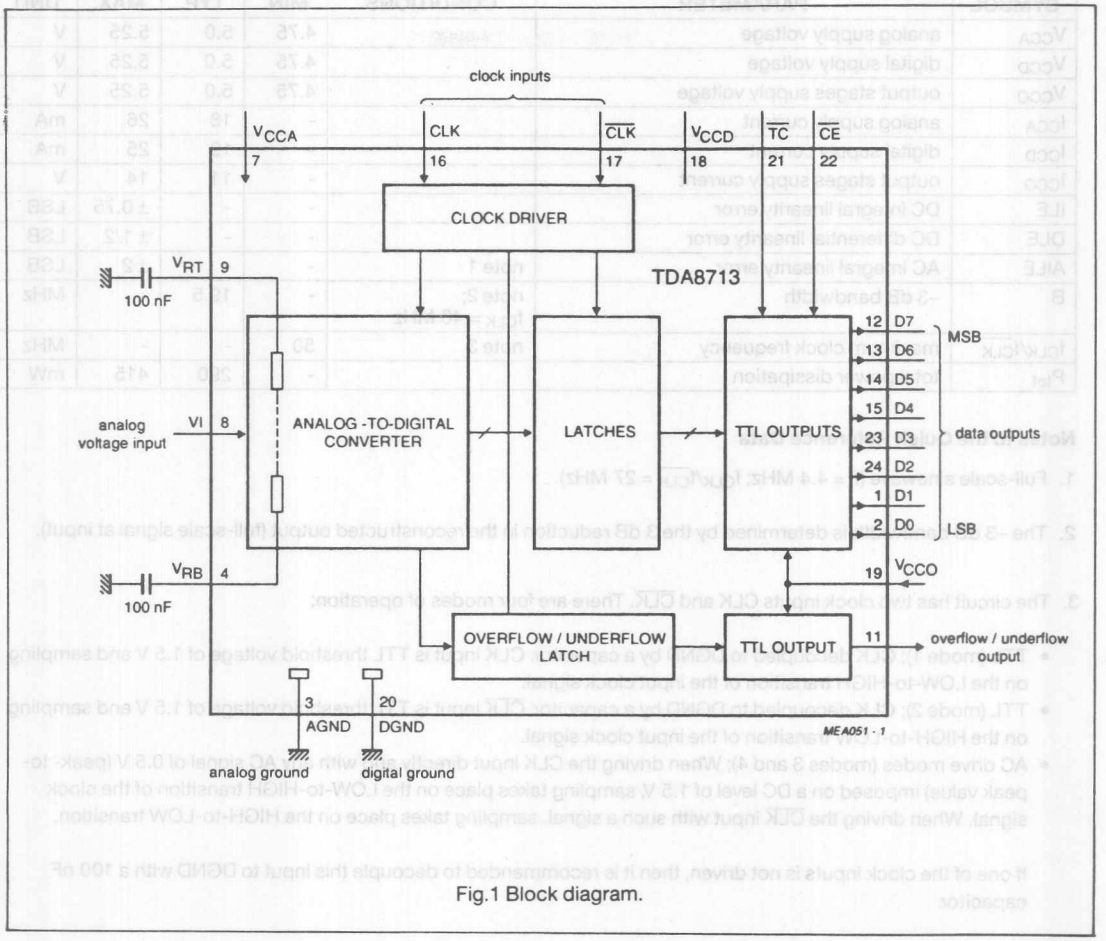


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter

TDA8713

PIN CONFIGURATION

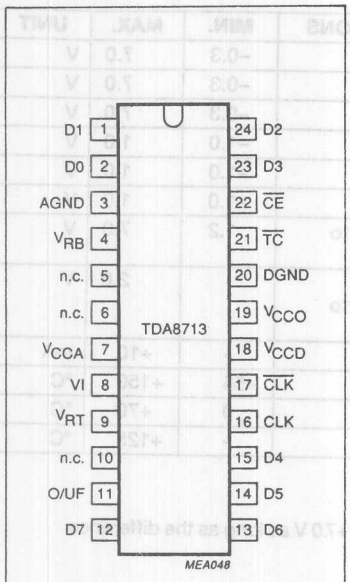


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
AGND	3	analog ground
V_{RB}	4	reference voltage bottom (decoupling)
n.c.	5	not connected
n.c.	6	not connected
V_{CCA}	7	positive supply voltage for analog circuits (+5 V)
VI	8	analog voltage input
V_{RT}	9	reference voltage top (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output, bit 7 (MSB)
D6	13	data output, bit 6
D5	14	data output, bit 5
D4	15	data output, bit 4
CLK	16	clock input
$\overline{CLK}$	17	complementary clock input
V_{CCD}	18	positive supply voltage for digital circuits (+5 V)
V_{CCO}	19	positive supply voltage for output stages (+5 V)
DGND	20	digital ground
$\overline{TC}$	21	input for two's complement output (TTL level input, active LOW)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output, bit 3
D2	24	data output, bit 2

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	see note 1	−0.3	7.0	V
V_{CCD}	digital supply voltage range	see note 1	−0.3	7.0	V
V_{CCO}	output stages supply voltage	see note 1	−0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage differences		−1.0	1.0	V
V_{VI}	input voltage range	referenced to AGND	1.2	7.0	V
$V_{\overline{CLK}}$ / V_{CLK}	AC input voltage for switching (peak-to-peak value)	see note 2; referenced to DGND	-	2.0	V
I_O	output current		-	+10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		0	+70	°C
T_j	junction temperature		-	+125	°C

Notes to the Ratings

1. The supply voltages V_{CCA} and V_{CCD} may have any value between −0.3 V and +7.0 V as long as the difference V_{CCA} - V_{CCD} lies between −1 V and + 1 V.

2. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:

- TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
- TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
- AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

  If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT101	+ 55	K/W
$R_{th\ j\text{-}a}$	SOT137A	+ 75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7 - V_3 = 4.75$ V to 5.25 V; $V_{CCD} = V_{18} - V_{20} = 4.75$ V to 5.25 V; $V_{CCO} = V_{19} - V_{20} = 4.75$ V to 5.25 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $T_{amb} = 0$ °C to +70 °C; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5.0$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output stages supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current		-	18	26	mA
I_{CCD}	digital supply current		-	19	25	mA
I_{CCO}	output stage supply current	all outputs LOW	-	11	14	mA
Inputs CLOCK INPUT CLK AND $\overline{CLK}$ (note 1; referenced to DGND)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V	−400	-	-	µA
I_{IH}	input current HIGH	$V_{CLK}/V_{\overline{CLK}} = 2.7$ V	-	-	100	µA
		$V_{CLK}/V_{\overline{CLK}} = V_{CCD}$	-	-	300	µA
Z_o	input impedance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	-	4	-	kΩ
C_i	input capacitance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	-	4.5	-	pF
$V_{CLK(p-p)} - V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)	note 1; DC level = 1.5 V	0.5	-	2.0	V
INPUTS $\overline{TC}$ AND $\overline{CE}$ (referenced to DGND)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_{IL} = 0.4$ V	−400	-	-	µA
I_{IH}	input current HIGH	$V_{IH} = 2.7$ V	-	-	20	µA
VI (analog input voltage referenced to AGND)						
I_{IL}	input current LOW	$V_{VI} = 1.6$ V	-	0	-	µA
I_{IH}	input current HIGH	$V_{VI} = 3.8$ V	60	120	180	µA
Z_o	input impedance	$f_i = 1$ MHz	-	10	-	kΩ
C_i	input capacitance	$f_i = 1$ MHz	-	14	-	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference voltages for the resistor ladder						
V_{RB}	reference voltage LOW		1.5	1.6	1.9	V
V_{RT}	reference voltage HIGH		3.5	3.8	3.9	V
V_{REF}	differential reference voltage V_{RT}-V_{RB}		2	2.2	-	V
I_{REF}	reference current		-	10	-	mA
R_{LAD}	resistor ladder		-	200	-	Ω
R_{TLC}	temperature coefficient of the ladder		-	0.24	-	Ω/°C
V_{OB}	voltage offset bottom	note 5	-	258	-	mV
V_{OBTC}	voltage offset bottom temperature coefficient	note 5	-	0.1	-	mV/°C
V_{OT}	voltage offset top	note 5	-	132	-	mV
V_{OTTC}	voltage offset top temperature coefficient	note 5	-	−0.3	-	mV/°C
Outputs DIGITAL OUTPUTS (D7 - D0) (referenced to DGND)						
V_{OL}	output voltage LOW	I_O = 1 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_O = −0.4 mA	2.7	-	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	-	20	µA
Switching characteristics (note 1,2; see Fig.3)						
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
Analog signal processing (f_{CLK} = 50 MHz)						
B	−3 dB bandwidth	note 3	-	19.5	-	MHz
G_d	differential gain	note 4	-	0.3	2.0	%
ϕ_d	differential phase	note 4	-	0.4	1.5	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	0	0	0	dB
F_{even}	even harmonics (full-scale)	f_i = 4.43 MHz	-	−65	-	dB
F_{odd}	odd harmonics (full scale)	f_i = 4.43 MHz	-	−55	-	dB
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		-	-	±0.75	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
AILE	AC integral linearity error	note 6	-	-	±2	LSB
EB	effective bits f_i = 1 MHz	f_{CLK} = 20MHZ	-	7.8	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 40MHZ	-	7.5	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 50MHZ	-	7.2	-	bits
Timing (note 7; see Figs 3 to 6; f_{CLK} = 50 MHz)						
t_{dS}	sampling delay		-	-	2	ns
t_{HD}	output hold time		6	-	-	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	-	8	10	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	-	14	16	ns
t_{dZH}	3-state output delay times	enable-to-HIGH	-	19	25	ns
t_{dZL}	3-state output delay times	enable-to-LOW	-	16	20	ns
t_{dHZ}	3-state output delay times	disable-to-HIGH	-	14	20	ns
t_{dLZ}	3-state output delay times	disable-to-LOW	-	9	12	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

     If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.
2. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 2 ns.
3. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
4. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
5. Analog input voltages producing code 00 up to and including FF
   - V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C.
   - V_{OBTC} (voltage offset bottom temperature coefficient) is the dependence of V_{OB} with temperature.
   - V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
   - V_{OTTC} (voltage offset top temperature coefficient) is the dependence of V_{OT} with temperature.
6. Full-scale sinewave (f_i = 4.4 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 27 MHz).
7. Output data acquisition
   - Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
   - Output data is fully stable during the low level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; referenced to AGND, V_{RB} = 1.6 V, V_{RT} = 3.8 V)

STEP	$V_{VI(P-P)}$	O/UF	BINARY OUTPUT BITS								TWO'S COMPLEMENT OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow	<1.858	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1.858	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	.	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	3.668	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow	>3.668	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

Table 2 Mode selection

$\overline{TC}$	$\overline{CE}$	D7 - D0	O/UF
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

Where: X = don't care.

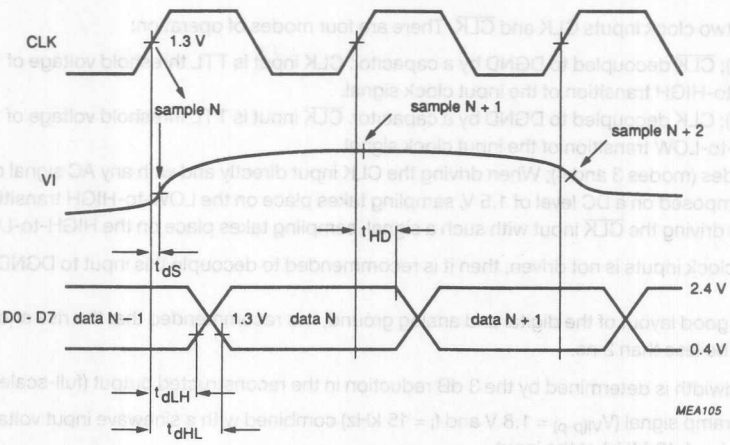


Fig.3 Timing diagram.

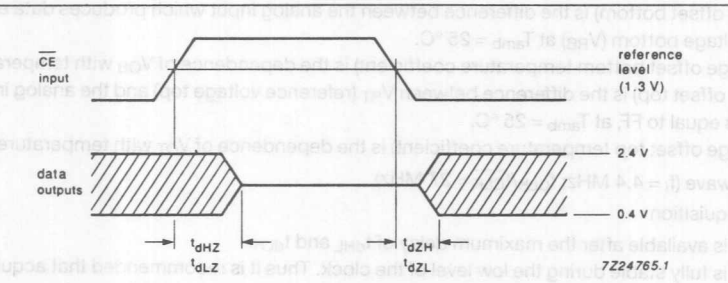


Fig.4 3-state delay timing diagram.

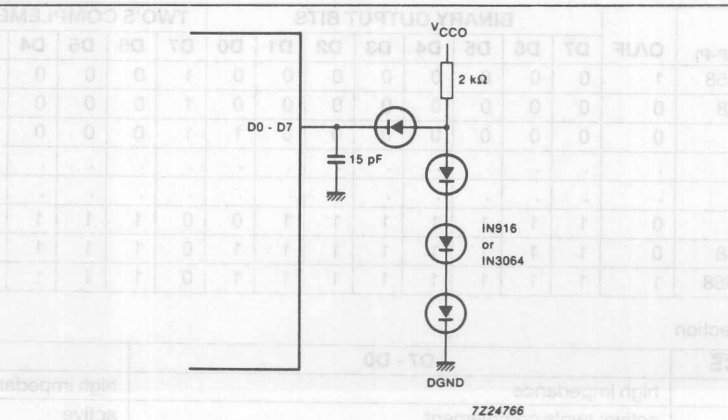


Fig.5 Load circuit for timing measurement; data outputs ($\overline{CE}$ = LOW).

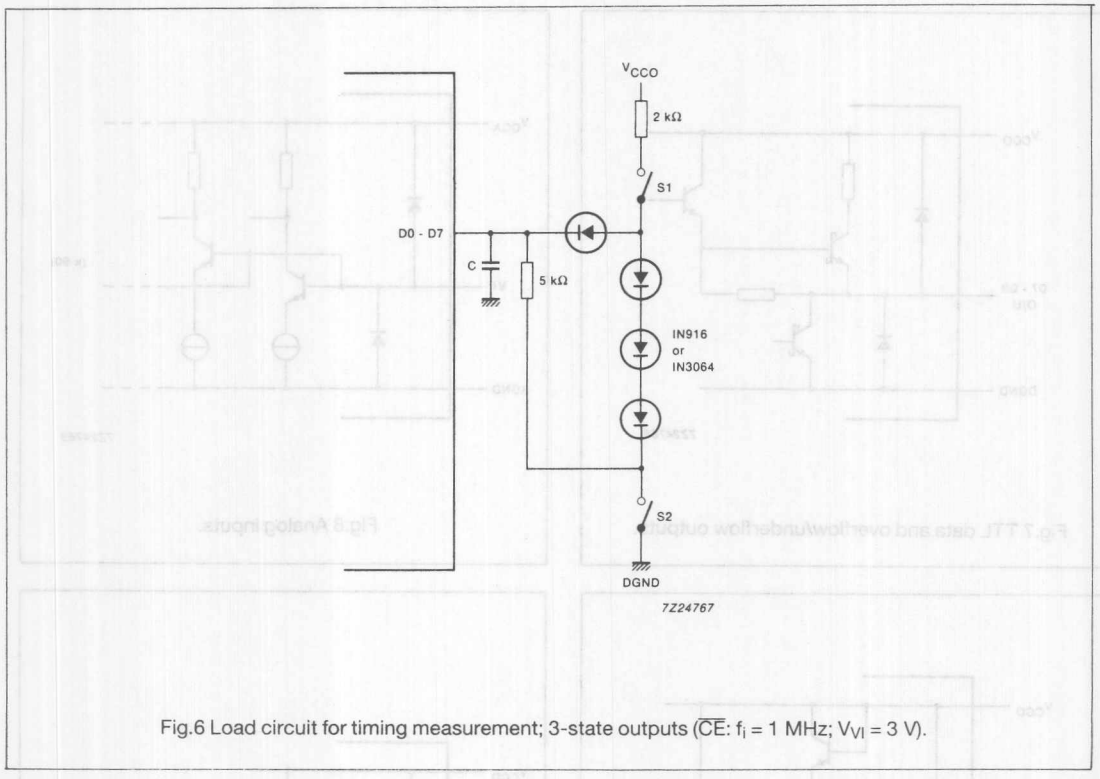


Fig.6 Load circuit for timing measurement; 3-state outputs ($\overline{CE}$: f_i = 1 MHz; V_{VI} = 3 V).

Note to Fig.6

TIMING MEASUREMENT	SWITCH S1	SWITCH S2	CAPACITOR C
t_{dZH}	open	closed	15 pF
t_{dZL}	closed	open	15 pF
t_{dHZ}	closed	closed	5 pF
t_{dLZ}	closed	closed	5 pF

INTERNAL PIN CONFIGURATIONS

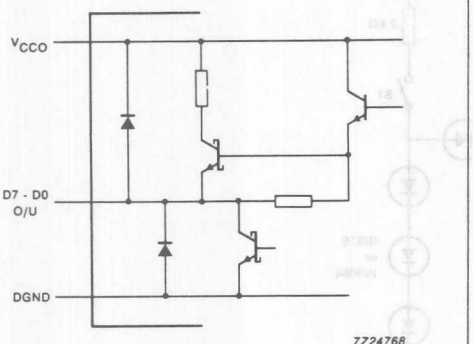


Fig.7 TTL data and overflow/underflow outputs.

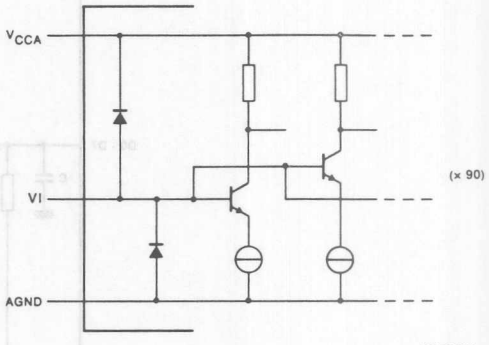


Fig.8 Analog inputs.

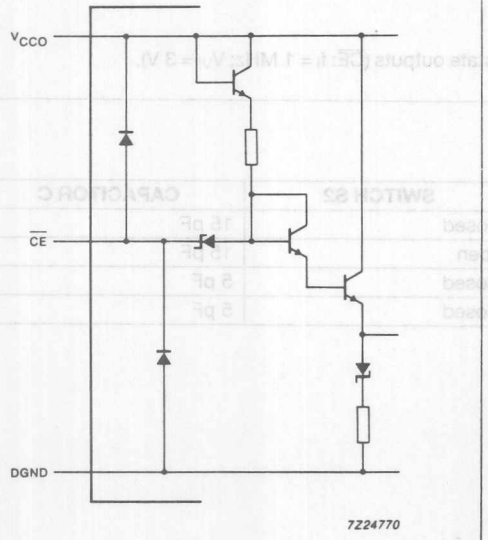


Fig.9 $\overline{CE}$ (3-state) input.

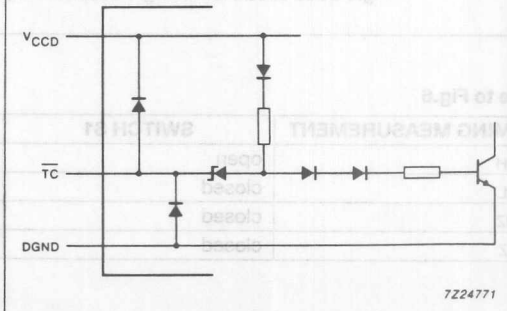


Fig.10 $\overline{TC}$ (two's complement) input.

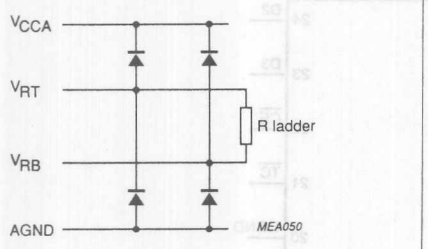


Fig.11 V_{RB}, V_{RT}.

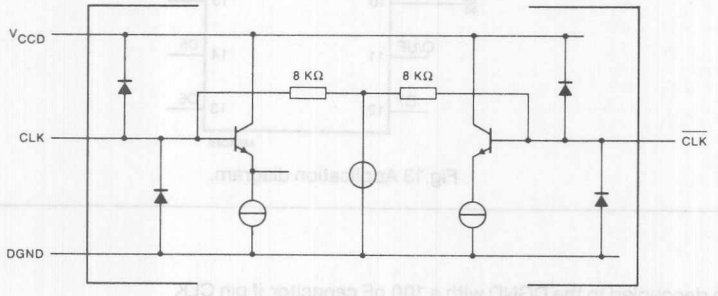


Fig.12 CLK and $\overline{CLK}$ inputs.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/9001).

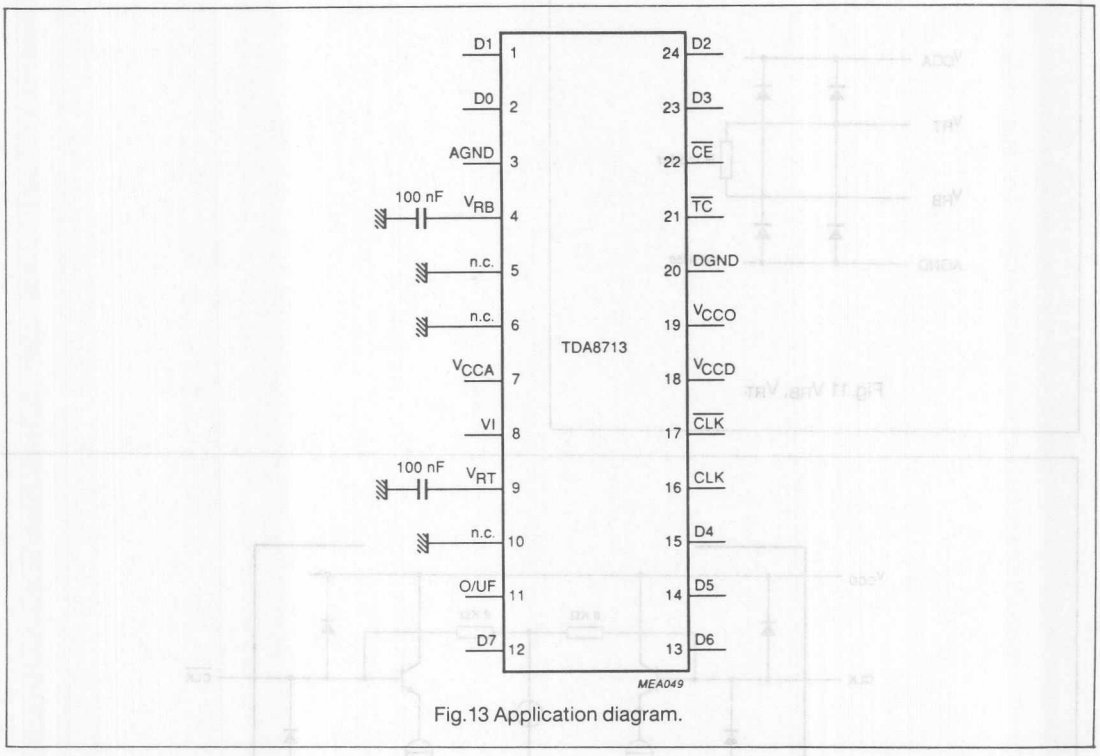


Fig.13 Application diagram.

Notes to Fig.13

1. $\overline{CLK}$ should be decoupled to the DGND with a 100 nF capacitor, if pin CLK is used (see 'Notes to the characteristics', note 1).
2. CLK and $\overline{CLK}$ can be used in a differential mode (see 'Notes to the characteristics', note 1).
3. V_{RB} and V_{RT} are decoupled to AGND.
4. Analog and digital supplies should be separated and decoupled.
5. Pins 5,6 and 10 should be connected to AGND in order to prevent noise influence.
6. The external voltage regulator must be build in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.

8-bit high-speed analog-to-digital converter

TDA8715

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.5 effective bits at 4.43 MHz full-scale input at a 40 MHz clock frequency)
- ECL (10KH family) compatible digital inputs and outputs
- Overflow/underflow ECL output
- Low-level AC clock input signal allowed
- Power dissipation only 325 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - video data digitizing
  - radar pulse analysis
  - transient signal analysis
  - high energy physics research
  - $\Sigma\Delta$ modulators
  - medical imaging

DESCRIPTION

The TDA8715 is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for profesional video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are 10KH ECL compatible.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8715	18	DIL	plastic	SOT102
TDA8715T	20	SO20	plastic	SOT163A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		–4.7	–5.2	–5.7	V
V_{EED}	digital supply voltage		–4.7	–5.2	–5.7	V
I_{EEA}	analog supply current		-	20	25	mA
I_{EED}	digital supply current	see note	-	52	60	mA
ILE	DC integral linearity error		-	± 0.4	± 0.75	LSB
DLE	DC differential linearity error		-	± 0.25	± 0.5	LSB
EB	effective bits (f_i = 4.43 MHz)	f_{CLK} = 50 MHz	-	7.2	-	bits
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
T_{amb}	operating ambient temperature range		0	-	+125	°C
P_{tot}	total power dissipation	see note	-	325	425	mW

Note to the Quick Reference Data

All digital outputs connected to V_{EED} via 2.2 kΩ resistors.

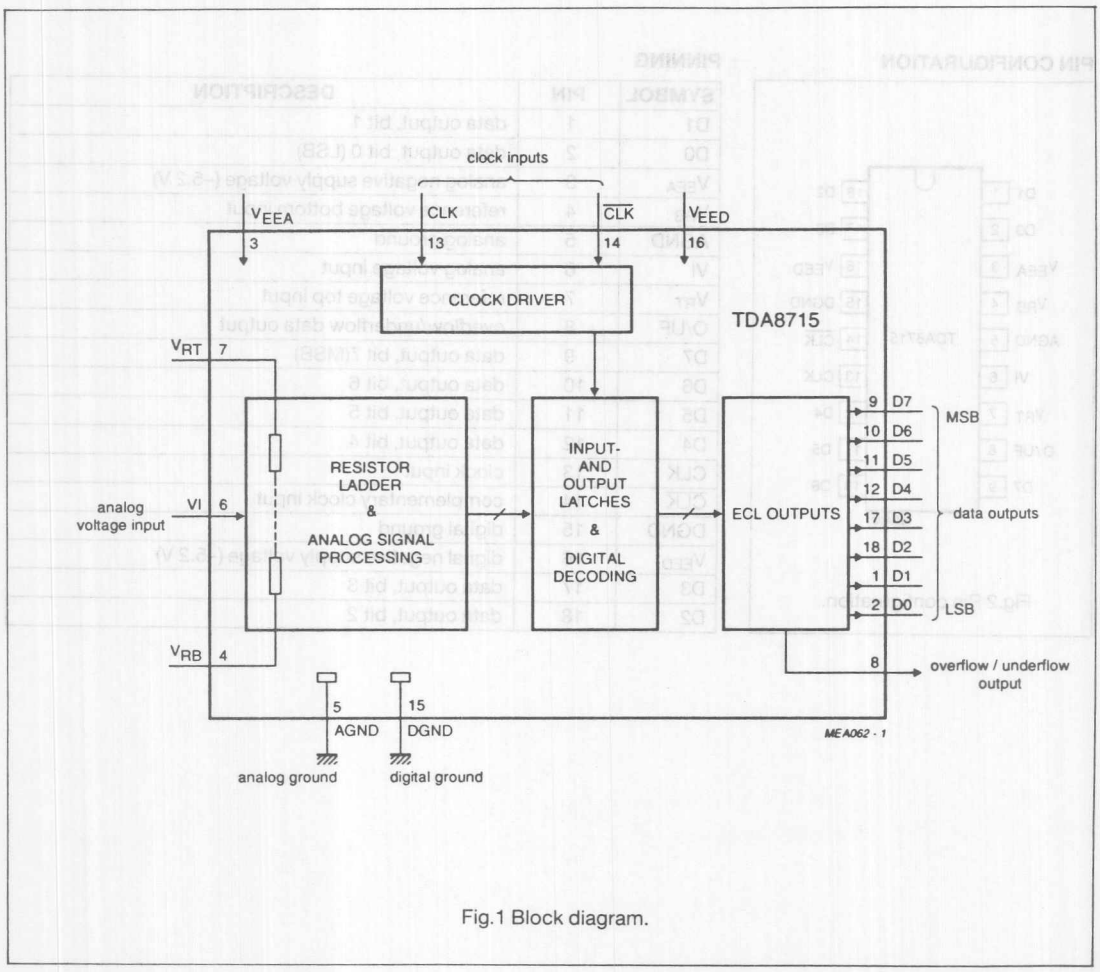


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter TDA8715

PIN CONFIGURATION

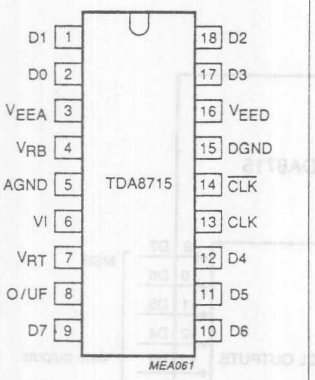


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
V_{EEA}	3	analog negative supply voltage (−5.2 V)
V_{RB}	4	reference voltage bottom input
AGND	5	analog ground
VI	6	analog voltage input
V_{RT}	7	reference voltage top input
O/UF	8	overflow/underflow data output
D7	9	data output, bit 7(MSB)
D6	10	data output, bit 6
D5	11	data output, bit 5
D4	12	data output, bit 4
CLK	13	clock input
$\overline{CLK}$	14	complementary clock input
DGND	15	digital ground
V_{EED}	16	digital negative supply voltage (−5.2 V)
D3	17	data output, bit 3
D2	18	data output, bit 2

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage range		−7	0.3	V
V_{EED}	digital supply voltage range		−7	0.3	V
V_{VI}	input voltage range		−7	0.3	V
V_{CLK}/ $V_{\overline{CLK}}$	AC input voltage for switching (peak-to-peak value)	see note	-	2.0	V
I_O	output current		−15	+10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		0	70	°C
T_j	junction temperature		-	+175	°C

Note to the Ratings

The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals or with two complementary sinewave signals, imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- When driving the CLK input with a ECL signal only (Asymmetrical drive modes), it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT102	+65	K/W
$R_{th\ j\text{-}a}$	SOT163A	0	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{EEA} = V_3 - V_5 = -4.7$ V to -5.7 V; $V_{EED} = V_{16} - V_{15} = -4.7$ V to -5.7 V; AGND and DGND shorted together; $T_{amb} = 0$ °C to 70 °C; unless otherwise specified (typical values measured at $V_{EEA} = -5.2$V; $V_{EED} = -5.2$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{EEA}	analog supply voltage		−4.7	−5.2	−5.7	V
V_{EED}	digital supply voltage		−4.7	−5.2	−5.7	V
I_{EEA}	analog supply current		-	20	25	mA
I_{EED}	digital supply current	note 5	-	52	60	mA
ΔV_{EE}	supply voltage difference V_{EEA} - V_{EED}		−0.5	0	+0.5	V
Reference voltages for the resistor ladder						
V_{RB}	reference voltage LOW		−3.2	−3.0	−2.7	V
V_{RT}	reference voltage HIGH		−0.9	−0.6	−0.4	V
V_{ref}	differential reference voltage V_{RT}-V_{RB}		2.3	2.4	-	V
I_{ref}	reference current		-	12.6	-	mA
R_{LAD}	resistor ladder		-	200	-	Ω
R_{TLC}	temperature coefficient of the ladder		-	0.24	-	Ω/°C
V_{OB}	voltage offset bottom	note 6	-	317	-	mV
V_{OBTC}	voltage offset bottom temperature coefficient	note 6	-	0.1	-	mV/°C
V_{OT}	voltage offset top	note 6	-	174	-	mV
V_{OTTC}	voltage offset top temperature coefficient	note 6	-	−0.3	-	mV/°C
Inputs CLOCK INPUT CLK (note 1)						
V_{IL}	input voltage LOW		−1.85	−1.77	−1.65	V
V_{IH}	input voltage HIGH		−0.96	−0.88	−0.81	V
I_{IL}	input current LOW	$V_{CLK} = -1.77$ V	-	−240	-	µA
I_{IH}	input current HIGH	$V_{CLK} = -0.88$ V	-	−14	-	µA
R_i	input resistance	f_{CLK} = 10 MHz	-	7.0	-	kΩ
		f_{CLK} = 50 MHz	-	3.5	-	kΩ
C_i	input capacitance	f_{CLK} = 10 MHz	-	1.8	-	pF
		f_{CLK} = 50 MHz	-	1.55	-	pF
CLOCK INPUT $\overline{CLK}$ (note 1)						
V_{IL}	input voltage LOW		−1.85	−1.77	−1.65	V
V_{IH}	input voltage HIGH		−0.96	−0.88	−0.81	V
I_{IL}	input current LOW	$V_{\overline{CLK}} = -1.77$ V	-	−140	-	µA
I_{IH}	input current HIGH	$V_{\overline{CLK}} = -0.88$ V	-	75	-	µA
R_i	input resistance	$f_{\overline{CLK}}$ = 10 MHz	-	9.3	-	kΩ
		$f_{\overline{CLK}}$ = 50 MHz	-	4.5	-	kΩ
C_i	input capacitance	$f_{\overline{CLK}}$ = 10 MHz	-	2.6	-	pF
		$f_{\overline{CLK}}$ = 50 MHz	-	2.4	-	pF
$V_{CLK(p-p)} - V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)		0.5	0.9	1.1	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VI (analog input with V_{RB} = –3.1 V and V_{RT} = –0.6 V)						
I_{IL}	input current LOW	data output 00	-	0	-	µA
I_{IH}	input current HIGH	data output FF	-	120	-	µA
R_i	input resistance	f_i = 1 MHz	-	9.4	-	kΩ
C_i	input capacitance	f_i = 1 MHz	-	13.7	20	pF
Outputs DIGITAL OUTPUTS (D7 - D0 and 0/UF) (Digital 10KH ECL outputs)						
V_{OL}	output voltage LOW	T_{amb} = 25 °C	–1.95	–1.77	–1.65	V
V_{OH}	output voltage HIGH	T_{amb} = 25 °C	–0.96	–0.88	–0.81	V
I_{OL}	output current LOW		-	1.8	4	mA
I_{OH}	output current HIGH		-	1.8	4	mA
Switching characteristics						
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
Analog signal processing (f_{CLK} = 50 MHz)						
B	–3 dB bandwidth	note 2	-	20.5	-	MHz
G_d	differential gain	note 3	-	0.3	2.0	%
ϕ_d	differential phase	note 3	-	0.4	1.5	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	0	0	0	dB
F_{even}	even harmonics (full-scale)	f_i = 4.43 MHz	-	–60	-	dB
F_{odd}	odd harmonics (full scale)	f_i = 4.43 MHz	-	–50	-	dB
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		-	-	± 0.75	LSB
DLE	DC differential linearity error		-	-	± 0.5	LSB
AILE	AC integral linearity error	note 4	-	± 0.75	-	LSB
EB	effective bits f_i = 600 kHz	f_{CLK} = 20MHz	-	7.8	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 50MHz	-	7.2	-	bits
EB	effective bits f_i = 7 MHz	f_{CLK} = 50MHz	-	6.9	-	bits
Timing (note 7; see Fig. 3)						
t_{dS}	sampling delay		-	1	3	ns
t_{HD}	output hold time		3	4	-	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	4	5	8	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	6	7	10	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals or with two complementary sinewave signals, imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- When driving the CLK input with a ECL signal only (Asymmetrical drive modes) , it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

2. The −3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).

3. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.

4. Full-scale sinewave (f_i = 4.43 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 50 MHz).

5. All digital outputs connected to V_{EED} via 2.2 kΩ resistors.

6. Analog input voltages producing code 00 up to and including FF

- V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C.
- V_{OBTC} (voltage offset bottom temperature coefficient) is the dependence of V_{OB} with temperature.
- V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
- V_{OTTC} (voltage offset top temperature coefficient) is the dependence of V_{OT} with temperature.

7. Output data acquisition

- Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
- Output data is fully stable during the low level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; V_{RB} = –3.0 V; V_{RT} = -0.6 V and V_{VI} referenced to AGND)

STEP	V_{VI}	O/UF	BINARY OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
underflow	<–2.789	1	0	0	0	0	0	0	0	0
0	–2.783	0	0	0	0	0	0	0	0	0
1	–2.775	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0
255	–0.774	0	1	1	1	1	1	1	1	1
overflow	>–0.770	1	1	1	1	1	1	1	1	1

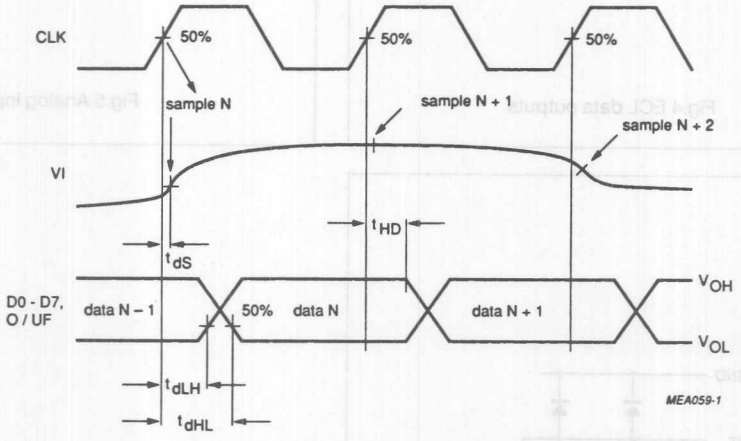


Fig.3 Timing diagram.

INTERNAL PIN CONFIGURATIONS

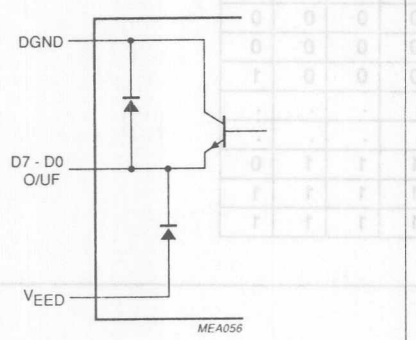


Fig.4 ECL data outputs

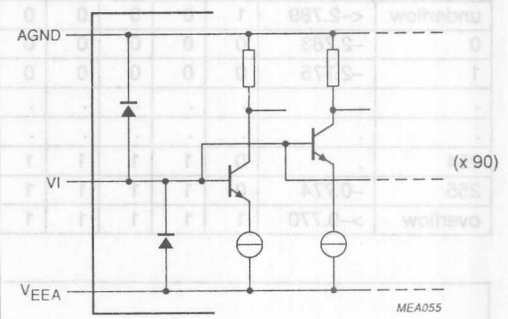


Fig.5 Analog input

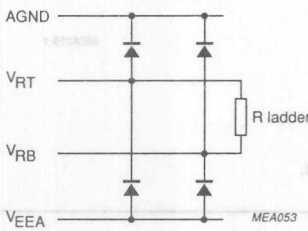


Fig.6 V_{RT} and V_{RB} inputs

APPLICATION INFORMATION

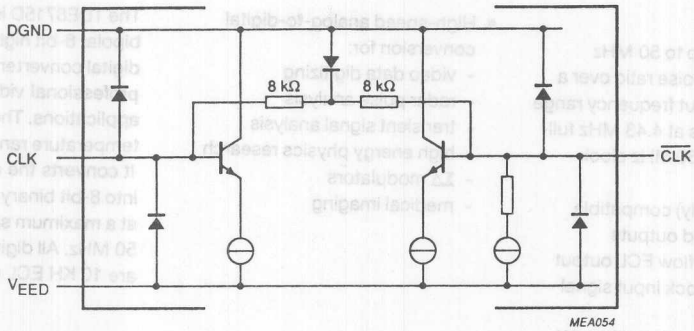


Fig.7 CLK and $\overline{CLK}$ input

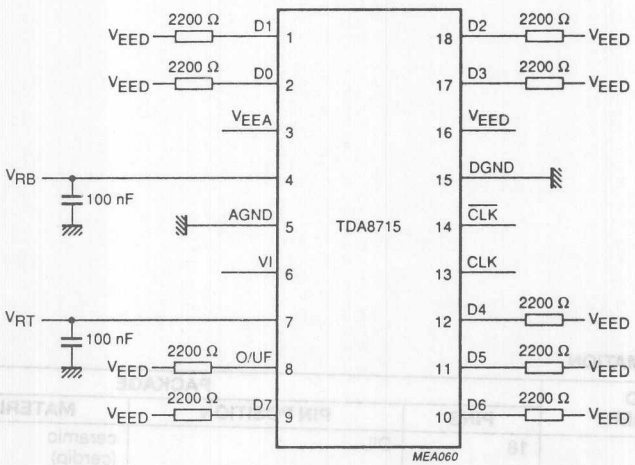


Fig.8 Application diagram.

Notes to Fig.8

- All resistors have a value of 2.2 kΩ; all capacitors have a value of 100 nF
- Analog and digital supplies should be separated and decoupled.
- The external voltage regulator must be build in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.
- $V_{EEA} = V_{EED} = -5.2$ V; $V_{RB} = -3.0$ V; $V_{RT} = -0.6$ V.

8-bit high-speed analog-to-digital converter (Mil. temp.) TDE8715D

FEATURES

- 8-bit resolution
- Sampling rate up to 50 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.5 effective bits at 4.43 MHz full-scale input at a 50 MHz clock frequency)
- ECL (10KH family) compatible digital inputs and outputs
- Overflow/underflow ECL output
- Low-level AC clock input signal allowed
- Power dissipation only 325 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - video data digitizing
  - radar pulse analysis
  - transient signal analysis
  - high energy physics research
  - $\Sigma\Delta$ modulators
  - medical imaging

DESCRIPTION

The TDE8715D is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for professional video and other applications. The operating temperature range is 55 °C up to 125 °C. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 50 MHz. All digital inputs and outputs are 10 KH ECL compatible.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDE8715D	18	DIL	ceramic (cerdip)	SOT 133BH3

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EEA}	analog supply voltage		–4.95	–5.2	–5.45	V
V_{EED}	digital supply voltage		–4.95	–5.2	–5.45	V
I_{EEA}	analog supply current		-	20	25	mA
I_{EED}	digital supply current	see note	-	52	60	mA
ILE	DC integral linearity error		-	± 0.4	± 0.75	LSB
DLE	DC differential linearity error		-	± 0.25	± 0.5	LSB
EB	effective bits (f_i = 4.43 MHz)	f_{CLK} = 50 MHz	-	7.2	-	bits
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
T_{amb}	operating ambient temperature range		–55	-	+125	°C
P_{tot}	total power dissipation	see note	-	325	425	mW

Note to the Quick Reference Data

All digital outputs connected to V_{EED} via 2.2 kΩ resistors.

8-bit high-speed analog-to-digital converter (Mil. temp.) TDE8715D

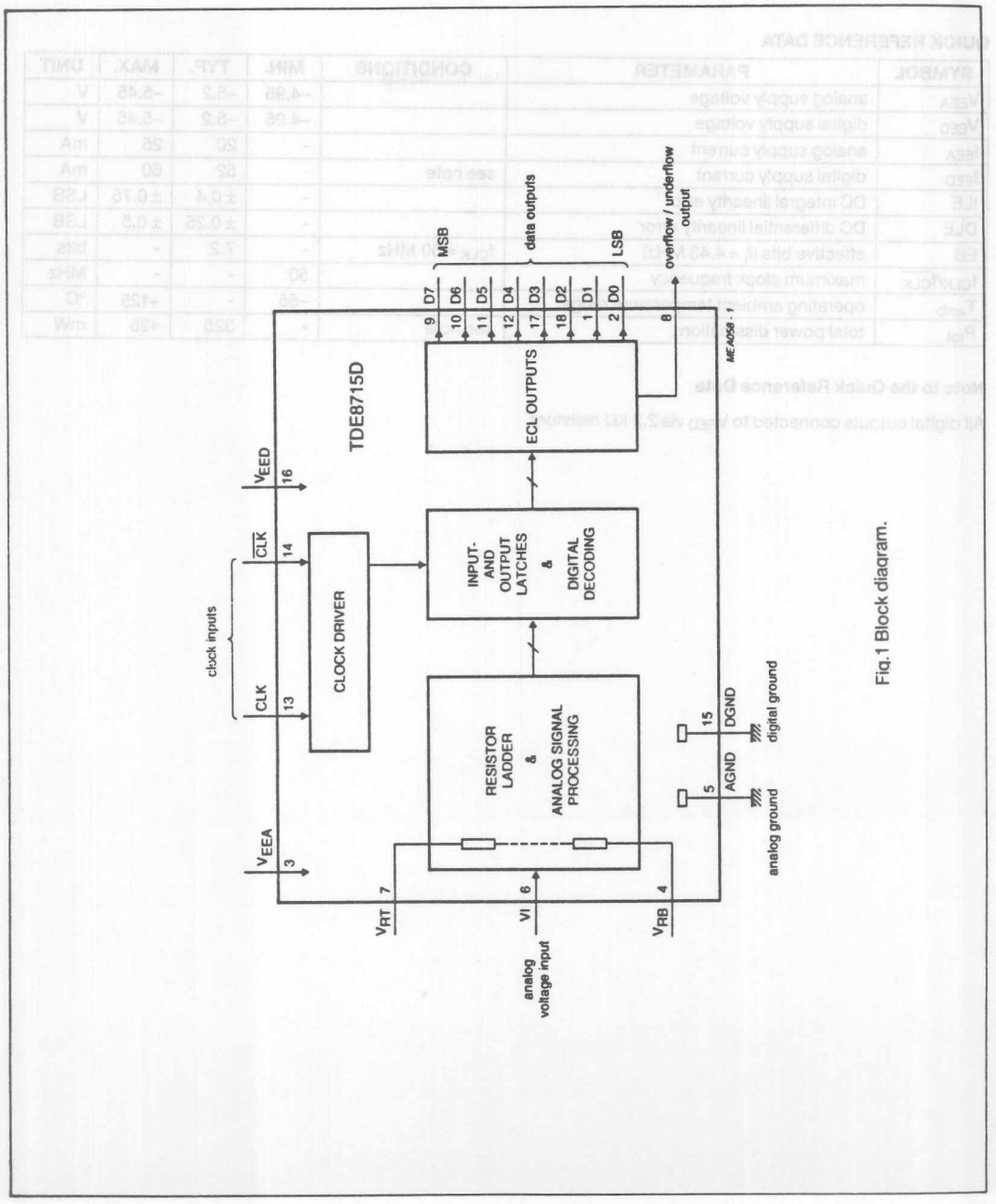


Fig.1 Block diagram.

8-bit high-speed analog-to-digital converter (Mil. temp.) TDE8715D

PIN CONFIGURATION

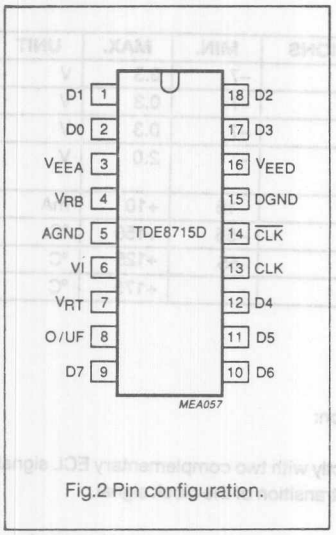


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
V_{EEA}	3	analog negative supply voltage (−5.2 V)
V_{RB}	4	reference voltage bottom input
AGND	5	analog ground
VI	6	analog voltage input
V_{RT}	7	reference voltage top input
O/UF	8	overflow/underflow data output
D7	9	data output, bit 7(MSB)
D6	10	data output, bit 6
D5	11	data output, bit 5
D4	12	data output, bit 4
CLK	13	clock input
$\overline{CLK}$	14	complementary clock input
DGND	15	digital ground
V_{EED}	16	digital negative supply voltage (−5.2 V)
D3	17	data output, bit 3
D2	18	data output, bit 2

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EEA}	analog supply voltage range		−7	0.3	V
V_{EED}	digital supply voltage range		−7	0.3	V
V_{VI}	input voltage range		−7	0.3	V
$V_{\overline{CLK}}$/ V_{CLK}	AC input voltage for switching (peak-to-peak value)	see note	-	2.0	V
I_O	output current		−15	+10	mA
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		-55	+125	°C
T_j	junction temperature		-	+175	°C

Note to the Ratings

The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of −1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- When driving the CLK input with a ECL signal only (Asymmetrical drive modes), it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT133BH3	+75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{EEA} = V_3 - V_5 = -4.95$ V to -5.45 V; $V_{EED} = V_{16} - V_{15} = -4.95$ V to -5.45 V; AGND and DGND shorted together; $T_{amb} = -55$ °C to $+125$ °C; unless otherwise specified (typical values measured at $V_{EEA} = -5.2$V; $V_{EED} = -5.2$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{EEA}	analog supply voltage		–4.95	–5.2	–5.45	V
V_{EED}	digital supply voltage		–4.95	–5.2	–5.45	V
I_{EEA}	analog supply current		-	20	25	mA
I_{EED}	digital supply current	note 5	-	52	60	mA
ΔV_{EE}	supply voltage difference V_{EEA} - V_{EED}		–0.5	0	+0.5	V
Reference voltages for the resistor ladder						
V_{RB}	reference voltage LOW		–3.4	–3.1	–2.8	V
V_{RT}	reference voltage HIGH		–1.0	–0.6	–0.4	V
V_{ref}	differential reference voltage V_{RT}-V_{RB}		2.4	2.5	-	V
I_{ref}	reference current		-	12.6	-	mA
R_{LAD}	resistor ladder		-	200	-	Ω
R_{TLC}	temperature coefficient of the ladder		-	0.24	-	Ω/°C
V_{OB}	voltage offset bottom	note 6	-	317	-	mV
V_{OBTC}	voltage offset bottom temperature coefficient	note 6	-	0.1	-	mV/°C
V_{OT}	voltage offset top	note 6	-	174	-	mV
V_{OTTC}	voltage offset top temperature coefficient	note 6	-	–0.3	-	mV/°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs CLOCK INPUT CLK (note 1)						
V_{IL}	input voltage LOW		−1.85	−1.77	−1.65	V
V_{IH}	input voltage HIGH		−0.96	−0.88	−0.81	V
I_{IL}	input current LOW	V_{CLK} = −1.77 V	-	−240	-	µA
I_{IH}	input current HIGH	V_{CLK} = −0.88 V	-	−14	-	µA
R_i	input resistance	f_{CLK} = 10 MHz	-	7.0	-	kΩ
		f_{CLK} = 50 MHz	-	3.5	-	kΩ
C_i	input capacitance	f_{CLK} = 10 MHz	-	1.8	-	pF
		f_{CLK} = 50 MHz	-	1.55	-	pF
CLOCK INPUT $\overline{CLK}$ (note 1)						
V_{IL}	input voltage LOW		−1.85	−1.77	−1.65	V
V_{IH}	input voltage HIGH		−0.96	−0.88	−0.81	V
I_{IL}	input current LOW	$V_{\overline{CLK}}$ = −1.77 V	-	−140	-	µA
I_{IH}	input current HIGH	$V_{\overline{CLK}}$ = −0.88 V	-	75	-	µA
R_i	input resistance	$f_{\overline{CLK}}$ = 10 MHz	-	9.3	-	kΩ
		$f_{\overline{CLK}}$ = 50 MHz	-	4.5	-	kΩ
C_i	input capacitance	$f_{\overline{CLK}}$ = 10 MHz	-	2.6	-	pF
		$f_{\overline{CLK}}$ = 50 MHz	-	2.4	-	pF
$V_{\underline{CLK}(p\text{-}p)}$ − $V_{CLK(p\text{-}p)}$	AC input voltage for switching (peak-to-peak value)		0.5	0.9	1.1	V
VI (analog input with V_{RB} = −3.1 V and V_{RT} = −0.6 V)						
I_{IL}	input current LOW	data output 00	-	0	-	µA
I_{IH}	input current HIGH	data output FF	-	120	-	µA
R_i	input resistance	f_i = 1 MHz	-	9.4	-	kΩ
C_i	input capacitance	f_i = 1 MHz	-	13.7	20	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs DIGITAL OUTPUTS (D7 - D0 and 0/UF) (Digital 10KH ECL outputs)						
V_{OL}	output voltage LOW	T_{amb} = 25 °C	−1.9	−1.77	−1.65	V
V_{OH}	output voltage HIGH	T_{amb} = 25 °C	−0.96	−0.88	−0.81	V
I_{OL}	output current LOW		-	1.8	4	mA
I_{OH}	output current HIGH		-	1.8	4	mA
Switching characteristics						
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		50	-	-	MHz
Analog signal processing (f_{CLK} = 50 MHz)						
B	−3 dB bandwidth	note 2	-	20.5	-	MHz
G_d	differential gain	note 3	-	0.3	2.0	%
ϕ_d	differential phase	note 3	-	0.4	1.5	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	0	0	0	dB
F_{even}	even harmonics (full-scale)	f_i = 4.43 MHz	-	−60	-	dB
F_{odd}	odd harmonics (full-scale)	f_i = 4.43 MHz	-	−50	-	dB
Transfer function (f_{CLK} = 50 MHz)						
ILE	DC integral linearity error		-	-	± 0.75	LSB
DLE	DC differential linearity error		-	-	± 0.5	LSB
AILE	AC integral linearity error	note 4	-	± 0.75	-	LSB
EB	effective bits f_i = 600 kHz	f_{CLK} = 20 MHz	-	7.8	-	bits
EB	effective bits f_i = 4.43 MHz	f_{CLK} = 50 MHz	-	7.2	-	bits
EB	effective bits f_i = 7 MHz	f_{CLK} = 50 MHz	-	6.9	-	bits
Timing (note 7; see Fig. 3)						
t_{dS}	sampling delay		-	1	3	ns
t_{HD}	output hold time		3	4	-	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	4	5	8	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	6	7	10	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are two modes of operation:

- Differential drive modes; When driving the CLK input and the $\overline{CLK}$ input directly with two complementary ECL signals imposed on a DC level of –1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- Asymmetrical drive modes; When driving the CLK input directly with a ECL signal or a sinewave signal imposed on a DC level of –1.3 V, sampling takes place on the LOW-to-HIGH transition of the clock signal.
- When driving the CLK input with a ECL signal only (Asymmetrical drive modes) , it is recommended to decouple the $\overline{CLK}$ input to DGND with a capacitor and connected to V_{EED} by a 150 kΩ resistor.

2. The –3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).

3. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VI(p-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.

4. Full-scale sinewave (f_i = 4.43 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 50 MHz).

5. All digital outputs connected to V_{EED} via 2.2 kΩ resistors.

6. Analog input voltages producing code 00 up to and including FF

- V_{OB} (voltage offset bottom) is the difference between the analog input which produces data equal to 00 and the reference voltage bottom (V_{RB}) at T_{amb} = 25 °C.
- V_{OBTC} (voltage offset bottom temperature coefficient) is the dependence of V_{OB} with temperature.
- V_{OT} (voltage offset top) is the difference between V_{RT} (reference voltage top) and the analog input which produces data outputs equal to FF, at T_{amb} = 25 °C.
- V_{OTTC} (voltage offset top temperature coefficient) is the dependence of V_{OT} with temperature.

7. Output data acquisition

- Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
- Output data is fully stable during the low level of the clock. Thus it is recommended that acquisition of this data is made after the falling edge of the clock, instead of after the maximum (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; V_{RB} = –3.1 V; V_{RT} = –0.6 V and V_{VI} referenced to AGND)

STEP	V_{VI}	O/UF	BINARY OUTPUT BITS							
			D7	D6	D5	D4	D3	D2	D1	D0
underflow	<–2.789	1	0	0	0	0	0	0	0	0
0	–2.783	0	0	0	0	0	0	0	0	0
1	–2.775	0	0	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0
255	–0.774	0	1	1	1	1	1	1	1	1
overflow	>–0.770	1	1	1	1	1	1	1	1	1

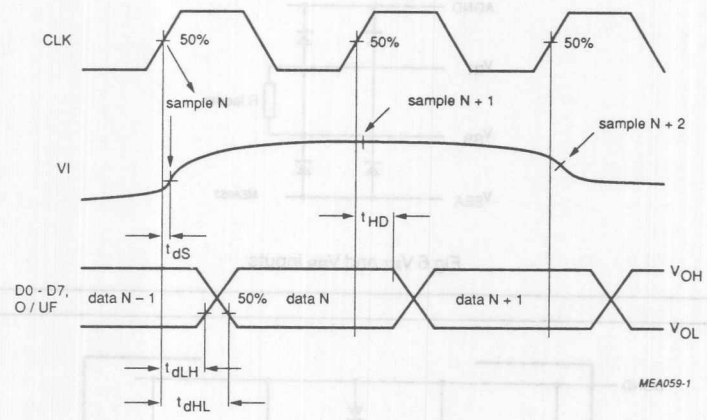


Fig.3 Timing diagram.

INTERNAL PIN CONFIGURATIONS

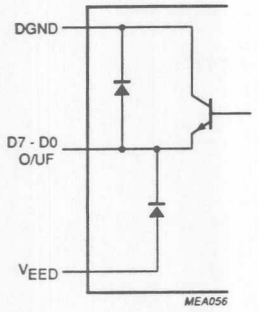


Fig.4 ECL data outputs

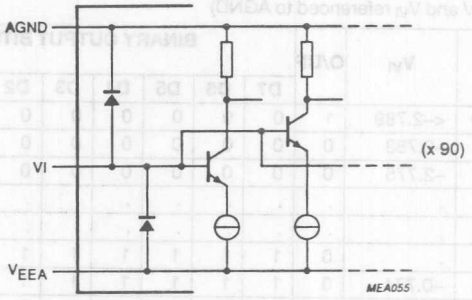


Fig.5 Analog input

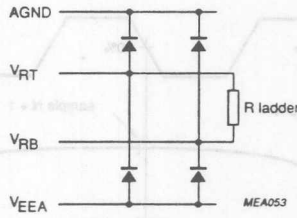


Fig.6 V_{RT} and V_{RB} inputs

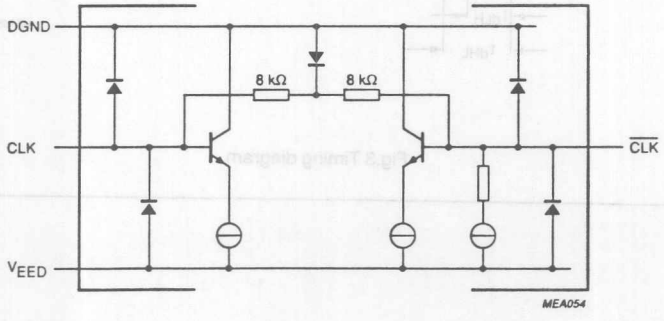


Fig.7 CLK and $\overline{CLK}$ input

APPLICATION INFORMATION

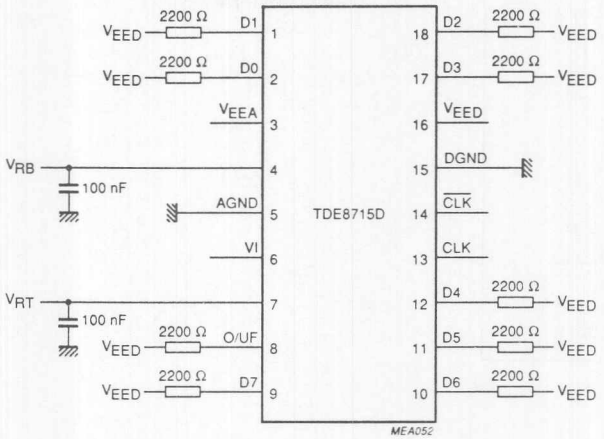


Fig.8 Application diagram.

Notes to Fig.8

- All resistors have a value of 2.2 kΩ; all capacitors have a value of 100 nF
- Analog and digital supplies should be separated and decoupled.
- The external voltage regulator must be build in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.
- $V_{EEA} = V_{EED} = -5.2$ V; $V_{RB} = -3.1$ V; $V_{RT} = -0.6$ V.

APPLICATION INFORMATION

Fig.8 Application diagram.

Notes to Fig.8

- All resistors have a value of 2.2 kΩ; all capacitors have a value of 100 nF.
- Analog and digital supplies should be separated and decoupled.
- The external voltage regulator must be built in such a way that a good supply voltage ripple rejection is achieved with respect to the LSB value.
- $V_{EEA} = V_{EED} = -5.2$ V; $V_{RB} = -3.1$ V; $V_{RT} = -0.8$ V.

Section 10
Digital-to-Analog Converters

General Purpose/Linear ICs

INDEX

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DAC08 Series	8-Bit high-speed multiplying D/A converter	517
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Absolute Accuracy Error

Absolute Accuracy Error of a DAC at an input code is the difference between the theoretical output voltage/current at a digital input code and the actual analog output voltage/current produced at the same code.

Absolute Accuracy Error includes gain error, offset error and relative accuracy error and is typically expressed in LSBs or in percent of full-scale range (FSR).

Differential Linearity Error

Differential Linearity Error of a DAC is the difference between the actual step size between any two adjacent codes and the ideal step size (which is equal to 1 LSB of the DAC). A differential linearity error of greater than 1 LSB can lead to non-monotonicity.

Digital Feedthrough

The amount of digital energy at the digital inputs that appear at the DAC output.

Full-Scale Range (FSR)

The Full-Scale Range (FSR) of a DAC is the scale factor that determines the nominal conversion relationship; e.g., 10V span for a full-scale code change in a fixed reference converter.

In a unipolar DAC of n bits, the output voltage/current is 0V/mA with all bits OFF. With all bits turned ON, the output voltage/current is FSR x $(1-2^{-N})$.

In a bipolar DAC, the output voltage/current is –FSR/2 with all bits OFF. With all bits turned ON, the output voltage/current is FSR x $(1-2^{-(N-1)})$.

Glitch

The transition spike that occurs at the output of a DAC. When the digital input code changes, not all input switches change at precisely the same time, leading to either positive or negative spikes when the input code changes. The energy in these "glitches" is proportional to the area under the glitch; hence, we generally refer to "glitch energy" as the area under the glitch in nV – seconds or LSB – seconds. The largest glitch tends to occur at the transition from the code where the MSB is a logic low with all other bits a logic high to the 1's complement of this word.

Integral Non-Linearity

Same as Relative Accuracy.

Least Significant Bit

The Least Significant Bit (LSB) is the lowest-order bit and carries the smallest weight. In an n-bit DAC, the weight of the LSB is FSR/(2^N-1). It is the smallest discrete step that can be attained in the output of the DAC.

Monotonicity

A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases from any code to the next higher code.

Most Significant Bit

The Most Significant Bit (MSB) is the highest order bit and carries the most weight. The weight of the MSB is 1/2 the FSR of the DAC.

Offset Error (Unipolar and Bipolar)

In a DAC, unipolar offset is the actual analog output voltage/current with all the bits turned OFF. Offset Error causes a shift in the transfer characteristic of the DAC. Similarly for bipolar offset, it is the actual output voltage/current with the digital input at half-scale.

Output Voltage Compliance

For a current output DAC, the maximum range of output voltage for which the output current will be within specifications.

Power Supply Sensitivity

The Power Supply Sensitivity of a DAC is the change in the DAC output with changes in the DC power supply voltages. It is usually expressed in LSBs/V or in %FSR/V.

Relative Accuracy

Relative Accuracy Error is the deviation of the DACs actual output voltage/current from the ideal output voltage/current on a straight line connecting the end points of the transfer characteristic after nulling offset error and gain error. It is generally expressed in LSBs or in %FSR.

Resolution

Resolution of a DAC is the number of bits at its input. The number of discrete output levels is 2^N where N is the resolution of the converter.

Settling Time

The time required, following a prescribed change in the digital inputs, for the output of the DAC to reach and remain within a specified fraction (typically ±1/2 LSB) of its final value. This parameter is usually specified for a full-scale change.

Temperature Coefficients

In general, Temperature Coefficients are expressed either in ppm/°C or in LSBs/°C or as a change in the specified parameter over the temperature range. Measurements are usually made at room temperature and at the temperature extremes of the specified temperature range; the Temperature Coefficient is defined as the change in the parameter from its room temperature value divided by the corresponding temperature change.

DESCRIPTION

The DAC08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 70ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 20-to-1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All DAC08 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 37mW power consumption attainable at ±5V supplies.

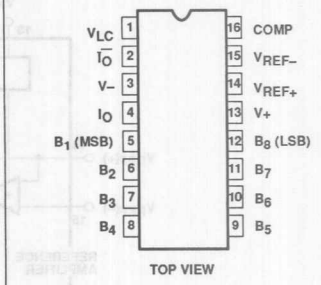
The compact size and low power consumption make the DAC08 attractive for portable and military aerospace applications.

FEATURES

- Fast settling output current—70ns
- Full-scale current prematched to ±1 LSB
- Direct interface to TTL, CMOS, ECL, HTL, PMOS
- Relative accuracy to 0.1% maximum over temperature range
- High output compliance -10V to +18V
- True and complemented outputs
- Wide range multiplying capability
- Low FS current drift — ±10ppm/°C
- Wide power supply range—±4.5V to ±18V
- Low power consumption—37mW at ±5V

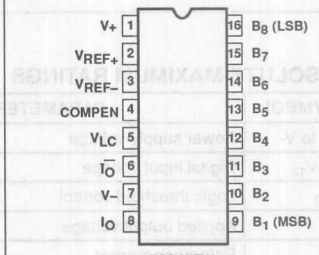
PIN CONFIGURATIONS

F, N Packages



TOP VIEW

D[1] Package



TOP VIEW

NOTE:
1. SO and non-standard pinouts.

APPLICATIONS

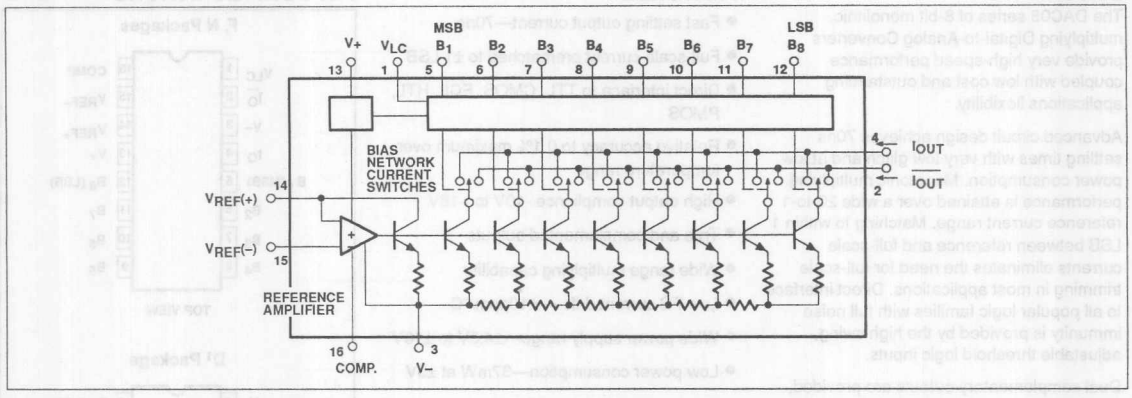
- 8-bit, 1µs A-to-D converters
- Servo-motor and pen drivers
- Waveform generators
- Audio encoders and attenuators
- Analog meter drivers
- Programmable power supplies
- CRT display drivers
- High-speed modems
- Other applications where low cost, high speed and complete input/output versatility are required
- Programmable gain and attentuation
- Analog-Digital multiplication

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Hermetic Cerdip	-55°C to +125°C	DAC08F
16-Pin Hermetic Cerdip	-55°C to +125°C	DAC08AF
16-Pin Plastic DIP	0 to +70°C	DAC08CN
16-Pin Hermetic Cerdip	0 to +70°C	DAC08CF
16-Pin Plastic DIP	0 to +70°C	DAC08EN
16-Pin Hermetic Cerdip	0 to +70°C	DAC08EF
16-Pin Plastic SO	0 to +70°C	DAC08ED
16-Pin Plastic DIP	0 to +70°C	DAC08HN

8-Bit high-speed multiplying D/A converter DAC08 Series

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V+ to V-	Power supply voltage	36	V
V_5-V_{12}	Digital input voltage	V- to V- plus 36V	
V_{LC}	Logic threshold control	V- to V+	
V_0	Applied output voltage	V- to +18	V
I_{14}	Reference current	5.0	mA
V_{14}, V_{15}	Reference amplifier inputs	V_{EE} to V_{CC}	
P_D	Maximum power dissipation T_A=25°C (still-air)[1]		
	F package	1190	mW
	N package	1450	mW
	D package	1090	mW
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C
T_A	Operating temperature range		
	DAC08, DAC08A	-55 to +125	°C
	DAC08C, E, H	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.6mW/°C
   D package at 8.7mW/°C

DC ELECTRICAL CHARACTERISTICS

Pin 3 must be at least 3V more negative than the potential to which R_{15} is returned. V_{CC}=±15V, I_{REF}=2.0mA. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$ unless otherwise noted. DAC08C, E, H: T_A=0°C to 70°C DAC08/08A: T_A=-55°C to 125°C

SYMBOL	PARAMETER	TEST CONDITIONS	DAC08C			DAC08E DAC08			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy	Over temperature range			±0.39			±0.19	%FS
	Differential non-linearity				±0.78			±0.39	%FS
TCI_{FS}	Full-scale tempco			±10			±10		ppm/°C
V_{OC}	Output voltage compliance	Full-scale current change< 1/2LSB	-10		+18	-10		+18	V
I_{FS4}	Full-scale current	V_{REF}=10.000V, R_{14}, R_{15}=5.000kΩ	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FSS}	Full-scale symmetry	I_{FS4}-I_{FS2}		±2.0	±16		±1.0	±8.0	µA
I_{ZS}	Zero-scale current			0.2	4.0		0.2	2.0	µA
I_{FSR}	Full-scale output current range	R_{14}, R_{15}=5.000kΩ V_{REF}=+15.0V, V-=-10V V_{REF}=+25.0V, V-=-12V	2.1 4.2			2.1 4.2			mA
V_{IL} V_{IH}	Logic input levels Low High	V_{LC}=0V	2.0		0.8	2.0		0.8	V
I_{IL} I_{IH}	Logic input current Low High	V_{LC}=0V V_{IN}=-10V to +0.8V V_{IN}=2.0V to 18V		-2.0 0.002	-10 10		-2.0 0.002	-10 10	µA
V_{IS}	Logic input swing	V-=-15V	-10		+18	-10		+18	V
V_{THR}	Logic threshold range	V_S=±15V	-10		+13.5	-10		+13.5	V
I_{15}	Reference bias current			-1.0	-3.0		-1.0	-3.0	µA
dI/dt	Reference input slew rate		4.0	8.0		4.0	8.0		mA/µs
$PSSI_{FS+}$	Power supply sensitivity Positive	I_{REF}=1mA V+=4.5 to 5.5V, V-=-15V; V+=13.5 to 16.5V, V-=-15V		0.0003	0.01		0.0003	0.01	%FS/%VS
PSI_{FS-}	Negative	V-=-4.5 to -5.5V, V+=+15V; V-=-13.5 to -16.5, V+=+15V		0.002	0.01		0.002	0.01	
I+ I-	Power supply current Positive Negative	V_S=±5V, I_{REF}=1.0mA		3.1 -4.3	3.8 -5.8		3.1 -4.3	3.8 -5.8	mA
I+ I-	Positive Negative	V_S=+5V, -15V, I_{REF}=2.0mA		3.1 -7.1	3.8 -7.8		3.1 -7.1	3.8 -7.8	
I+ I-	Positive Negative	V_S=±15V, I_{REF}=2.0mA		3.2 -7.2	3.8 -7.8		3.2 -7.2	3.8 -7.8	
P_D	Power dissipation	±5V, I_{REF}=1.0mA +5V, -15V, I_{REF}=2.0mA ±15V, I_{REF}=2.0mA		37 122 156	48 136 174		37 122 156	48 136 174	mW

DC ELECTRICAL CHARACTERISTICS (Continued)

Pin 3 must be at least 3V more negative than the potential to which R15 is returned. V_{CC} = +15V, I_{REF} = 2.0mA, Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$, unless otherwise noted. DAC08C, E, H: T_A = 0°C to 70°C. DAC08/08A: T_A = -55°C to 125°C.

SYMBOL	PARAMETER	TEST CONDITIONS	DAC08H DAC08A			UNIT
			Min	Typ	Max	
	Resolution		8	8	8	Bits
	Monotonicity		8	8	8	Bits
	Relative accuracy	Over temperature range			±0.1	%FS
	Differential non-linearity				±0.19	%FS
TCI_{FS}	Full-scale tempco			±10	±50	ppm/°C
V_{OC}	Output voltage compliance	Full-scale current change LSB	-10		+18	V
I_{FS4}	Full-scale current	V_{REF}=10.000V, R_{14}, R_{15}=5.000kΩ	1.984	1.992	2.000	mA
I_{FSS}	Full-scale symmetry	I_{FS4}-I_{FS2}		±1.0	±4.0	µA
I_{ZS}	Zero-scale current			0.2	1.0	µA
I_{FSR}	Full-scale output current range	R_{14}, R_{15}=5.000kΩ V_{REF}=+15.0V, V-=-10V V_{REF}=+25.0V, V-=-12V	 2.1 4.2			mA
	Logic input levels					
V_{IL}	Low	V_{LC}=0V			0.8	V
V_{IH}	High		2.0			
	Logic input current	V_{LC}=0V				
I_{IL}	Low	V_{IN}=-10V to +0.8V		-2.0	-10	µA
I_{IH}	High	V_{IN}=2.0V to 18V		0.002	10	
V_{IS}	Logic input swing	V-=-15V	-10		+18	V
V_{THR}	Logic threshold range	V_S=±15V	-10		+13.5	V
I_{15}	Reference bias current			-1.0	-3.0	µA
dI/dt	Reference input slew rate		4.0	8.0		mA/µs
	Power supply sensitivity	I_{REF}=1mA				
$PSSI_{FS+}$	Positive	V+=4.5 to 5.5V, V-=-15V;		0.0003	0.01	
		V+=13.5 to 16.5V, V-=-15V				%FS/%VS
PSI_{FS-}	Negative	V-=-4.5 to -5.5V, V+=+15V;		0.002	0.01	
		V-=-13.5 to -16.5, V+=+15V				
	Power supply current					
I+	Positive	V_S=±5V, I_{REF}=1.0mA		3.1	3.8	
I-	Negative			-4.3	-5.8	
I+	Positive	V_S=+5V, -15V, I_{REF}=2.0mA		3.1	3.8	mA
I-	Negative			-7.1	-7.8	
I+	Positive	V_S=±15V, I_{REF}=2.0mA		3.2	3.8	
I-	Negative			-7.2	-7.8	
P_D	Power dissipation	±5V, I_{REF}=1.0mA		37	48	
		+5V, -15V, I_{REF}=2.0mA		122	136	mW
		±15V, I_{REF}=2.0mA		156	174	

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	DAC08C			DAC08E DAC08			DAC08H DAC08A			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_S	Settling time	To ± LSB, all bits switched on or off, T_A=25°C		70	135		70	135		70	135	ns
	Propagation delay											
t_{PLH}	Low-to-High	T_A=25°C, each bit.										ns
t_{PHL}	High-to-Low	All bits switched		35	60		35	60		35	60	

TEST CIRCUITS

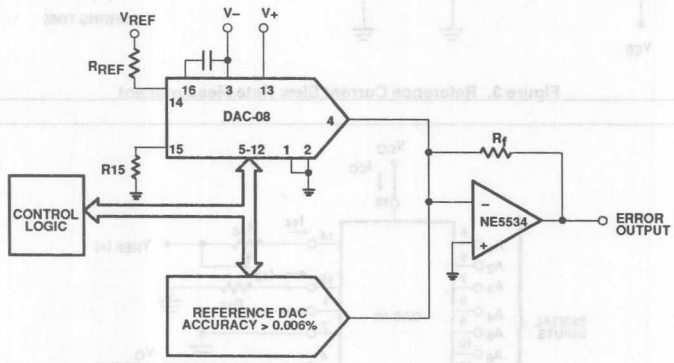


Figure 1. Relative Accuracy Test Circuit

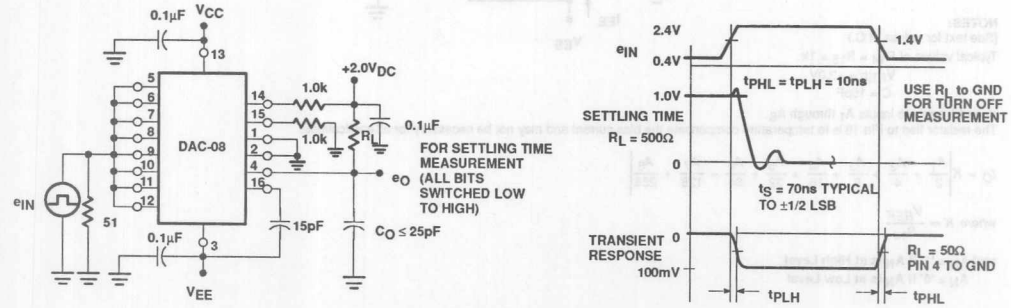


Figure 2. Transient Response and Settling Time

TEST CIRCUITS (Continued)

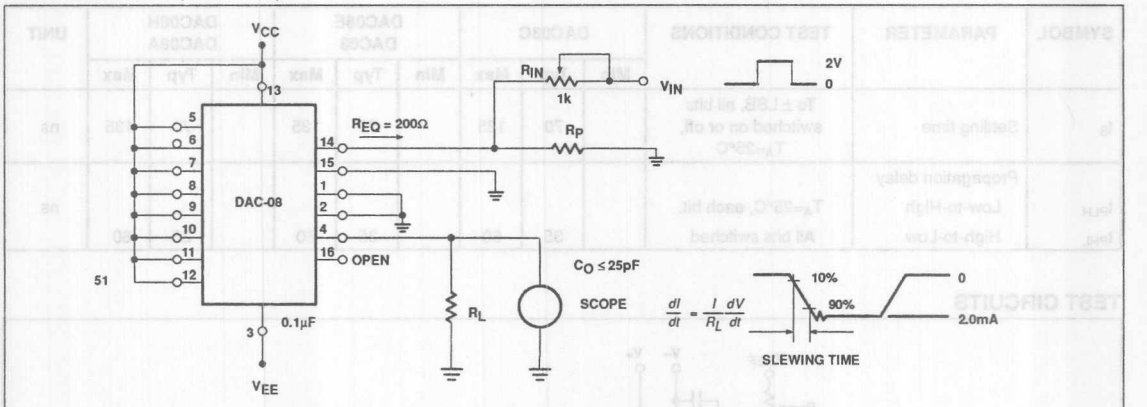
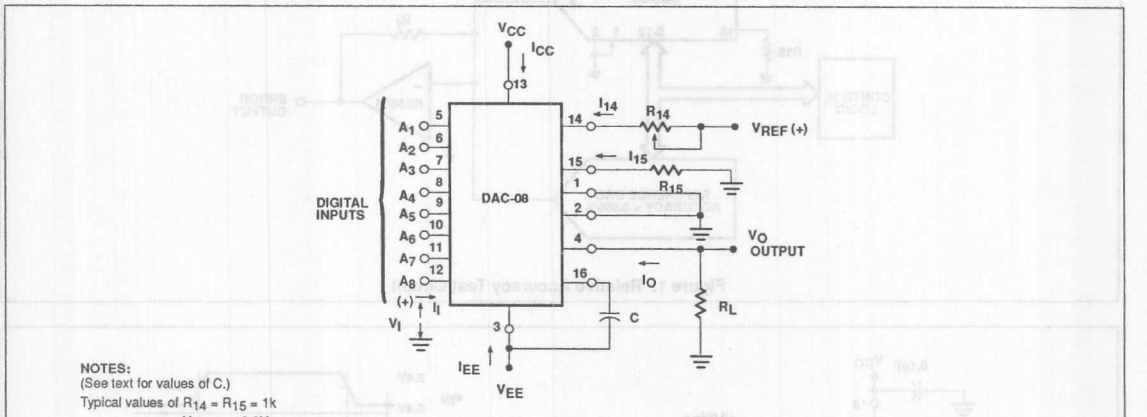


Figure 3. Reference Current Slew Rate Measurement



NOTES:
(See text for values of C.)
Typical values of $R_{14} = R_{15} = 1k$
$V_{REF} = +2.0V$
$C = 15pF$

V_I and I_I apply to inputs A_1 through A_8
The resistor tied to Pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left|\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256}\right|$$

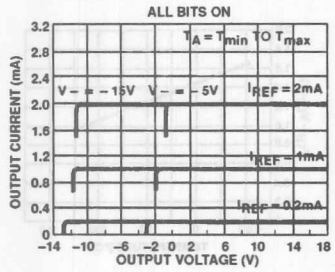
where $K \approx \frac{V_{REF}}{R_{14}}$

and A_N = '1' if A_N is at High Level
A_N = '0' if A_N is at Low Level

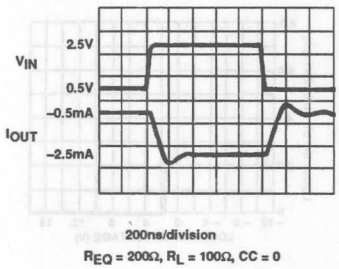
Figure 4. Notation Definitions

TYPICAL PERFORMANCE CHARACTERISTICS

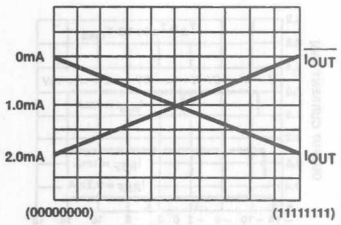
Output Current vs Output Voltage (Output Voltage Compliance)



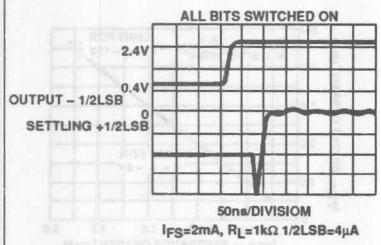
Fast Pulsed Reference Operation



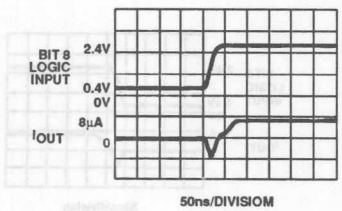
True and Complementary Output Operation



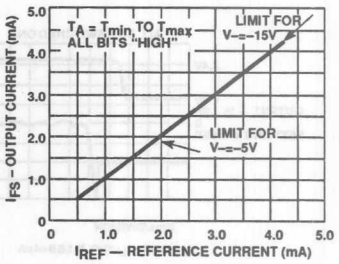
Full-Scale Settling Time



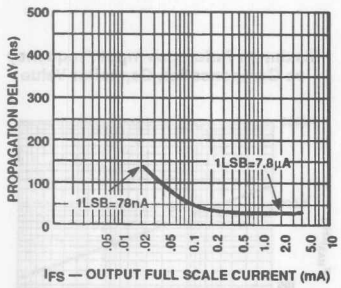
LSB Switching



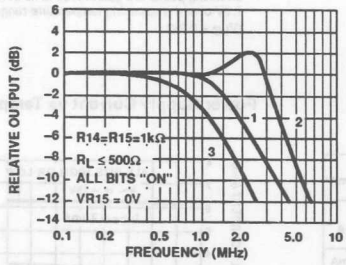
Full-Scale Current vs Reference Current



LSB Propagation Delay vs IFS



Reference Input Frequency Response

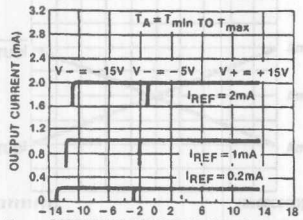


NOTES:

Curve 1: CC = 15pF, V_{IN} = 2.0V_{P-P} centered at +1.0V
Curve 1: CC = 15pF, V_{IN} = 5m0V_{P-P} centered at +200mV
Curve 1: CC = 15pF, V_{IN} = 100m0V_{P-P} centered at 0V and applied through 50Ω connected to Pin 14. +2.0V applied to R_{14}.

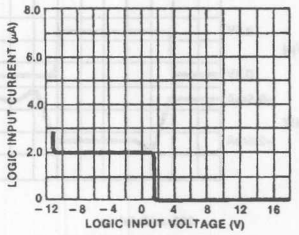
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Reference AMP Common-Mode Range All Bits On

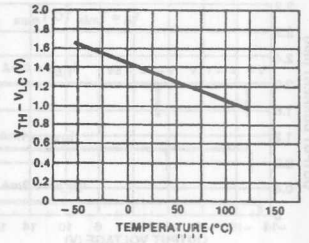


POSITIVE COMMON-MODE RANGE IS ALWAYS (V+) -1.5V.

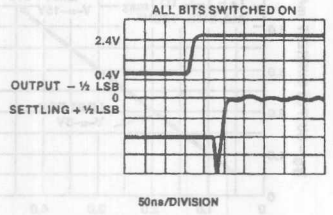
Logic Input Current vs Input Voltage



$V_{TH} - V_{LC}$ vs Temperature

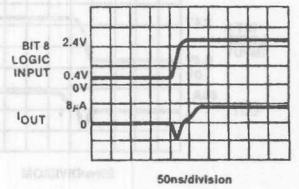


Output Voltage Compliance vs Temperature

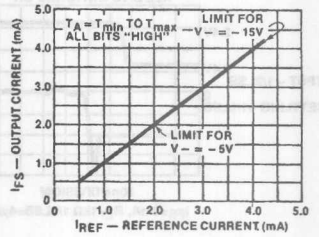


I_{FS}=2mA, R_L=1kΩ ½ LSB=4μA

Bit Transfer Characteristics



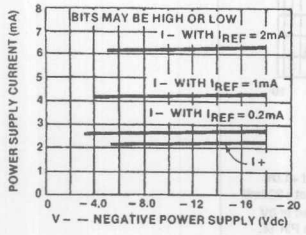
Power Supply Current vs V+



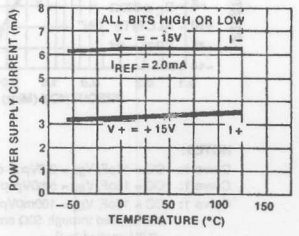
NOTES:

B_1 through B_8 have identical transfer characteristics. Bits are fully switched, with less than 1/2LSB error, at less than ±100mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2.0V over the operating temperature range (V_{LC} = 0.0V).

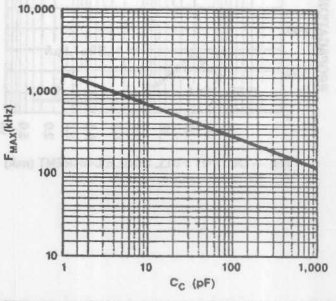
Power Supply Current vs V−



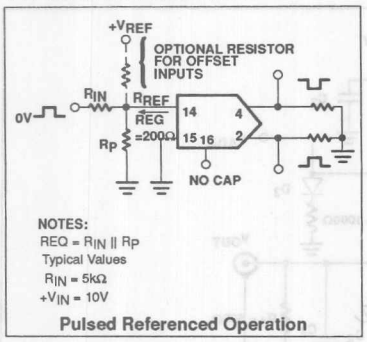
Power Supply Current vs Temperature



Maximum Reference Input Frequency vs Compensation Capacitor Value



TYPICAL APPLICATION



Pulsed Referenced Operation

FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier input current must always flow into Pin 14 regardless of the setup method or reference supply voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full reference current. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. R_{15} may be eliminated with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased as R_{14} value is increased. This is in order to maintain proper phase margin. For R_{14} values of 1.0, 2.5, and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF, respectively. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection. (Fluctuations in the negative supply have more effect on accuracy than do any changes in the positive supply.)

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at Pin 15.

When using a DC reference voltage, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage, but if a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be formed of two series resistors with the junction of the two resistors bypassed with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods applies and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage at Pin 4 must always be at least 4.5V more positive than the voltage of the negative supply (Pin 3) when the reference current is 2mA or less, and at least 8V more positive than the negative supply when the reference current is between 2mA and 4mA. This is necessary to avoid saturation of the output transistors, which would cause serious accuracy degradation.

Output Current Range

Any time the full-scale current exceeds 2mA, the negative supply must be at least 8V more negative than the output voltage. This is due to the increased internal voltage drops between the negative supply and the outputs with higher reference currents.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy, full-scale accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current after zero-scale current has been nulled out. The relative accuracy of the DAC08 series is essentially constant over the operating temperature range due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC08 series has a very low full-scale current drift over the operating temperature range.

The DAC08 series is guaranteed accurate to within ± LSB at +25°C at a full-scale output current of 1.992mA. The relative accuracy test circuit is shown in Figure 1. The 12-bit converter is calibrated to a full-scale output current of 1.99219mA, then the DAC08 full-scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on the oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total of ± part in 65,536, or ±0.00076%, which is much more accurate than the ±0.19% specification of the DAC08 series.

Monotonicity

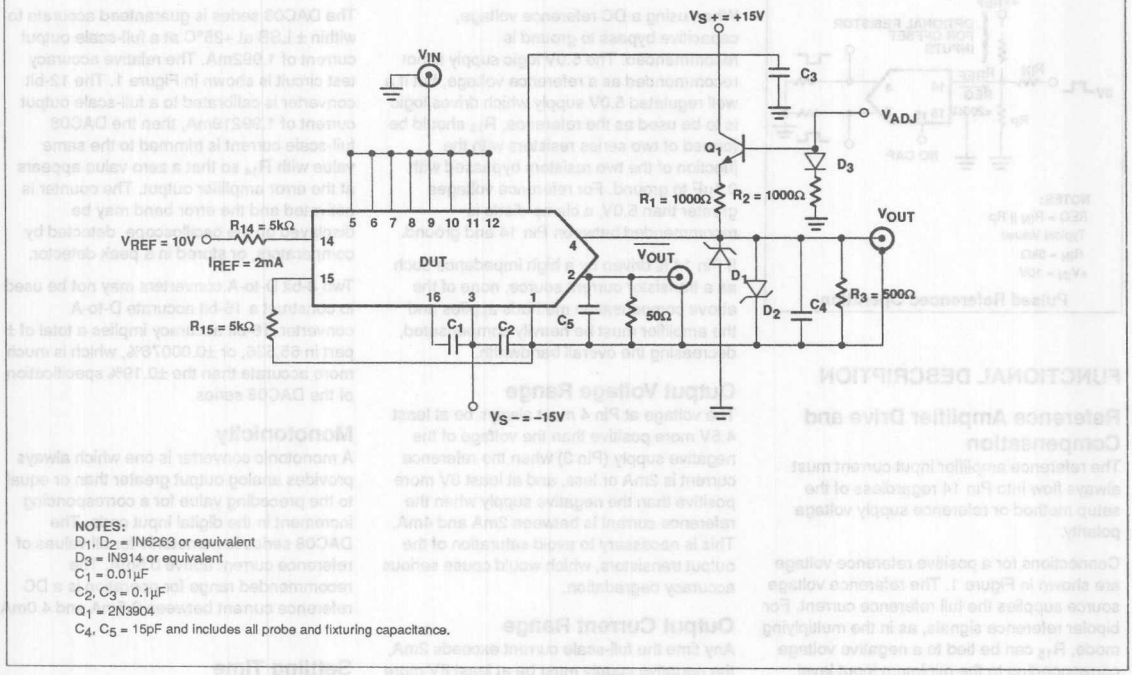
A monotonic converter is one which always provides analog output greater than or equal to the preceding value for a corresponding increment in the digital input code. The DAC08 series is monotonic for all values of reference current above 0.5mA. The recommended range for operation is a DC reference current between 0.5mA and 4.0mA.

Settling Time

The worst-case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all input bits. This time is typically 70ns for settling to within LSB for 8-bit accuracy. This time applies when R_L<500Ω and C_O<25pF. The slowest single switch is the least significant bit, which typically turns on and settles in 65ns. In applications where the DAC functions in a positive-going ramp mode, the worst-case condition does not occur and settling times less than 70ns may be realized.

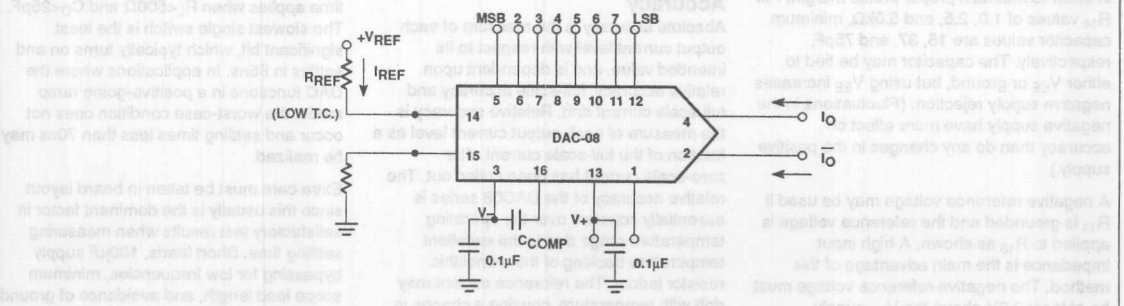
Extra care must be taken in board layout since this usually is the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, minimum scope lead length, and avoidance of ground loops are all mandatory.

SETTLING TIME AND PROPAGATION DELAY



NOTES:
D_1, D_2 = IN6263 or equivalent
D_3 = IN914 or equivalent
C_1 = 0.01μF
C_2, C_3 = 0.1μF
Q_1 = 2N3904
C_4, C_5 = 15pF and includes all probe and fixturing capacitance.

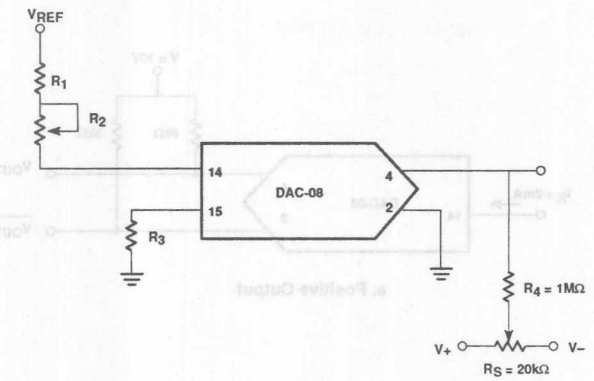
BASIC DAC08 CONFIGURATION



NOTES:

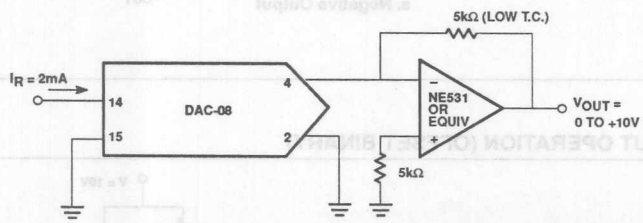
$I_{FS} = \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$; $I_O + \overline{I_O} = I_{FS}$ for *all logic states*

RECOMMENDED FULL-SCALE AND ZERO-SCALE ADJUST

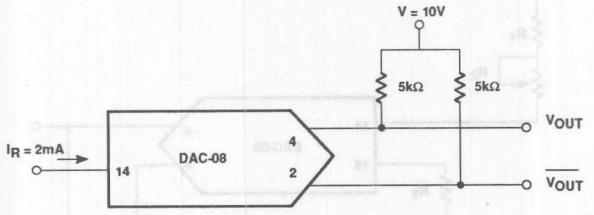


NOTES:
R_1 = low T.C.
$R_3 = R_1 + R_2$
$R_2 = 0.1\ R_1$ to minimize pot. contribution to full-scale drift

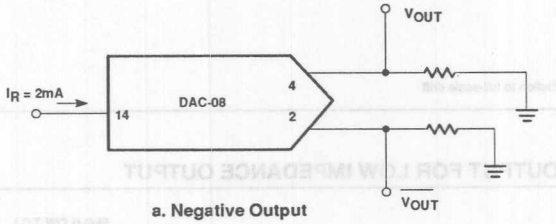
UNIPOLAR VOLTAGE OUTPUT FOR LOW IMPEDANCE OUTPUT



UNIPOLAR VOLTAGE OUTPUT FOR HIGH IMPEDANCE OUTPUT

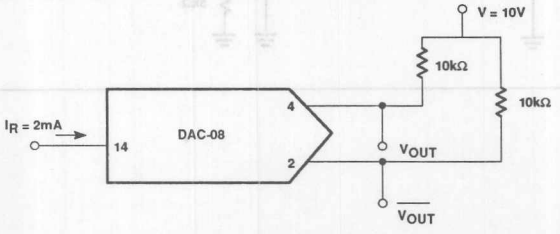


a. Positive Output



a. Negative Output

BASIC BIPOLAR OUTPUT OPERATION (OFFSET BINARY)



	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	V_{OUT}	$V_{\overline{OUT}}$
Positive full-scale	1	1	1	1	1	1	1	1	–9.920V	+10.000
Positive FS – 1LSB	1	1	1	1	1	1	1	0	–9.840V	+9.920
+ Zero-scale + 1LSB	1	0	0	0	0	0	0	1	–0.080V	+0.160
Zero-scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero-scale – 1LSB	0	1	1	1	1	1	1	1	0.080	0.000
Negative full scale – 1LSB	0	0	0	0	0	0	0	1	+9.920	–9.840
Negative full scale	0	0	0	0	0	0	0	0	+10.000	–9.920

8-bit multiplying D/A converter — MC1508-8/1408-8

DESCRIPTION

The MC1508/MC1408 series of 8-bit monolithic digital-to-analog converters provide high-speed performance with low cost. They are designed for use where the output current is a linear product of an 8-bit digital word and an analog reference voltage

FEATURES

- Fast settling time — 70ns (typ)
- Relative accuracy ±0.19% (max error)
- Non-inverting digital inputs are TTL and CMOS compatible
- High-speed multiplying rate 4.0mA/μs (input slew)
- Output voltage swing _0.5V to –5.0V
- Standard supply voltages +5.0V and –5.0V to –15V
- Military qualifications pending

APPLICATIONS

- Tracking A-to-D converters
- 2 1/2-digit panel meters and DVMs
- Waveform synthesis
- Sample-and-Hold
- Peak detector
- Programmable gain and attenuation
- CRT character generation
- Audio digitizing and decoding
- Programmable power supplies
- Analog-digital multiplication
- Digital-digital multiplication
- Analog-digital division
- Digital addition and subtraction
- Speech compression and expansion
- Stepping motor drive modems
- Servo motor and pen drivers

CIRCUIT DESCRIPTION

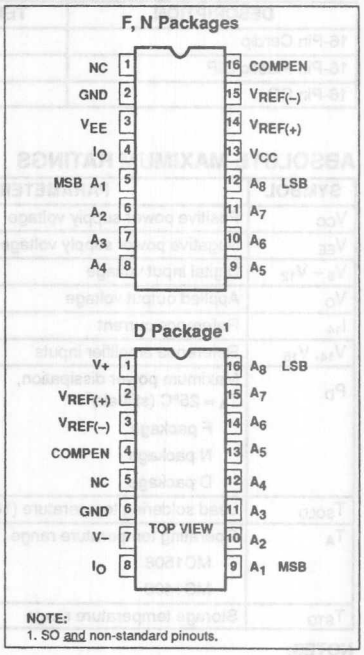
The MC1508/MC1408 consists of a reference current amplifier, an R-2R ladder, and 8 high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are non-inverting in operation; therefore, a high state on the input turns on the specified output current component.

The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

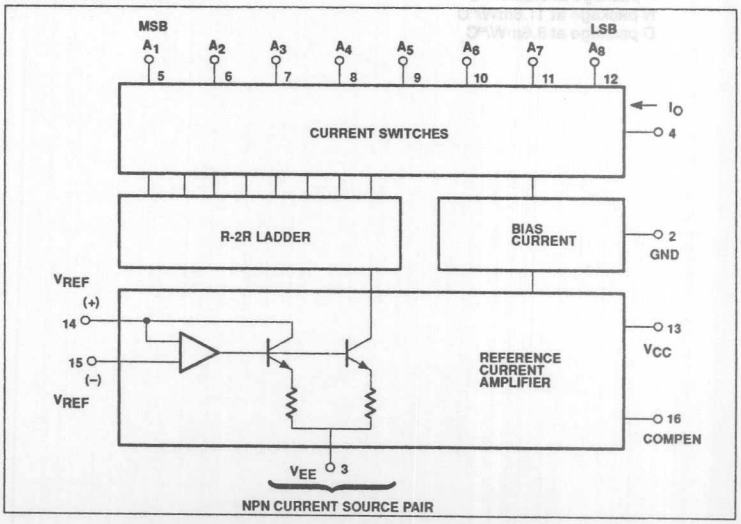
The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992mA for a 2.0mA reference amplifier current if the NPN current source pair is perfectly matched.

PIN CONFIGURATIONS



NOTE:
1. SO and non-standard pinouts.

BLOCK DIAGRAM



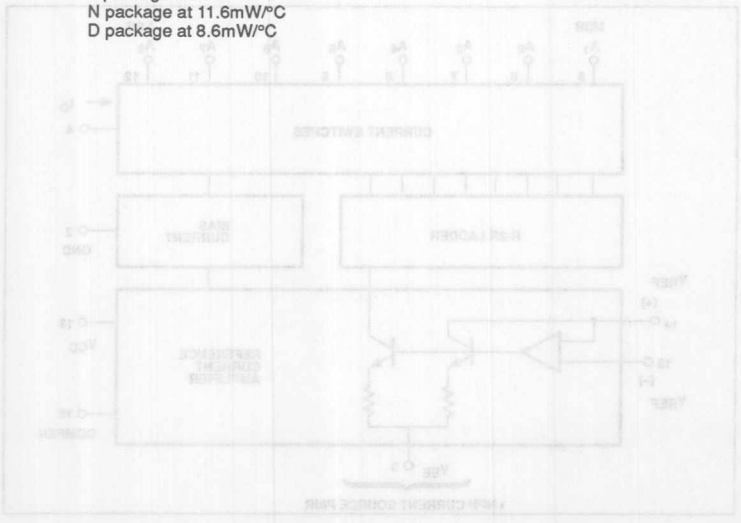
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	-55°C to +125°C	MC1508-8F
16-Pin Plastic DIP	0 to +70°C	MC1408-8N
16-Pin SO	0 to +70°C	MC1408-8D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Positive power supply voltage	+5.5	V
V_{EE}	Negative power supply voltage	–16.5	V
$V_5 - V_{12}$	Digital input voltage	0 to V_{CC}	V
V_O	Applied output voltage	–5.2 to +18	V
I_{14}	Reference current	5.0	mA
V_{14}, V_{15}	Reference amplifier inputs	V_{EE} to V_{CC}	
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1]		
	F package	1190	mW
	N package	1450	mW
	D package	1080	mW
T_{SOLD}	Lead soldering temperature (10 sec)	300	°C
T_A	Operating temperature range	300	°C
	MC1508	–55 to +125	°C
	MC1408	0 to +75	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:
1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C
   N package at 11.6mW/°C
   D package at 8.6mW/°C



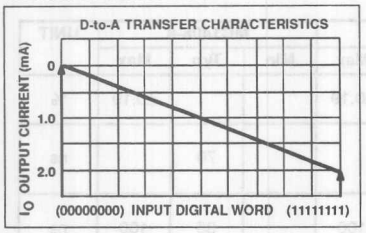
DC ELECTRICAL CHARACTERISTICS

Pin 3 must be 3V more negative than the potential to which R_{15} is returned. $V_{CC} = +5.0V_{DC}$, $V_{EE} = -15V_{DC}$, $V_{REF}/R_{14} = 2.0mA$ unless otherwise specified. MC1508: $T_A = -55°C$ to $125°C$. MC1408: $T_A = 0°C$ to $75°C$, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1508-8			MC1408-8			UNIT
			Min	Typ	Max	Min	Typ	Max	
E_r	Relative accuracy	Error relative to full-scale I_O, Figure 3			±0.19			±0.19	%
t_S	Settling time[1]	To within 1/2 LSB, includes t_{PLH}, $T_A = +25°C$, Figure 4		70			70		ns
t_{PLH} t_{PHL}	Propagation delay time Low-to-High High-to-Low	$T_A = +25°C$, Figure 4		35	100		35	100	ns
TCI_O	Output full-scale current drift			–20			–20		ppm/°C
V_{IH} V_{IL}	Digital input logic level (MSB) High Low	Figure 5	2.0		0.8	2.0		0.8	V_{DC}
I_{IH} I_{IL}	Digital input current (MSB) High Low	Figure 5 $V_{IH} = 5.0V$ $V_{IL} = 0.8V$		0 –0.4	0.04 –0.8		0 –0.4	0.04 –0.8	mA
I_{15}	Reference input bias current	Pin 15, Figure 5		–1.0	–5.0		–1.0	–5.0	µA
I_{OR}	Output current range	Figure 5 $V_{EE} = -5.0V$ $V_{EE} = -7.0V$ to $-15V$	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	mA
I_O	Output current	Figure 5 $V_{REF} = 2.000V$, $R14 = 1000\Omega$	1.9	1.99	2.1	1.9	1.99	2.1	mA
$I_{O(min)}$	Off-state	All bits low		0	4.0		0	4.0	µA
V_O	Output voltage compliance	$E_r \leq 0.19\%$ at $T_A = +25°C$, Figure 5 $V_{EE} = -5V$ V_{EE} below $-10V$		–0.6 +10 –5.5, +10	–0.55, +0.5 –5.0, +0.5		–0.6 +10 –5.5, +10	–0.55, +0.5 –5.0, +0.5	V_{DC}
SRI_{REF}	Reference current slew rate	Figure 6		8.0			8.0		mA/µs
PSRR(–)	Output current power supply sensitivity	$I_{REF} = 1mA$		0.5	2.7		0.5	2.7	µA/V
I_{CC} I_{EE}	Power supply current Positive Negative	All bits low, Figure 5		+2.5 –6.5	+22 –13		+2.5 –6.5	+22 –13	mA
V_{CCR} V_{EER}	Power supply voltage range Positive Negative	$T_A = +25°C$, Figure 5	+4.5 –4.5	+5.0 –15	+5.5 –16.5	+4.5 –4.5	+5.0 –15	+5.5 –16.5	V_{DC}
P_D	Power dissipation	All bits low, Figure 5 $V_{EE} = -5.0V_{DC}$ $V_{EE} = -15.0V_{DC}$		34 110	170 305		34 110	170 305	mW

NOTES:
1. All bits switched.

TYPICAL PERFORMANCE CHARACTERISTICS



FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier input current must always flow into Pin 14. regardless of the setup method or reference supply voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full reference current. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. R_{15} may be eliminated and Pin 15 grounded, with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increasing values of R_{14} to maintain proper phase margin. For R_{14} values of 1.0, 2.5, and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection. (Fluctuations in the negative supply have more effect on accuracy than do any changes in the positive supply.)

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15}, as shown in Figure 2. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at Pin 15.

Capacitive bypass to ground is recommended when a DC reference voltage is used. The 5.0V logic supply is not recommended as a reference voltage, but if a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be formed of two series resistors and the junction of the two resistors bypassed with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage at Pin 4 must always be at least 4.5V more positive than the voltage of the negative supply (Pin 3) when the reference current is 2mA or less, and at least 8V more positive than the negative supply when the reference current is between 2mA and 4mA. This is necessary to avoid saturation of the output transistors, which would cause serious degradation of accuracy.

Signetics MC1508/MC1408 does not need a range control because the design extends the compliance range down to 4.5V (or 8V — see above) above the negative supply voltage without significant degradation of accuracy. Signetics MC1508/MC1408 can be used in sockets designed for other manufacturers' MC1508/MC1408 without circuit modification.

Output Current Range

Any time the full-scale current exceeds 2mA, the negative supply must be at least 8V more negative than the output voltage. This is due to the increased internal voltage drops between the negative supply and the outputs with higher reference currents.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy, full-scale accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current after zero-scale current has been nulled out. The relative accuracy of the MC1508/MC1408 is essentially constant over the operating temperature range because of the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current; however, the MC1508/MC1408 has a very low full-scale current drift over the operating temperature range.

The MC1508/MC1408 series is guaranteed accurate to within ±1/2LSB at +25°C at a full-scale output current of 1.99mA. The relative accuracy test circuit is shown in Figure 3. The 12-bit converter is calibrated to a full-scale output current of 1.99219mA; then the MC1508/MC1408's full-scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on the oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total of ±1/2 part in 65,536, or ±0.00076%, which is much more accurate than the ±0.19% specification of the MC1508/MC1408.

Monotonicity

A monotonic converter is one which always provides an analog output greater than or equal to the preceding value for a corresponding increment in the digital input code. The MC1508/MC1408 is monotonic for all values of reference current above 0.5mA. The recommended range for operation is a DC reference current between 0.5mA and 4.0mA.

Settling Time

The worst case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all input bits. This time is typically 70ns for settling to within 1/2LSB for 8-bit accuracy. This time applies when $R_L < 500\Omega$ and $C_O <$ 25pF. The slowest single switch is the least significant bit, which typically turns on and settles in 65ns. In applications where the D-to-A converter functions in a positive going ramp mode, the worst-case condition does not occur and settling times less than 70ns may be realized.

Extra care must be taken in board layout since this usually is the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, minimum scope lead length, good ground planes, and avoidance of ground loops are all mandatory.

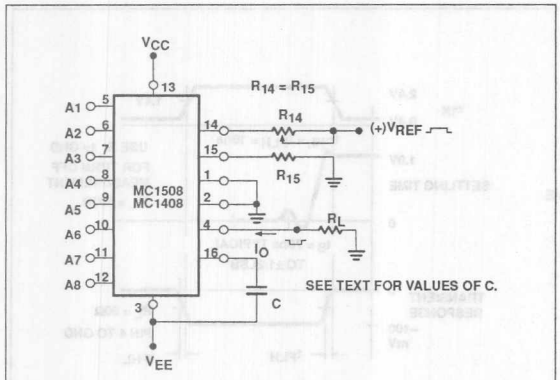


Figure 1. Positive V_{REF}

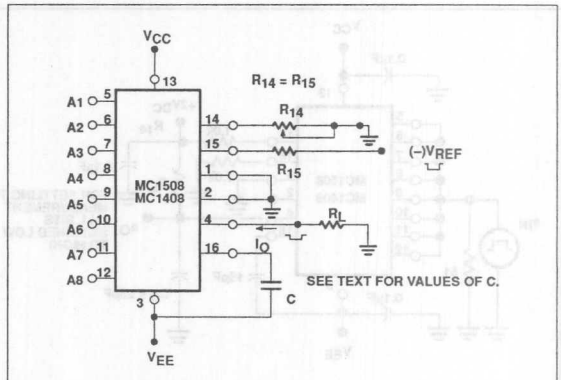


Figure 2. Negative V_{REF}

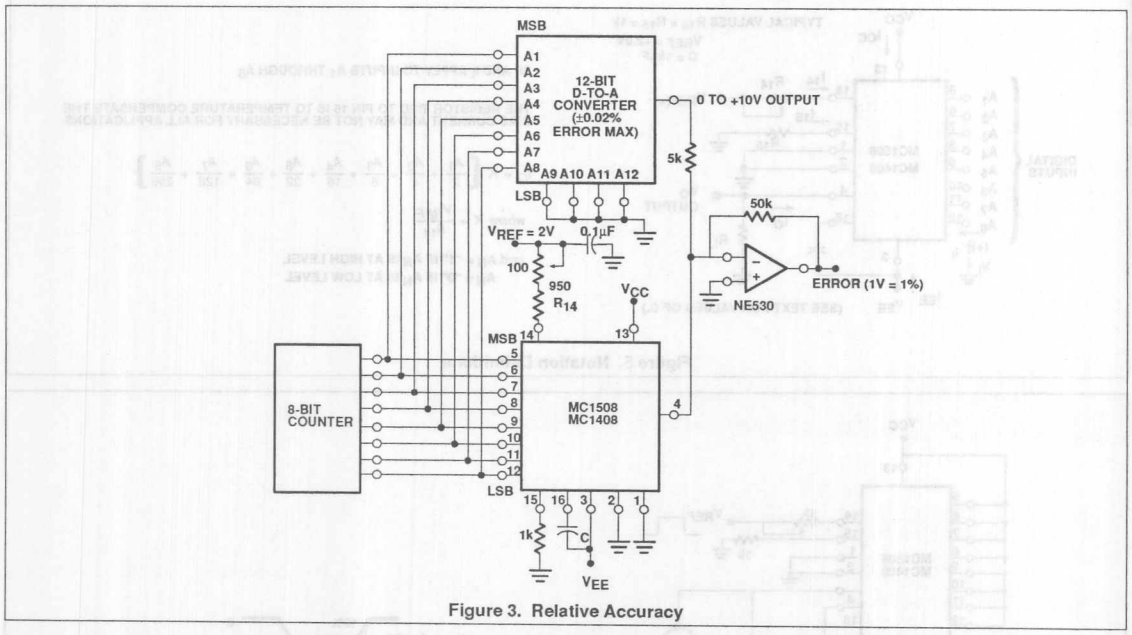


Figure 3. Relative Accuracy

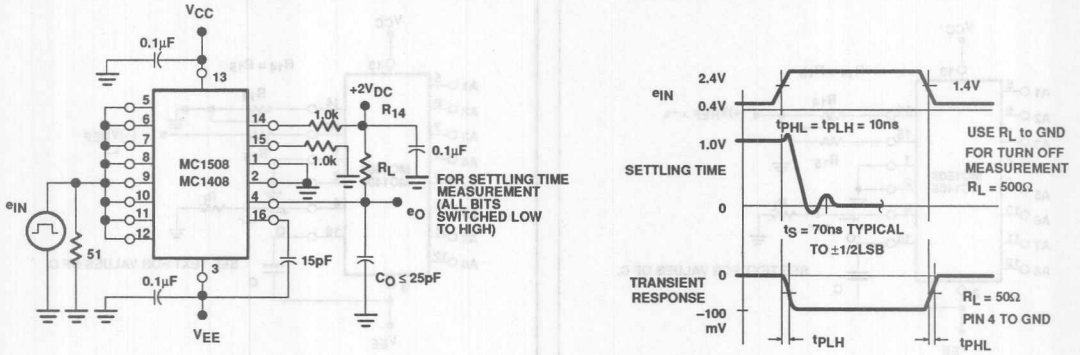


Figure 4. Transient Response and Settling Time

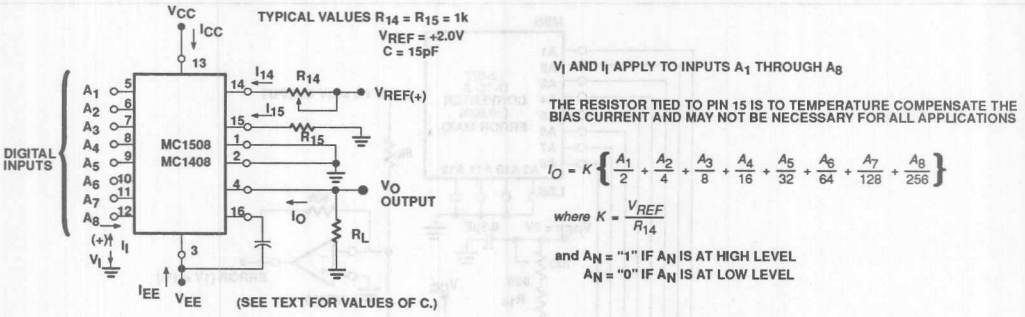


Figure 5. Notation Definitions

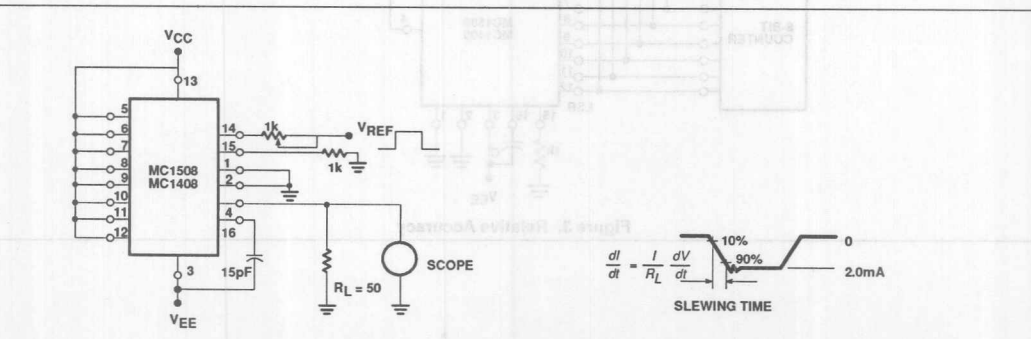


Figure 6. Reference Current Slew Rate Measurement

10-Bit high-speed multiplying D/A converter

MC3410, MC3410C

DESCRIPTION

The MC3410 series are 10-bit Multiplying Digital-to-Analog Converters. They are capable of high-speed performance, and are used as general-purpose building blocks in cost-effective D/A systems.

The Signetics' design provides complete 10-bit accuracy without laser trimming, and guaranteed monotonicity over temperature. Segmented current sources, in conjunction with an R-2R DAC provides the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

FEATURES

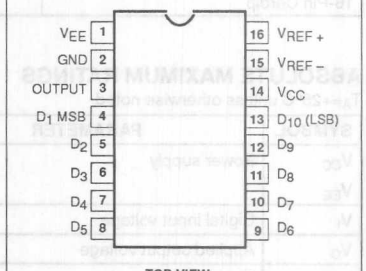
- 10-bit resolution and accuracy (±0.05%)
- Guaranteed monotonicity over temperature
- Fast settling time—250ns typical
- Digital inputs are TTL and CMOS compatible
- Wide output voltage compliance range
- High-speed multiplying input slew rate—20mA/μs
- Reference amplifier internally-compensated
- Standard supply voltages +5V and -15V

APPLICATIONS

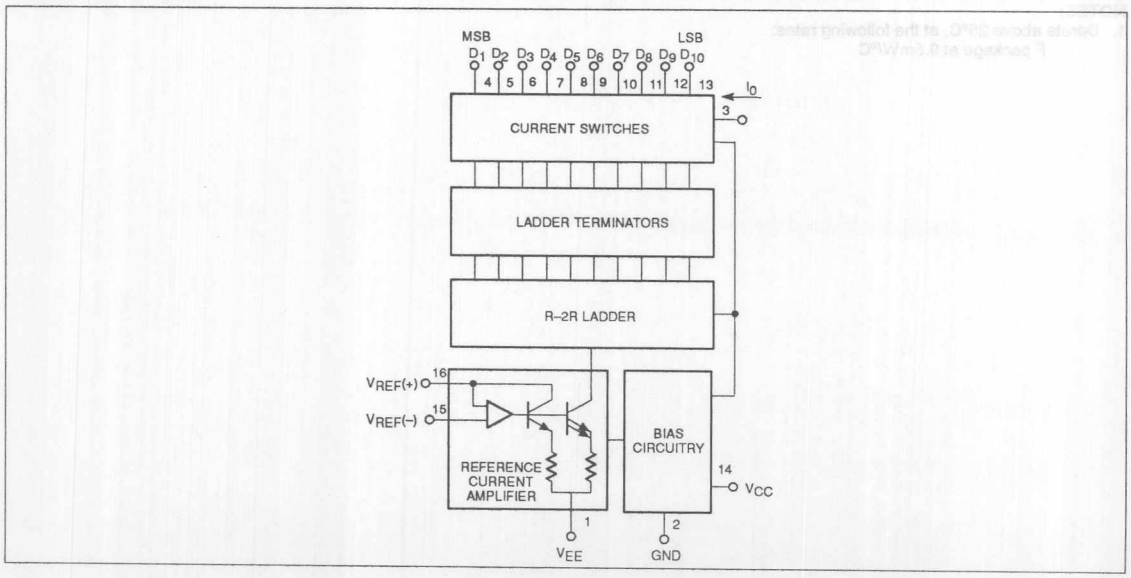
- Successive approximation A/D converters
- High-speed, automatic test equipment
- High-speed modems
- Waveform generators
- CRT displays
- Strip CHART and X-Y plotters
- Programmable power supplies
- Programmable gain and attenuation

PIN CONFIGURATION

F Package



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	MC3410F
16-Pin Cerdip	0 to +70°C	MC3410CF

ABSOLUTE MAXIMUM RATINGS

T_A=+25°C unless otherwise noted

SYMBOL	PARAMETER	RATING	UNIT
V_{CC} V_{EE}	Power supply	+7.0 -18	V_{DC} V_{DC}
V_I	Digital input voltage	+15	V_{DC}
V_O	Applied output voltage	0.5, -5.0	V_{DC}
$I_{REF(16)}$	Reference current	2.5	mA
V_{REF}	Reference amplifier inputs	V_{CC}, V_{EE}	V_{DC}
$V_{REF(D)}$	Reference amplifier differential inputs	0.7	V_{DC}
T_A	Operating ambient temperature range MC3410, 3410C	0 to +70	°C
T_J	Junction temperature, ceramic package	+150	°C
P_D	Maximum power dissipation, T_A=25°C (still-air)[1] F package	1190	mW

NOTES:

1. Derate above 25°C, at the following rates:
   F package at 9.5mW/°C

ELECTRICAL CHARACTERISTICS

V_{CC}=+5.0VDC, V_{EE}=-15DC, $\frac{V_{REF}}{R16}$ =2.0mA, all digital inputs at high logic level. MC3410 Series: T_A=0°C to +70°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MC3410			MC3410C			UNIT
			Min	Typ	Max	Min	Typ	Max	
E_r	Relative accuracy (error relative to full-scale I_O)	T_A=25°C			±0.05			±0.1	%
					1/4			1/2	LSB
TCE_r	Relative accuracy drift (relative to full-scale I_O)			2.5			2.5		ppm/°C
	Monotonicity	Over temperature	10			10			Bits
t_S	Settling time to within ± LSB (all bits LOW-to-HIGH)	T_A=25°C		250			250		ns
t_{PLH} t_{PHL}	Propagation delay time	T_A=25°C		35 20			35 20		ns
TCI_O	Output full scale current drift				60			70	ppm/°C
V_{IH}	Digital input logic levels (all bits) HIGH-level, Logic "1" LOW-level, Logic "0"		2.0		0.8	2.0		0.8	V_{DC}
I_{IH} I_{IL}	Digital input current (all bits) HIGH-level, V_{IH}=5.5V LOW-level, V_{IL}=0.8V			-0.05	+.04 -0.4		-0.05	+.04 -0.4	mA
$I_{REF(15)}$	Reference input bias current (Pin 15)			-1.0	-5.0		-1.0	-5.0	µA
I_{OR}	Output current range			4.0	5.0		4.0	5.0	mA
I_{OH}	Output current (all bits high)	V_{REF}=2.000V, R_{16}=1000Ω	3.8	3.996	4.2	3.8	3.996	4.2	mA
I_{OL}	Output current (all bits low)	T_A=25°C		0	2.0		0	4.0	µA
V_O	Output voltage compliance	T_A=25°C			-2.5 +0.2			-2.5 +0.2	V_{DC}
SR I_{REF}	Reference amplifier slew rate			20			20		mA/µs
ST I_{REF}	Reference amplifier settling time	0 to 4.0mA, ±0.1%		2.0			2.0		µs
PSRR(-)	Output current power supply sensitivity			0.003	0.01		0.003	0.02	%/%
C_O	Output capacitance	V_O=0		25			25		pF
C_I	Digital input capacitance (all bits high)			4.0			4.0		pF
I_{CC} I_{EE}	Power supply current (all bits low)			-11.4	+18 -20		-11.4	+18 -20	mA
V_{CC} V_{EE}	Power supply voltage range	T_A=25°C	+4.75 -14.2	+5.0 -15	+5.25 -15.7	+4.75 -14.2	+5.0 -15	+5.25 -15.7	V_{DC}
	Power consumption (all bits low) (all bits high)			220 200	380		220 200	380	mW

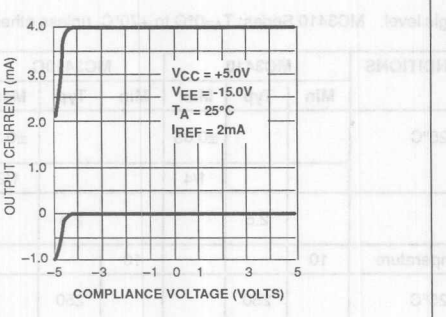


Figure 7. Output Current vs Output Compliance Voltage

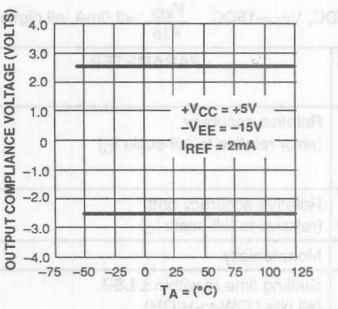


Figure 8. Maximum Output Compliance Voltage vs Temperature

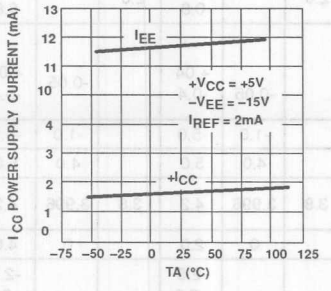


Figure 9. Power Supply Current vs Temperature

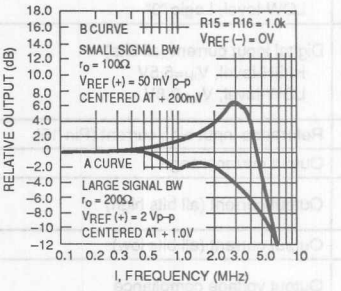


Figure 10. Reference Amplifier Frequency Response

10-Bit high-speed multiplying D/A converter

CIRCUIT DESCRIPTION

The MC3410 consists of four segment current sources which generate the two most significant bits (MSBs), and an R-2R DAC implemented with ion-implanted resistors for scaling the remaining eight least significant bits (LSBs) (See Figure 5). This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully differential current switches. The switches use current steering for speed.

An on-chip high-slew reference current amplifier drives the R-2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input. Out-board resistor R_{16} (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder.

Thus, for a reference voltage of 2.0V and a 1kΩ resistor tied to Pin 16, the full-scale current is approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R_{16} should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3V above the V_{EE} supply voltage for best operation. Bipolar input signals may be handled by connecting R_{16} to a positive voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R_{16} should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1μF capacitor to ground.

The reference amplifier is internally-compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R_{16} and reference voltages which supply 2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R_{16} increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R_{16}=1.0kΩ, and settling time is ≈ 10μs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

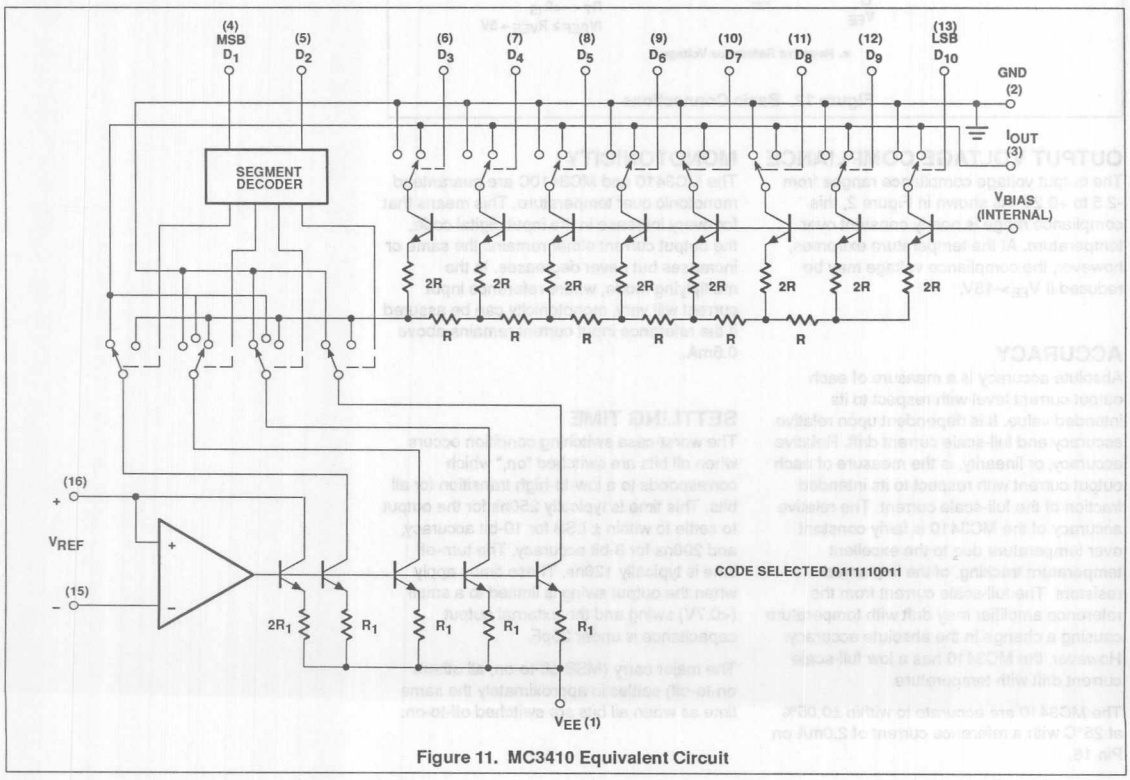


Figure 11. MC3410 Equivalent Circuit

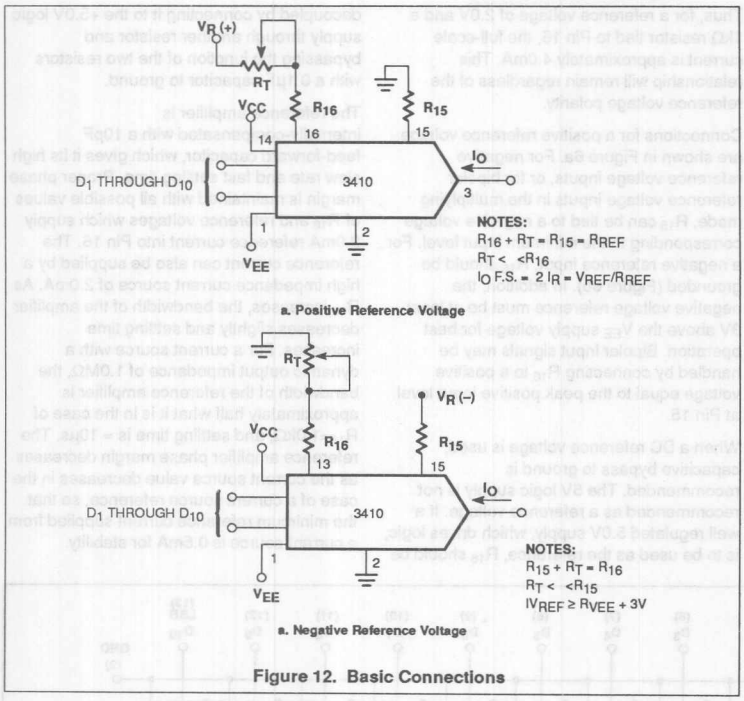


Figure 12. Basic Connections

If a load resistor of 625Ω is connected to ground, allowing the output to swing to -2.5V, the settling time increases to 1.5μs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing, and minimum scope lead length are all necessary.

A typical test setup for measuring settling time is shown in Figure 7. The same setup for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 500Ω load resistor R_L.

OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from -2.5 to +0.2V. As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if V_{EE}>-15V.

ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full-scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full-scale current. The relative accuracy of the MC3410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full-scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the MC3410 has a low full-scale current drift with temperature.

The MC3410 are accurate to within ±0.05% at 25°C with a reference current of 2.0mA on Pin 16.

MONOTONICITY

The MC3410 and MC3410C are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 250ns for the output to settle to within ± LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (<0.7V) swing and the external output capacitance is under 25pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

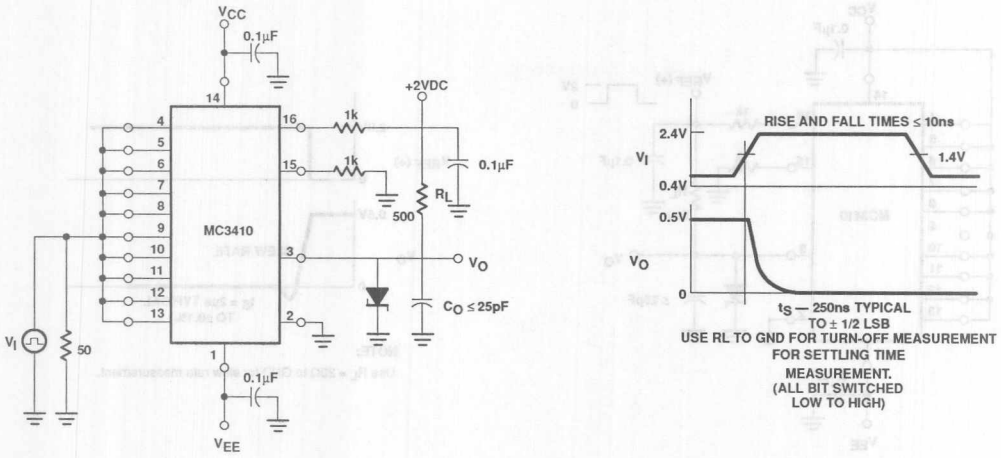


Figure 13. Settling Time

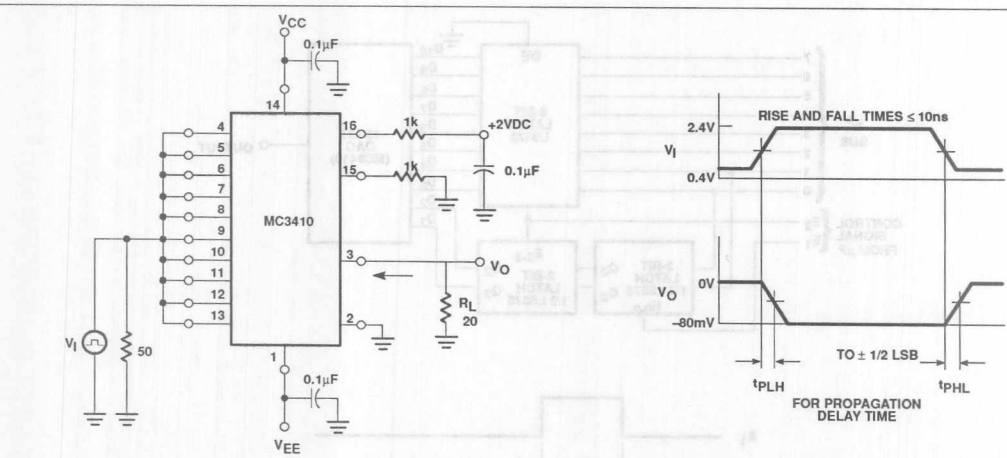


Figure 14. Propagation Delay Time

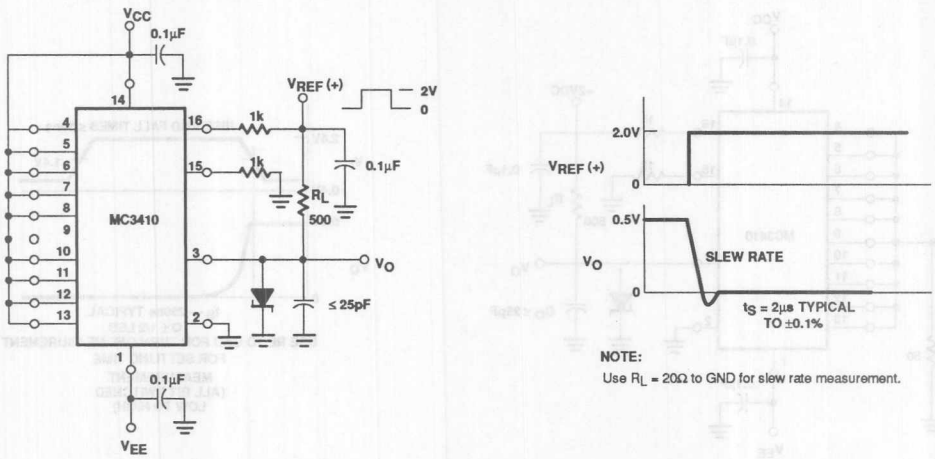


Figure 15. Reference Amplifier Settling Time and Slew Rate

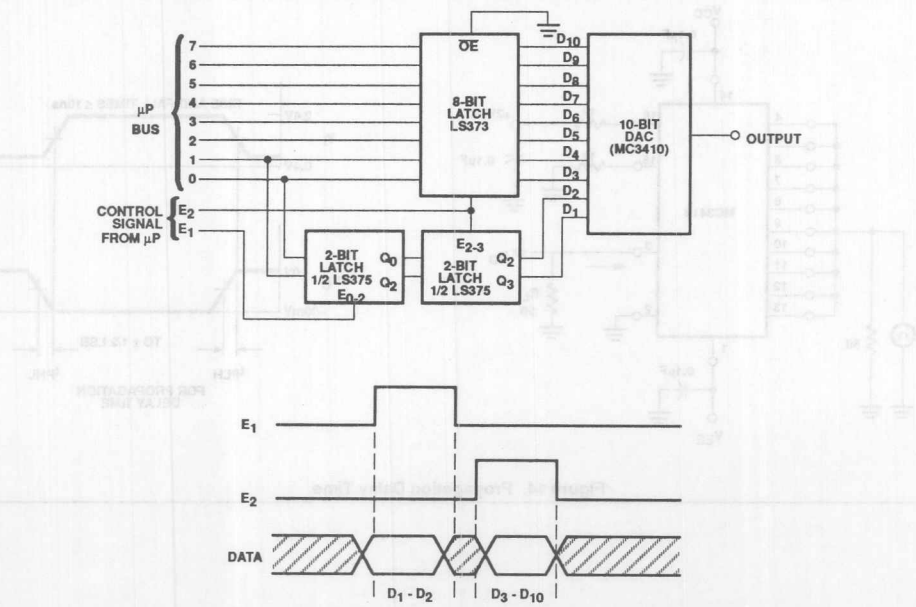


Figure 16. Interfacing 10-Bit DAC With 8-Bit Microprocessor

8-Bit μp-compatible D/A converter | NE/SE5018/5019

DESCRIPTION

The NE/SE5018/19 is a complete 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches which are controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full-scale while maintaining a low temperature coefficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

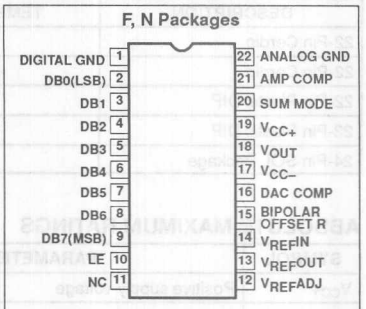
- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Output buffer amplifier
- Accurate to ± LSB (0.19%)
- Monotonic to 8 bits
- Amplifier and reference both short-circuit protected
- Compatible with 8085, 6800 and many other μPs

APPLICATIONS

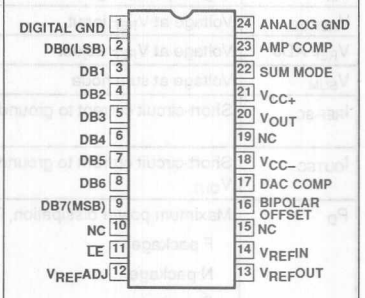
- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication

PIN CONFIGURATIONS

F, N Packages

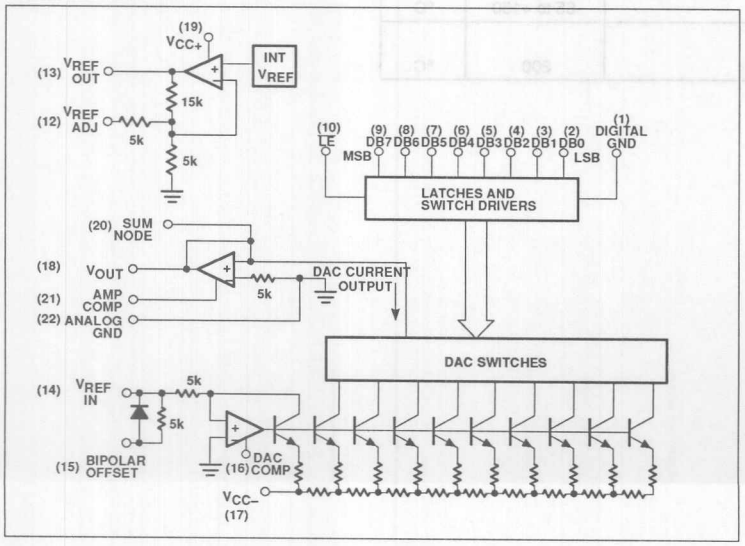


D Package[1]



NOTE:
1. SOL and non-standard pinout

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
22-Pin Cerdip	0 to +70°C	NE5018/5019F
22-Pin Cerdip	-55°C to +125°C	SE5018/5019F
22-Pin Plastic DIP	0 to +70°C	NE5018/5019N
22-Pin Plastic DIP	-55°C to +125°C	SE5018/5019N
24-Pin SOL Package	0 to +70°C	NE5018/5019D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	-18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at V_{REF} input	12	V
V_{REF} ADJ	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
$I_{REF\ SC}$	Short-circuit current to ground at $V_{REF\ OUT}$	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Maximum power dissipation, T_A=25°C (still-air)[1]		
	F package	1740	mW
	N package	2190	mW
	D package	1600	mW
T_A	Operating temperature range		
	SE5018	-55 to +125	°C
	NE5018	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTES:
1. Derate above 25°C at the following rates:
   F package at 13.9mW/°C
   N package at 17.5mW/°C
   D package at 12.8mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}+=+15V, V_{CC}-=-15V, SE5018. -55°C≤T_A≤125°C, NE5018. 0°C≤T_A≤70°C, unless otherwise specified. [1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5018			NE/SE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.1	%FS
V_{CC}+	Positive supply voltage		11.4	15		11.4	15		V
V_{CC}-	Negative supply voltage		-11.4	-15		-11.4	-15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1=0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1=0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1=0V, 2V<V_{IN}<18V		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1=0V, -5V<V_{IN}<0.8V		-2.0	-10		-2.0	-10	μA
V_{FS}	Full-scale output	Unipolar mode, V_{REF}=5.000V, all bits high, T_A=25°C	9.50		10.5	9.50		10.5	V
+V_{FS}	Full-scale output	Bipolar mode, V_{REF}=5.000V all bits high, T_A=25°C	4.75		5.25	4.75		5.25	V
-V_{FS}	Negative full scale	Bipolar mode, V_{REF}=5.000V, all bits low, T_A=25°C	-5.25		-4.75	-5.25		-4.75	V
V_{ZS}	Zero-scale Output	Unipolar mode, V_{REF}=5.000V all bits low, T_A=25°C	-30		+30	-30		+30	mV
I_{OS}	Output short circuit current	T_A=25°C V_{OUT}=0V		15	40		15	40	mA
$PSR+_{(OUT)}$	Output power supply rejection (+)	V-=-15V, 13.5V≤V+≤16.5V, external $V_{REF\ IN}$=5.000V		0.001	0.01		0.001	0.01	%FS %VS
$PSR-_{(OUT)}$	Output power supply rejection (-)	V+=-15V, -13.5V≤V-≤-16.5V, external $V_{REF\ IN}$=5.000V		0.001	0.01		0.001	0.01	%FS %VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN}$=5.000V		20			20		ppm/°C
TC_{ZS}	Zero-scale temperature coefficient			5			5		ppm/°C
I_{REF}	Reference output current				3			3	mA
I_{REFSC}	Reference short circuit current	T_A=25°C $V_{REF\ OUT}$=0V		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	V-=-15V, 13.5V≤V+≤16.5V, I_{REF}=1.0mA		0.003	0.01		0.003	0.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (-)	V+=-15V, -13.5V≤V-≤16.5V,		0.003	0.01		0.003	0.01	%VR/%VS
V_{REF}	Reference voltage	I_{REF}=1.0mA T_A=25°C	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	I_{REF}=1.0mA		60			60		ppm/°C
Z_{IN}	DAC $V_{REF\ IN}$ input impedance	I_{REF}=1.0mA, T_A=25°C	4.15	5.0	5.85	4.15	5.0	5.85	kΩ
I_{CC}+	Positive supply current	V_{CC}+=15V		7	14		7	14	mA
I_{CC}-	Negative supply current	V_{CC}-=-15V		-10	-15		-10	-15	mA
P_D	Power dissipation	I_{REF}=1.0mA, V_{CC}=±15V		255	435		255	435	mW

NOTES:
1. Refer to Figure 1.

AC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = ±15V, T_A = 25°C

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	NE/SE5018/19			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	±1/2LSB	Input	All bits low-to-high[2]		1.8		µs
t_{SHL}	Settling time	±1/2LSB	Input	All bits high-to-low[3]		2.3		µs
t_{PLH}	Propagation delay	Output	Input	All bits switched low-to-high[2]		300		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched high-to-low[3]		150		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change[2, 3]		150		ns
t_{PLH}	Propagation delay	Output	$\overline{CE}$	Low-to-high transition[4]		300		ns
t_{PHL}	Propagation delay	Output	$\overline{CE}$	High-to-low transition[5]		150		ns
t_S	Setup time	$\overline{CE}$	Input	1, 6	100			ns
t_H	Hold time	Input	$\overline{CE}$	1, 6	50			ns
t_{PW}	Latch enable pulse width			1, 6	150			ns

NOTES:
1. Refer to Figure 2.
2. See Figure 5.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. For reference currents>3mA, use of an external buffer is required.

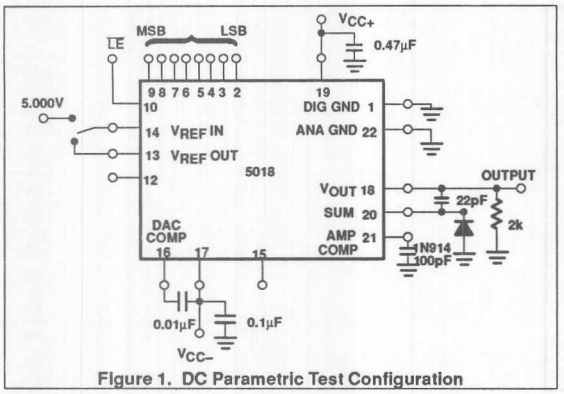


Figure 1. DC Parametric Test Configuration

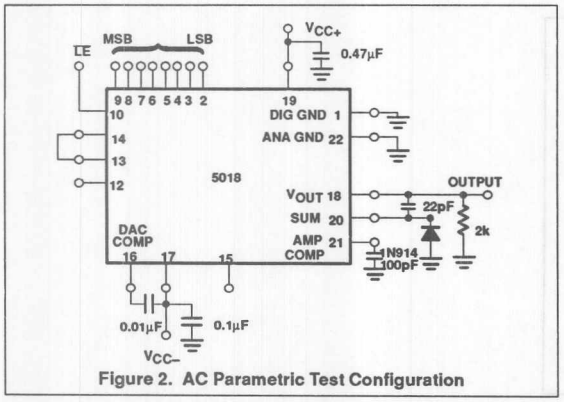


Figure 2. AC Parametric Test Configuration

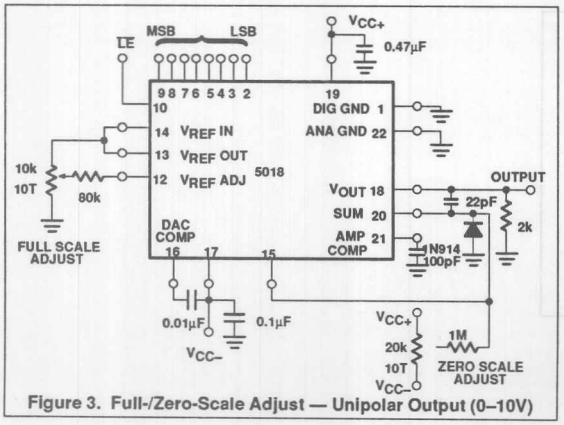


Figure 3. Full-/Zero-Scale Adjust — Unipolar Output (0–10V)

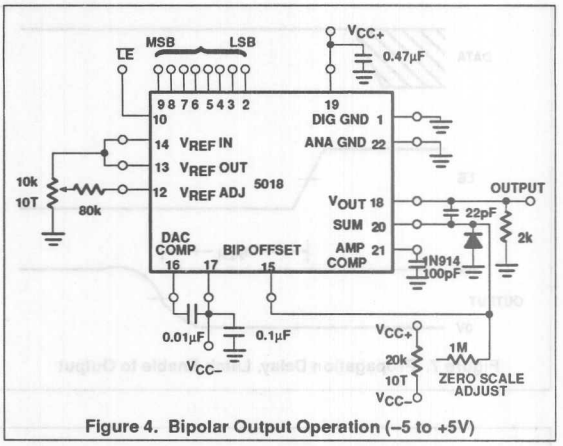


Figure 4. Bipolar Output Operation (–5 to +5V)

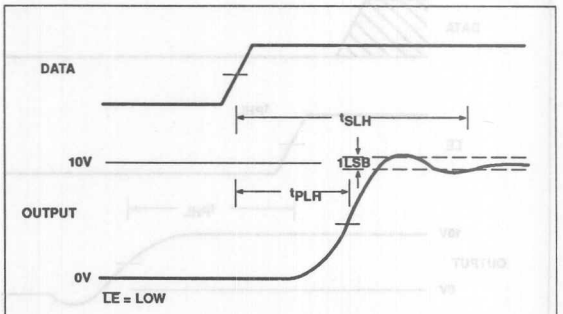


Figure 5. Settling Time and Propagation Delay, Low-to-High Data

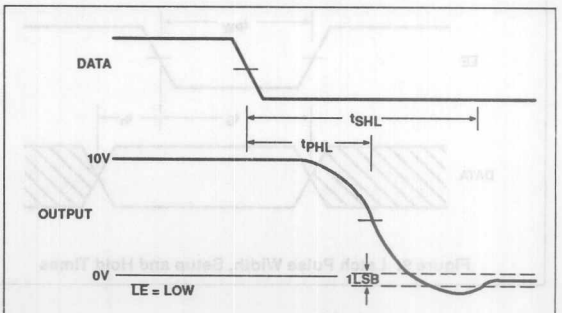


Figure 6. Settling Time and Propagation Delay, High-to-Low Data

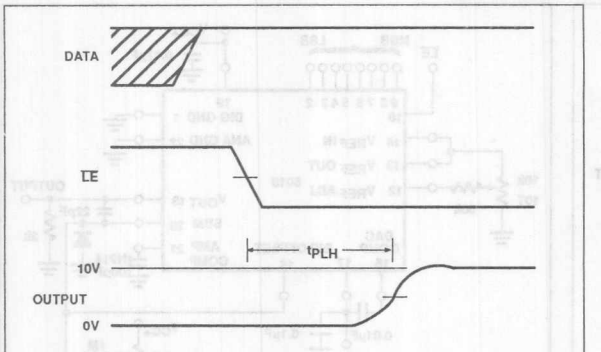


Figure 7. Propagation Delay, Latch Enable to Output

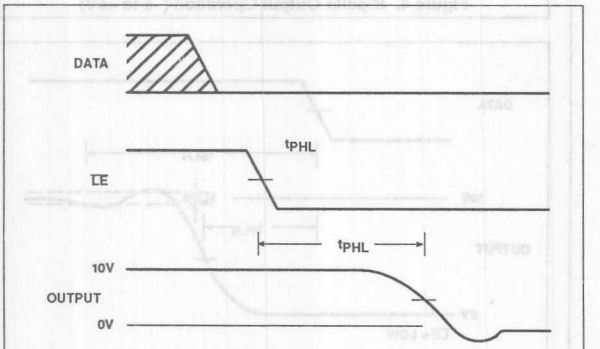


Figure 8. Propagation Delay, Latch Enable to Output

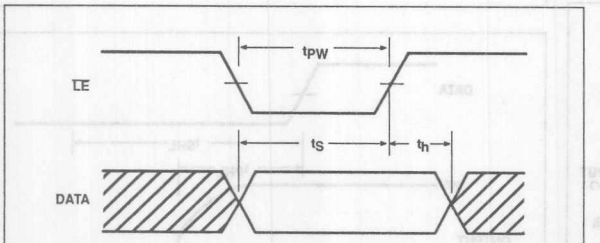


Figure 9. Latch Pulse Width, Setup and Hold Times

10-Bit μP-compatible D/A converter

NE5020

DESCRIPTION

The NE5020 is a microprocessor-compatible monolithic 10-bit digital-to-analog converter subsystem. This device offers 10-bit resolution and ±0.1% accuracy and monotonicity guaranteed over full operating temperature range.

Low loading latches, adjustable logic thresholds, and addressing capability allow the NE5020 to directly interface with most microprocessor- and logic-controlled systems.

The NE5020 contains internal voltage reference, DAC switches and resistor ladder. Also, the input buffer and output summing amplifier are included. In addition, the matched application resistors for scaling either unipolar or bipolar output values are included on a single monolithic chip.

The result is a near minimum component count 10-bit resolution DAC system.

FEATURES

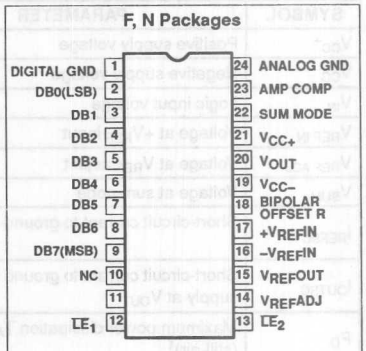
- 10-bit resolution
- Guaranteed monotonicity over operating range
- ±0.1% relative accuracy
- Unipolar (0V to +10V) and bipolar (± 5V) output range
- Logic bus compatible
- 5μs settling time

APPLICATIONS

- Precision 10-bit D/A converters
- 10-bit analog-to-digital converters
- Programmable power supplies
- Test equipment
- Measurement instruments

PIN CONFIGURATION

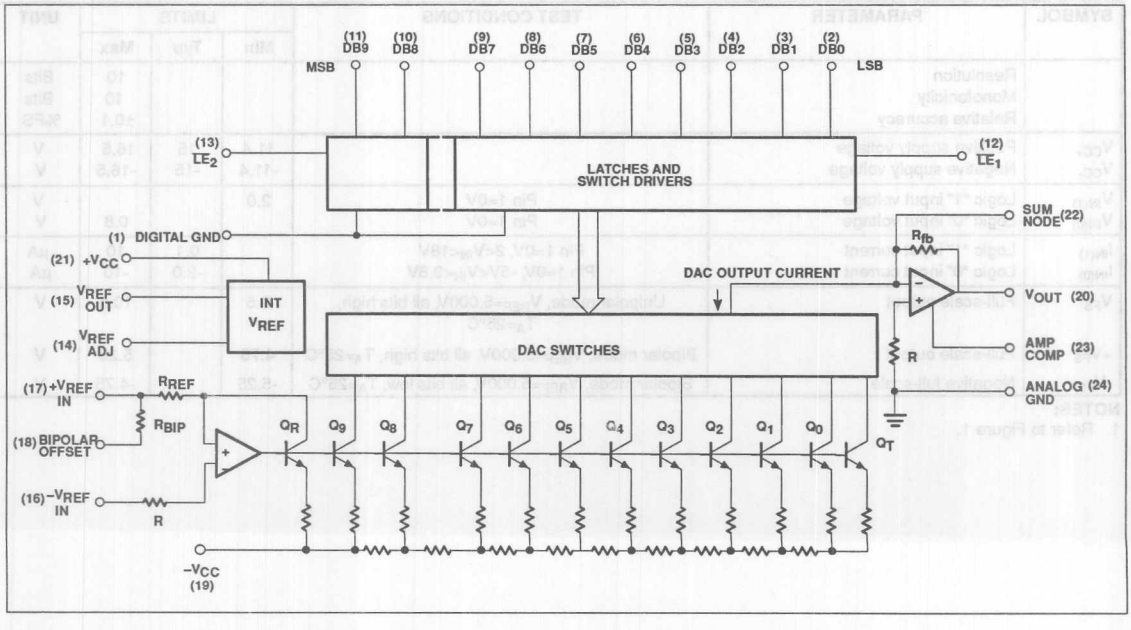
F, N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Cerdip	0 to 70°C	NE5020F
24-Pin Plastic DIP	0 to 70°C	NE5020N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}^+	Positive supply voltage	18	V
V_{CC}^-	Negative supply voltage	-18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at $+V_{REF}$ input	12	V
$V_{REF\ ADJ}$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at $V_{REF\ OUT}$	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Maximum power dissipation T_A=25°C, (still-air)[1]		
	F package	2150	mW
	N package	2150	mW
T_A	Operating temperature range NE5020	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	300	°C

NOTES:
1. Derate above 25°C at the following rates:
   F package at 17.2mW/°C
   N package at 17.2mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}+=+15V, V_{CC}-=-15V, 0 ≤ T_A≤70°C, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution				10	Bits
	Monotonicity				10	Bits
	Relative accuracy				±0.1	%FS
V_{CC+}	Positive supply voltage		11.4	15	16.5	V
V_{CC-}	Negative supply voltage		-11.4	-15	-16.5	V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1=0V	2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1=0V			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1=0V, 2<V_{IN}<18V		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1=0V, -5V<V_{IN}<0.8V		-2.0	-10	μA
V_{FS}	Full-scale output	Unipolar mode, V_{REF}=5.000V, all bits high, T_A=25°C	9.5		10.5	V
$+V_{FS}$	Full-scale output	Bipolar mode, V_{REF}=5.000V, all bits high, T_A=25°C	4.75		5.25	V
$-V_{FS}$	Negative full-scale	Bipolar mode, V_{REF}=5.000V, all bits low, T_A=25°C	-5.25		-4.75	V

NOTES:
1. Refer to Figure 1.

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{ZS}	Zero-scale output	Unipolar mode, V_{REF}=5.000V, all bits low, T_A=25°C	-30		+30	mV
I_{OS}	Output short-circuit current	T_A=25°C V_{OUT}=0V		±15	±40	mA
$PSR+_{(OUT)}$	Output power supply rejection (+)	V-=-15V, 13.5V≤V+≤16.5V, external $V_{REF\ IN}$=5.000V		0.001	0.01	%FS/%VS
$PSR-_{(OUT)}$	Output power supply rejection (-)	V+=15V, -13.5V≤V-≤-16.5V, external $V_{REF\ IN}$=5.000V		0.001	0.01	%FS/%VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN}$=5.000V		20		ppmFS/°C
TC_{ZS}	Zero-scale temperature coefficient			5		ppmFS/°C
I_{REF}[2]	Reference output current				3	mA
$I_{REF\ SC}$	Reference short circuit current	T_A=25°C $V_{REF\ OUT}$=0V		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	V-=-15V, 13.5V≤V+≤16.5V, I_{REF}=1.0mA		.003	.01	%VR/%VS
$PSR-_{REF}$	Reference power supply rejection (-)	V+=15V, -13.5V≤V-≤16.5V,		.003	.01	%VR/%VS
V_{REF}	Reference voltage	I_{REF}=1.0mA, T_A=25°C	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	I_{REF}=1.0mA		60		ppm/°C
Z_{IN}	DAC $V_{REF\ IN}$ input impedance	I_{REF}=1.0mA		5.0		kΩ
$I_{CC}+$	Positive supply current	V_{CC}+=15V		7	14	mA
$I_{CC}-$	Negative supply current	V_{CC} -=-15V		-10	-15	mA
P_D	Power dissipation	I_{REF}=1.0mA, V_{CC}=±15V		255	435	mW

NOTES:
1. Refer to Figure 1.
2. For $I_{REF\ OUT}$ greater than 3mA, an external buffer is required.

AC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = +15V, T_A = 25°C.

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	±1/2LSB	Input	All bits low-to-high[2]		5		µs
t_{SHL}	Settling time	±1/2LSB	Input	All bits high-to-low[3]		5		µs
t_{PLH}	Propagation delay	Output	Input	All bits switched low-to-high[2]		30		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched high-to-low[3]		150		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change[2,3]		150		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition[4]		300		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition[5]		150		ns
t_S	Set-up time	$\overline{LE}$	Input	[1,6]	100			ns
t_H	Hold time	Input	$\overline{LE}$	[1,6]	50			ns
t_{PW}	Latch enable pulse width			[1,6]	150			ns

NOTES:
1. Refer to Figure 2.
2. See Figure 5.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.

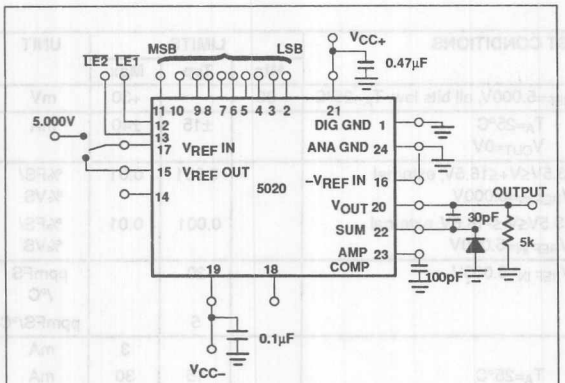


Figure 1. DC Parametric Test Configuration

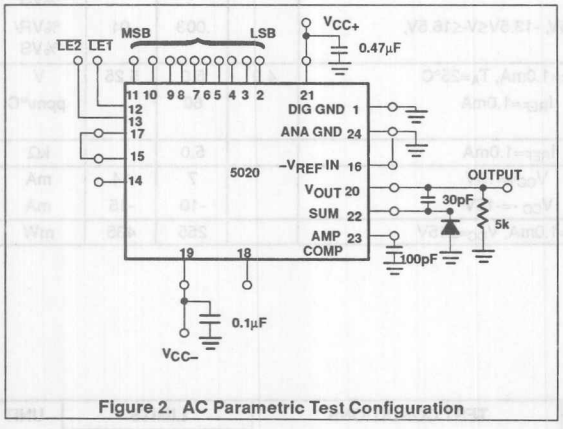


Figure 2. AC Parametric Test Configuration

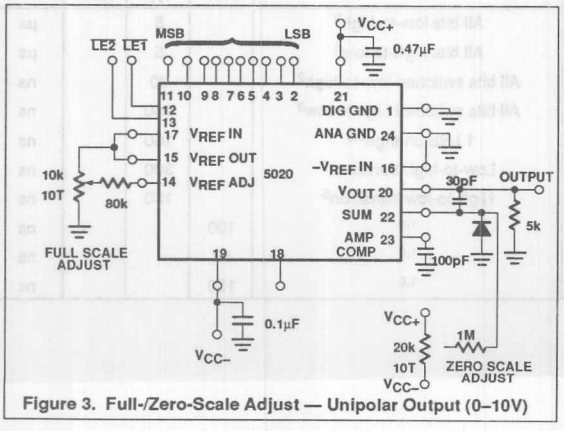


Figure 3. Full-/Zero-Scale Adjust — Unipolar Output (0–10V)

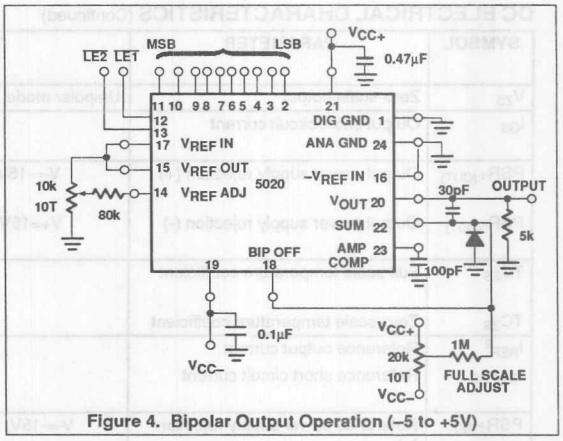


Figure 4. Bipolar Output Operation (–5 to +5V)

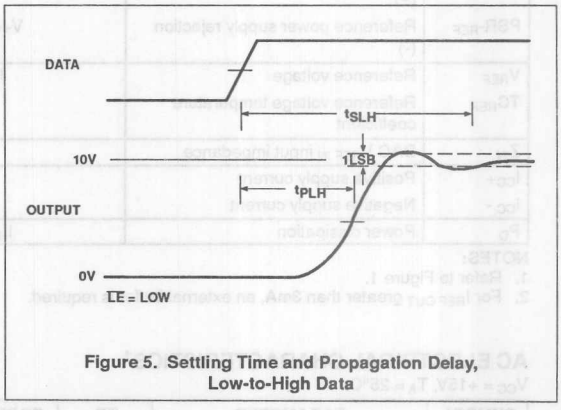


Figure 5. Settling Time and Propagation Delay, Low-to-High Data

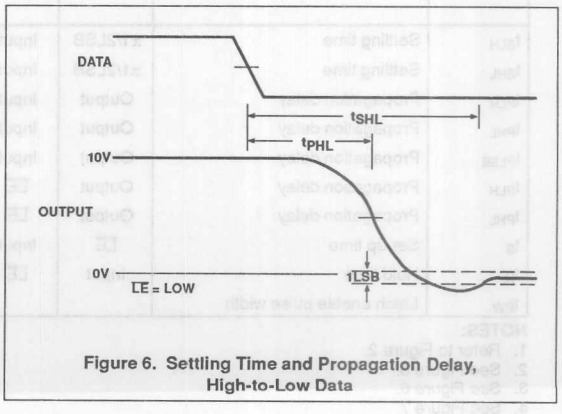


Figure 6. Settling Time and Propagation Delay, High-to-Low Data

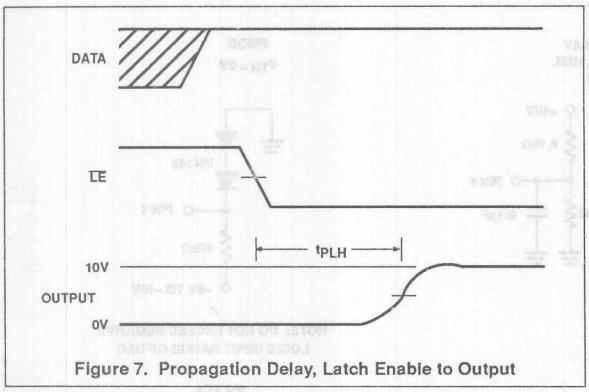


Figure 7. Propagation Delay, Latch Enable to Output

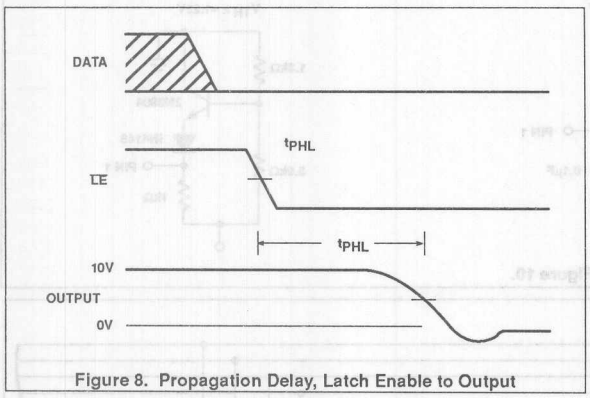


Figure 8. Propagation Delay, Latch Enable to Output

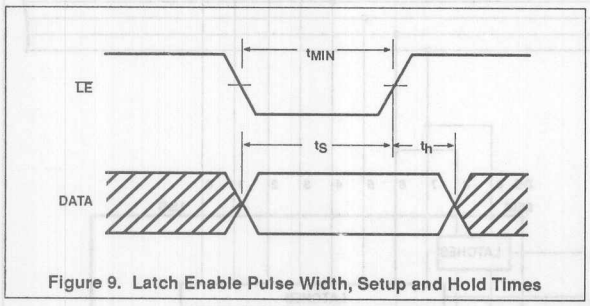


Figure 9. Latch Enable Pulse Width, Setup and Hold Times

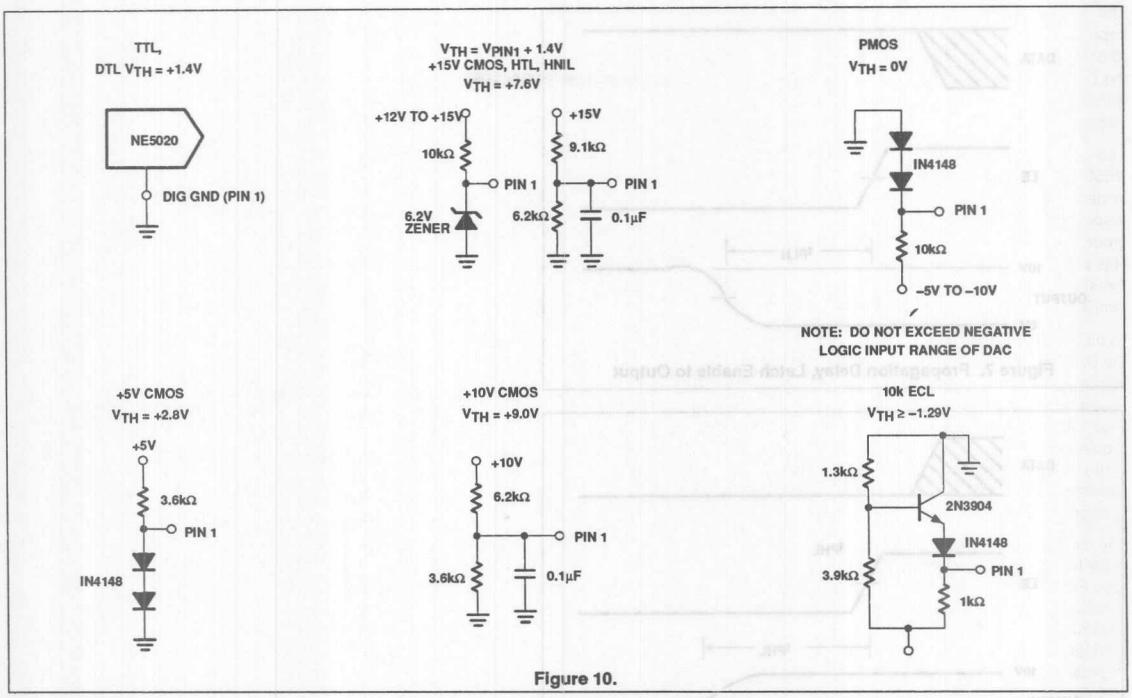


Figure 10.

CIRCUIT DESCRIPTION

The NE5020 provides ten data latches, an internal voltage reference, appliication resistors, and a scaled output voltage in addition to the basic DAC components (see Block Diagram).

Latch Circuit

Digital interface iwth the NE5020 is readily accomplished through the use of two latch enable ports ($\overline{LE}_1$ and $\overline{LE}_2$) and ten data input latches. $\overline{LE}_2$ controls the two most significant bits of data (DB9 and DB8) while $\overline{LE}_1$ controls the eight lesser significant bits (DB_7 through DB_0). Both the latch enable ports ($\overline{LE}$) and the data inputs are static- and threshold-sensitive. When the latch enable ports ($\overline{LE}$) are high (Logic '1') the data inputs become very high impedances and essentially disappear from the data bus. Addressing the $\overline{LE}$ with a low static (Logic '0'), the latches become active and adapt the logic states present on the data bus. During this state, the output of the DAC will change to the value proportional to the data bus value. When the latch enable returns to a high state, the selected set of data inputs (i.e., depending on which $\overline{LE}$ goes high) 'memorizes' the data bus logic states and the output changes to the unique output value corresponding to the binary word in the latch.

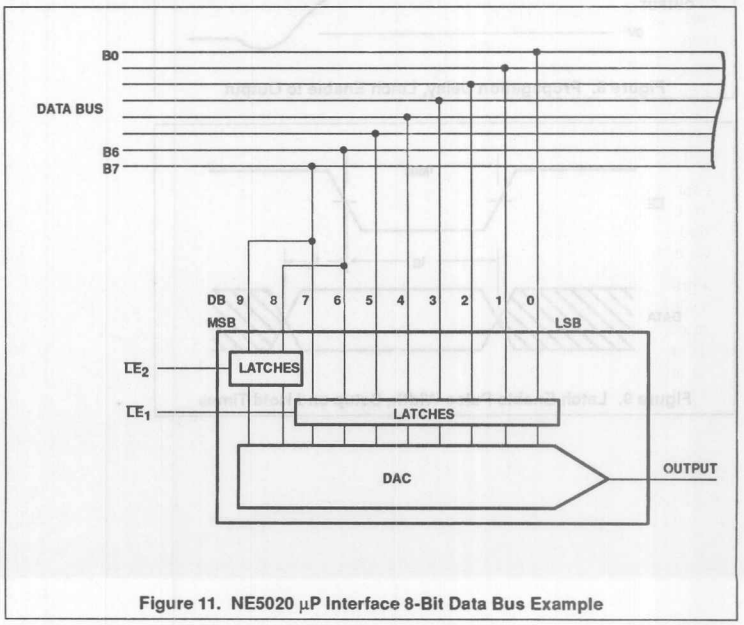


Figure 11. NE5020 μP Interface 8-Bit Data Bus Example

The data inputs are inactive and high impedance (typically requiring –2µA for low (0.8V max) or 0.1µA for high (2.0V min) when the $\overline{CE}$ is high. Any changes on the data bus with $\overline{CE}$ high will have no effect on the DAC output.

The digital logic inputs ($\overline{CE}$ and DB) for the NE5020 utilize a differential input logic system with a threshold level of +1.4V with respect to the voltage level on the digital ground pin (Pin 1). Figure 10 details several bias schemes used to provide the proper threshold voltage levels for various logic families.

To be compatible with a bus-oriented system, the DAC should respond in as short a period as possible to insure full utilization of the microprocessor, controller and I/O control lines. Figure 9 shows the typical timing requirements of the latch and data lines. This figure indicates that data on the data bus should be stable for at least 50ns after $\overline{CE}$ is changed to a high state.

The independent $\overline{CE}$ ($\overline{CE}_1$ and $\overline{CE}_2$) lines allow for direct interface from an 8-bit bus (see Figure 11). Data for the two MSBs is supplied and stored when $\overline{CE}_2$ is activated low and returned high according to the NE5020 timing requirements. Then $\overline{CE}_1$ is activated low and the remaining eight LSBs of data are transferred into the DAC. With $\overline{CE}_1$ returning high, the loading of 10-bit data word from an 8-bit data bus is complete.

Occasionally the analog output must change to its data value within one data address operation. This is no problem using the NE5020 on a 16-bit bus or any other data bus with 10 or greater data bits.

This can be accomplished from an 8-bit data bus by utilizing an external latch circuit to preload the two MSB data values. Figure 12 shows the circuit configuration.

After preloading (via $\overline{CE}$ preload) the external latch with the two MSB values, $\overline{CE}_2$ is activated low and the eight LSBs and the two MSBs are concurrently loaded into the DAC in one address operation. This permits the DAC output to make its appropriate change at one time.

Reference Interface

The NE5020 contains an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long-term stability characteristics.

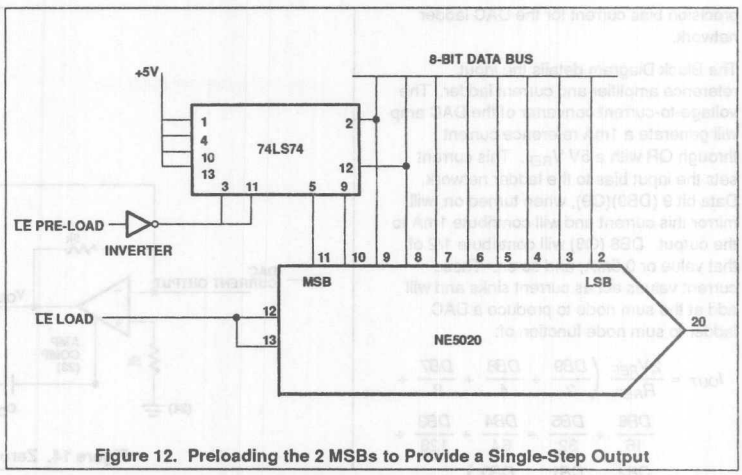


Figure 12. Preloading the 2 MSBs to Provide a Single-Step Output

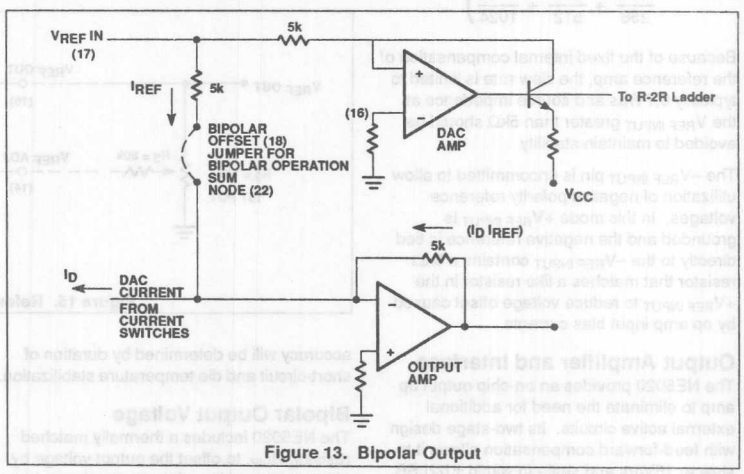


Figure 13. Bipolar Output

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5V reference output. Providing a $V_{REF\ ADJ}$ (Pin 14) allows trimming of the reference output. Utilization of the adjust circuit shown in Figure 15 performs not only V_{REF} adjustment, but also full-scale output adjust. Notice that the $V_{REF\ ADJ}$ pin is essentially the sum node of an op amp and is sensitive to excessive node capacitance. Any capacitance on the node can be minimized by placing the external resistors as close as possible to the $V_{REF\ ADJ}$ pin and observing good layout practices.

The $V_{REF\ OUT}$ node can drive loads greater than the DAC V_{REF} input requirements and can be used as an excellent system voltage reference. However, to minimize load effects on the DAC system accuracy, it is recommended that a buffer amplifier be used.

Input Amplifier

The DAC reference amplifier is a high gain internally-compensated op amp used to convert the input reference voltage to a

precision bias current for the DAC ladder network.

The Block Diagram details the input reference amplifier and current ladder. The voltage-to-current converter of the DAC amp will generate a 1mA reference current through QR with a 5V V_{REF}. This current sets the input bias to the ladder network. Data bit 9 (DB9)(Q9), when turned on, will mirror this current and will contribute 1mA to the output. DB8 (Q8) will contribute 1/2 of that value or 0.5mA, and so on. These current values act as current sinks and will add at the sum node to produce a DAC ladder to sum node function of:

$$I_{OUT} = \frac{2V_{REF}}{R_{REF}}\left(\frac{DB9}{2} + \frac{DB8}{4} + \frac{DB7}{8} + \frac{DB6}{16} + \frac{DB5}{32} + \frac{DB4}{64} + \frac{DB3}{128} + \frac{DB2}{256} + \frac{DB1}{512} + \frac{DB0}{1024}\right)$$

Because of the fixed internal compensation of the reference amp, the slew rate is limited to typically 0.7V/μs and source impedance at the $V_{REF\ INPUT}$ greater than 5kΩ should be avoided to maintain stability.

The $-V_{REF\ INPUT}$ pin is uncommitted to allow utilization of negative polarity reference voltages. In this mode $+V_{REF\ INPUT}$ is grounded and the negative reference is tied directly to the $-V_{REF\ INPUT}$ contains a 5kΩ resistor that matches a like resistor in the $+V_{REF\ INPUT}$ to reduce voltage offset caused by op amp input bias currents.

Output Amplifier and Interface

The NE5020 provides an on-chip output op amp to eliminate the need for additional external active circuits. Its two-stage design with feed-forward compensation allows it to slew at 15V/μs and settle to within ±1/2LSB in 5μs. These times are typical when driving the rated loads of $R_L \geq 5k$ and C_L 50pF with recommended values of C_{FF} = 1nF and C_{FB} = 30pF. Typical input offset voltages of 5mV and 50kΩ open-loop gain insure that an accurate current-to-voltage conversion is performed when using the on-chip R_{FB} resistor. R_{FB} is matched to R_{REF} and R_{BIP} to maintain accurate voltage gain over operating conditions. The diode shown from ground to sum node prevents the DAC current switches from saturating the op amp during large signal transitions which would otherwise increase the settling time.

The output op amp also incorporates output short circuit protection for both positive and negative excursions. During this fault condition I_{OUT} will limit at ±15mA typical. Recovery from this condition to rated accuracy will be determined by duration of short-circuit and die temperature stabilization.

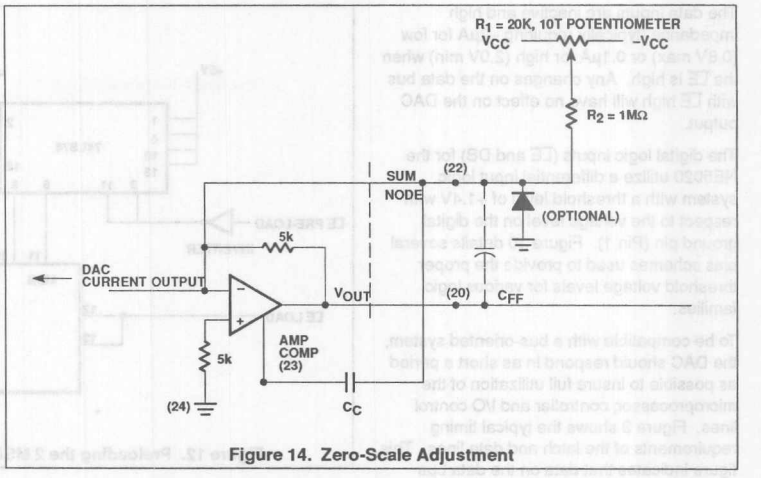


Figure 14. Zero-Scale Adjustment

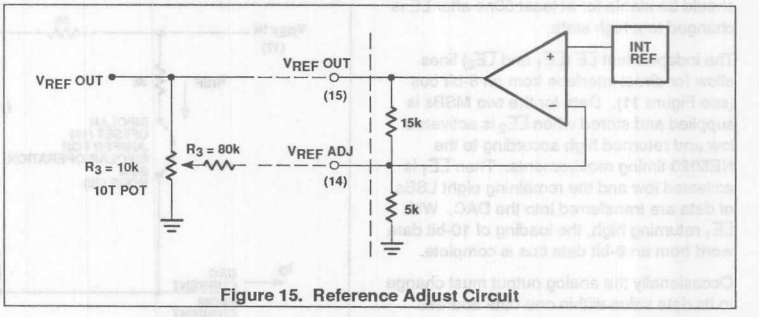


Figure 15. Reference Adjust Circuit

Bipolar Output Voltage

The NE5020 includes a thermally matched resistor, R_{BIP}, to offset the output voltage by 5V to obtain –5V to +5V output voltage range operation. This is accomplished by shorting Pins 18 and 22 (see Figure 13). This connection produces a current equal to $(V_{REFIN} - SUM\ NODE) \div R_{BIP}$ (1mA nominal), which is injected into the sum node. Since full-scale current out is approximately 2mA (1.9980mA), (2mA – 1mA)5kΩ = 5V will appear at the output. For zero DAC output currents, 1mA is still injected into sum node and $V_{OUT} = -(5k\Omega)\ (1mA) = -5V$. Zero-scale adjust and full-scale adjust are performed as described below, noting that full-scale voltage is now approximately +5V. Zero-scale adjust may be used to trim V_{OUT} = 0.00 with the MSB high or V_{OUT} = –5.0V with all bits off.

Zero-Scale Adjustment

The method of trimming the small offset error that may exist when all data bits are low is shown in Figure 14. The trim is the result of injecting a current from resistor R_2 that counteracts the error current. Adjusting potentiometer R_1 until V_{OUT} equals 0.000V in the unipolar mode or –5.000V in the bipolar mode (see bipolar section accomplishes this trim.

Full-Scale Adjustment

A recommended full-scale adjustment circuit, when using the internal voltage reference, is shown in Figure 15. Potentiometer R_3 is adjusted until V_{OUT} equals 9.99023V. In many applications where the absolute accuracy of full-scale is of low importance when compared to the other system accuracy factors this adjustment circuit is optional.

As resistors R_{REF}, R_{FB}, and R_{BIP} shown in the Block Diagram are integrated in close proximity, they match and track in value closely over wide ambient temperature variations. Typical matching is less than ±0.3% which implies that typical full-scale (or gain) error is less than ±0.3% of ideal full-scale value.

10-Bit high-speed multiplying D/A converter NE/SE5410

DESCRIPTION

The NE5410/SE5410 are 10-bit Multiplying Digital-to-Analog Converters pin- and function-compatible with the industry-standard MC3410, but with improved performance. These are capable of high-speed performance, and are used as general-purpose building blocks in cost effective D/A systems.

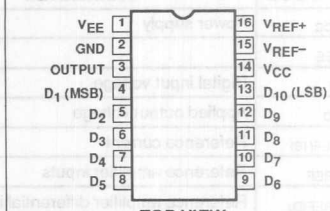
The NE/SE5410 provides complete 10-bit accuracy and differential non-linearity over temperature, and a wide compliance voltage range. Segmented current sources, in conjunction with an R/2R DAC, provide the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

FEATURES

- Pin- and function-compatible with MC3410
- 10-bit resolution and accuracy (±0.05%)
- Guaranteed differential non-linearity over temperature
- Wide compliance voltage range—-2.5 to +2.5V
- Fast settling time—250ns typical
- Digital inputs are TTL- and CMOS-compatible
- High-speed multiplying input slew rate—20mA/μs
- Reference amplifier internally-compensated
- Standard supply voltages +5V and -15V

PIN CONFIGURATION

F Package



TOP VIEW

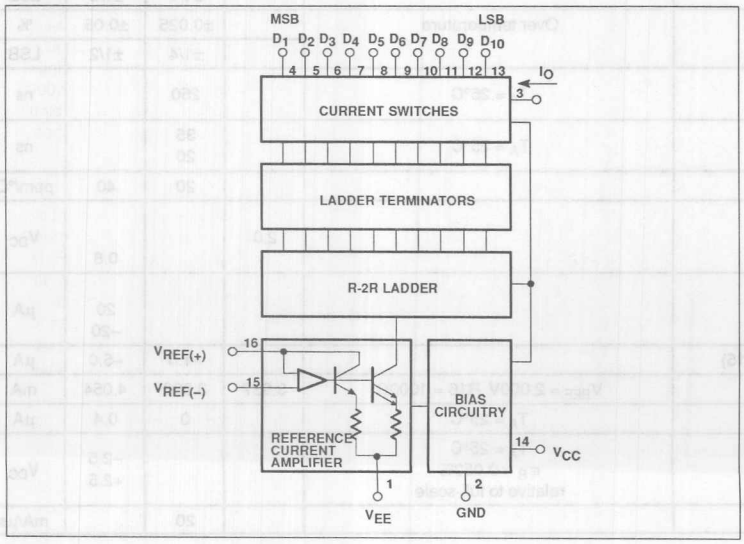
APPLICATIONS

- Successive approximation A/D converters
- High-speed, automatic test equipment
- High-speed modems
- Waveform generators
- CRT displays
- Strip CHART and X-Y plotters
- Programmable power supplies
- Programmable gain and attenuation

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	NE5410F
16-Pin Cerdip	-55 to +125°C	SE5410F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

T_A=+25°C, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	+7.0	V_{DC}
V_{EE}		-18	V_{DC}
V_I	Digital input voltage	+15	V_{DC}
V_O	Applied output voltage	+4, -5.0	V_{DC}
$I_{REF(16)}$	Reference current	2.5	mA
V_{REF}	Reference amplifier inputs	V_{CC}, V_{EE}	V_{DC}
$V_{REF(D)}$	Reference amplifier differential inputs	0.7	V_{DC}
T_A	Operating temperature range		
	SE5410	-55 to +125	°C
	NE5410	0 to +70	°C
T_J	Junction temperature		
	Ceramic package	+150	°C
T_{STG}	Storage temperature	-65 to +150	°C
P_D	Maximum power dissipation T_A=25°C (still-air)[1]	1190	mW

NOTES:
1. Derate above 25°C at the following rate:
   F package at 9.5mW/°C

DC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC}=+5.0V_{DC}, V_{EE}=-15V_{DC}, I_{REF}=2.0mA, all digital inputs at high logic level. SE5410: T_A=-55°C to +125°C, NE5410 Series: T_A=0°C to +70°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
ϵ_R	Relative accuracy	Over Temperature		±0.025	±0.05	%
	(Error relative to full scale I_O)			±1/4	±1/2	LSB
	Differential non-linearity	Over temperature		±0.025	±0.05	%
				±1/4	±1/2	LSB
I_S	Settling time to within ±1/2 LSB (all bits low to high)	T_A = 25°C		250		ns
t_{PLH} t_{PHL}	Propagation delay time	T_A = 25°C		35 20		ns
TCI_O	Output full-scale current drift			20	40	ppm/°C
V_{IH}	Digital input logic levels (all bits) High level, Logic "1" Low level, Logic "0"		2.0		 0.8	V_{DC}
I_{IH} I_{IL}	Digital input current (all bits) High level, V_{IH} = 5.5V Low level, V_{IL} = 0.8V				 20 –20	µA
$I_{REF(15)}$	Reference input bias current (Pin 15)			–1.0	–5.0	µA
I_{OH}	Output current (all bits high)	V_{REF} = 2.000V, R16 = 1000Ω	3.937	3.996	4.054	mA
I_{OL}	Output currents (all bits low)	T_A = 25°C		0	0.4	µA
V_O	Output voltage compliance	T_A = 25°C ϵ_R < 0.050% relative to full-scale			–2.5 +2.5	V_{DC}
SR I_{REF}	Reference amplifier slew rate			20		mA/µs

DC ELECTRICAL CHARACTERISTICS

V_{CC}=+5.0V_{DC}, V_{EE}=-15V_{DC}, I_{REF}=2.0mA, all digital inputs at high logic level. SE5410: T_A=-55°C to +125°C, NE5410 Series: T_A=0°C to +70°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
ST I_{REF}	Reference amplifier settling time	0 to 4.0mA, ±0.1%		2.0		µs
PSRR(–)	Output current power supply sensitivity			0.003	0.01	%/%
C_O	Output capacitance	V_O = 0		25		pF
C_I	Digital input capacitance (all bits high)			4.0		pF
I_{CC} I_{EE}	Power supply current (all bits low)			+2 –12	+4 –18	mA
V_{CC} V_{EE}	Power supply votlage range	T_A = 25°C V_O = 0	+4.75 –14.25	+5.0 –15	+5.25 –15.75	V_{DC}
	Power consumption			190	300	mW

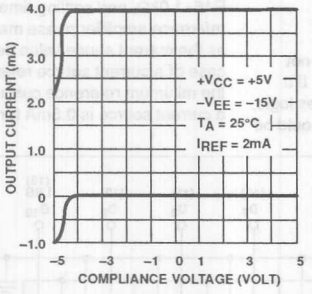


Figure 1. Output Current vs Output Compliance Voltage

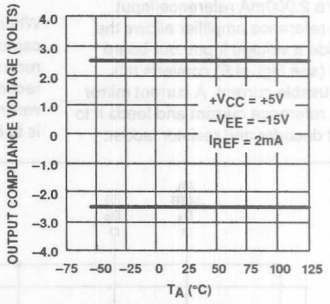


Figure 2. Maximum Output Compliance Voltage vs Temperature

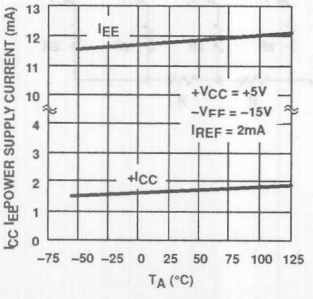


Figure 3. Power Supply Currents vs Temperature

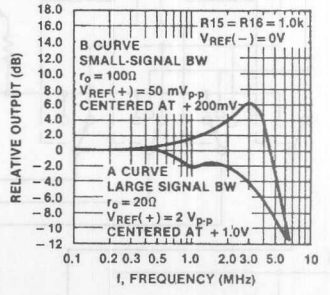


Figure 4. Reference Amplifier Frequency Response

CIRCUIT DESCRIPTION

The NE5410 consists of four segment current sources which generate the 2 Most Significant Bits (MSBs), and an R/2R DAC implemented with ion-implanted resistors for scaling the remaining 8 Least Significant Bits (LSBs) (see Figure 5). This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully-differential current switches. The switches use current steering for speed.

An on-chip high slew reference current amplifier drives the R/2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input: out-board resistor R16 (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder.

Thus, for a reference voltage of 2.0V and a 1kΩ resistor tied to Pin 16, the full-scale current is approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R16 should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3V above the V_{EE} supply voltage for best operation. Bipolar input signals may be handled by connecting R16 to a positive voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R16 should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1μF capacitor to ground.

The reference amplifier is internally-compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R16 and reference voltages which supply 2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R16 increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R16=1.0kΩ, and settling time is ±10μs. The reference amplifier phase margin decreases as the current souce value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

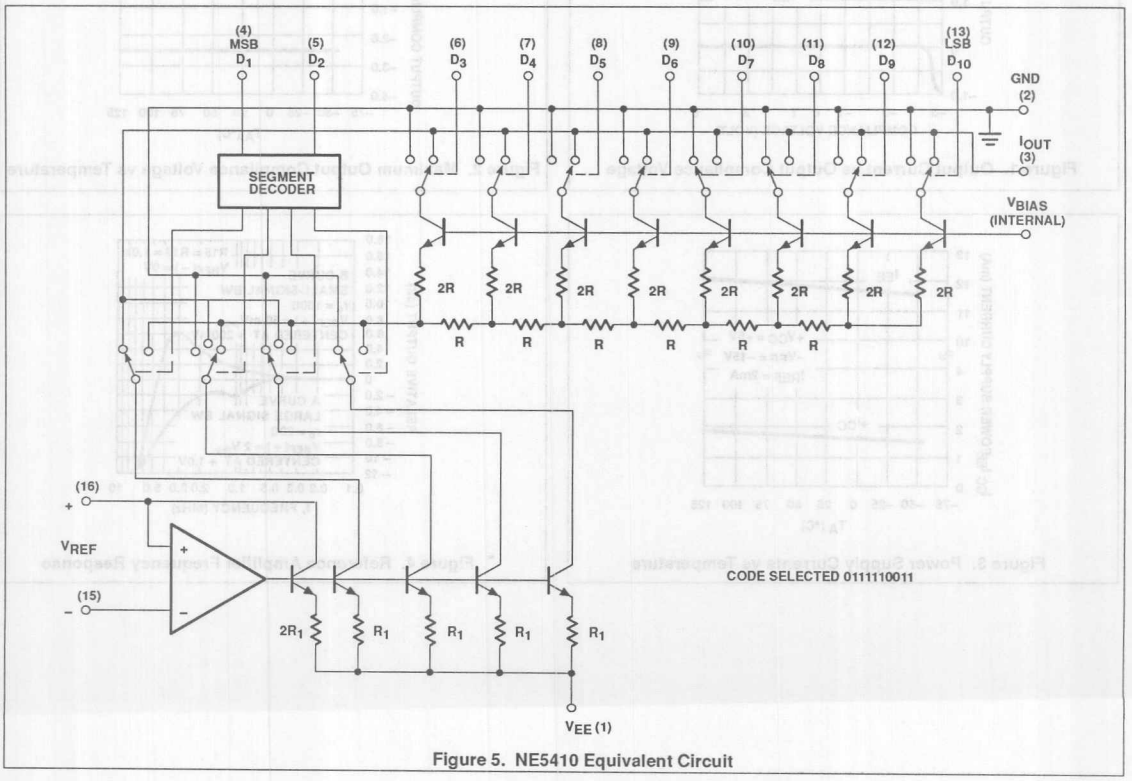


Figure 5. NE5410 Equivalent Circuit

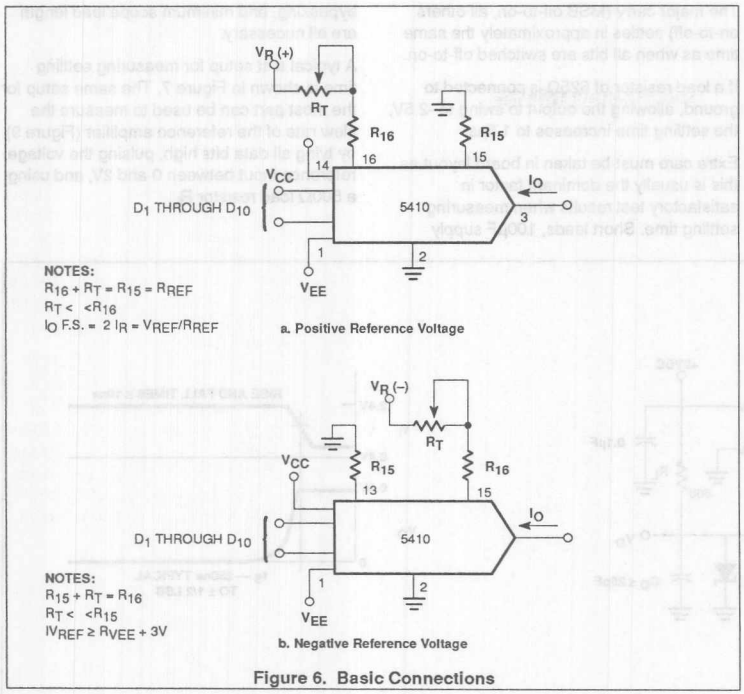


Figure 6. Basic Connections

OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from -2.5 to +2.5V. As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if V_{EE}>-15V.

ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full-scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full-scale current. The relative accuracy of the NE5410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full-scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the NE5410 has a low full-scale current drift with temperature.

The SE5410 and the NE5410 are accurate to within ± LSB at 25°C with a reference current of 2.0mA on Pin 16.

MONOTONICITY

The NE5410 and SE5410 are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

SETTLING TIME

The worst-case switching condition occurs when all bits are switched "on," which corresponds to a LOW-to-HIGH transition for all bits. This time is typically 250ns for the output to settle to within ± 1/2LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (<0.7V) swing and the external output capacitance is under 25pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

If a load resistor of 625Ω is connected to ground, allowing the output to swing to -2.5V, the settling time increases to 1.5μs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing, and minimum scope lead length are all necessary.

A typical test setup for measuring settling time is shown in Figure 7. The same setup for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 500Ω load resistor R_L.

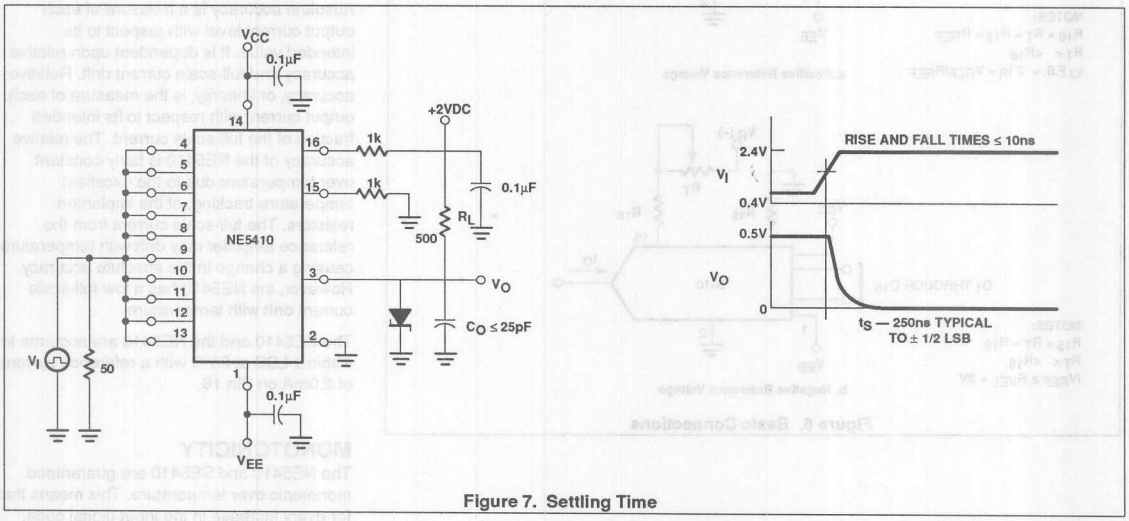


Figure 7. Settling Time

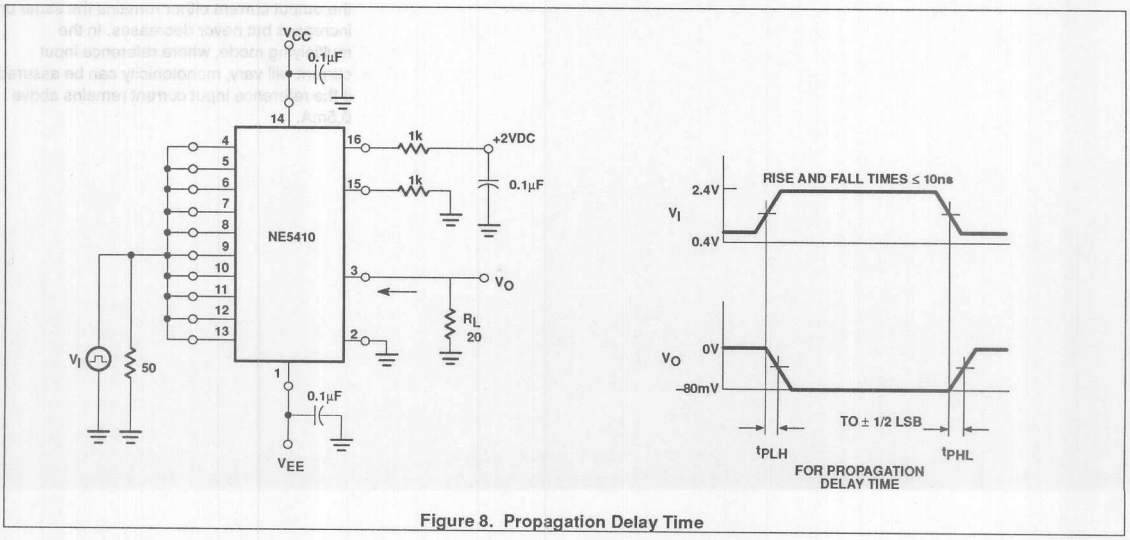


Figure 8. Propagation Delay Time

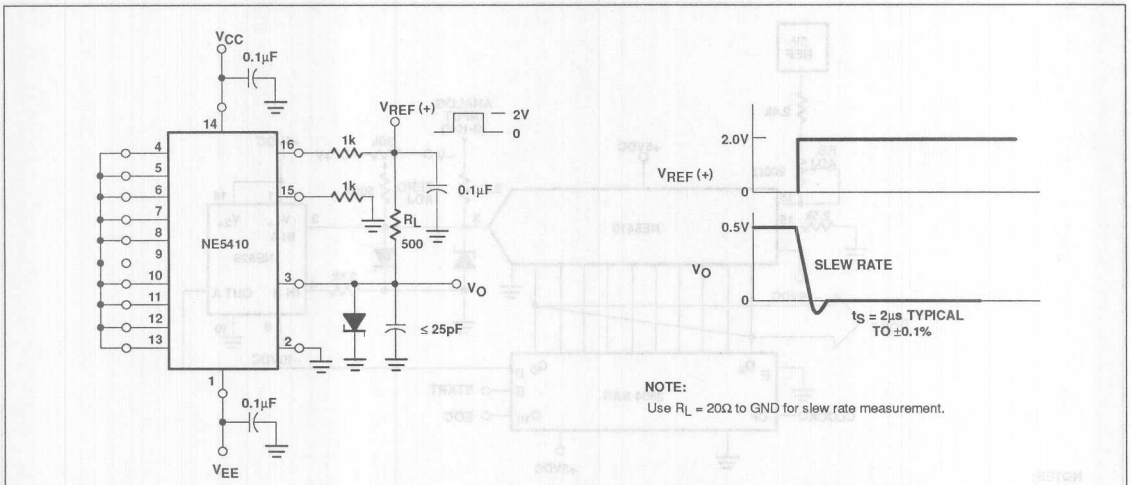


Figure 9. Reference Amplifier Settling Time and Slew Rate

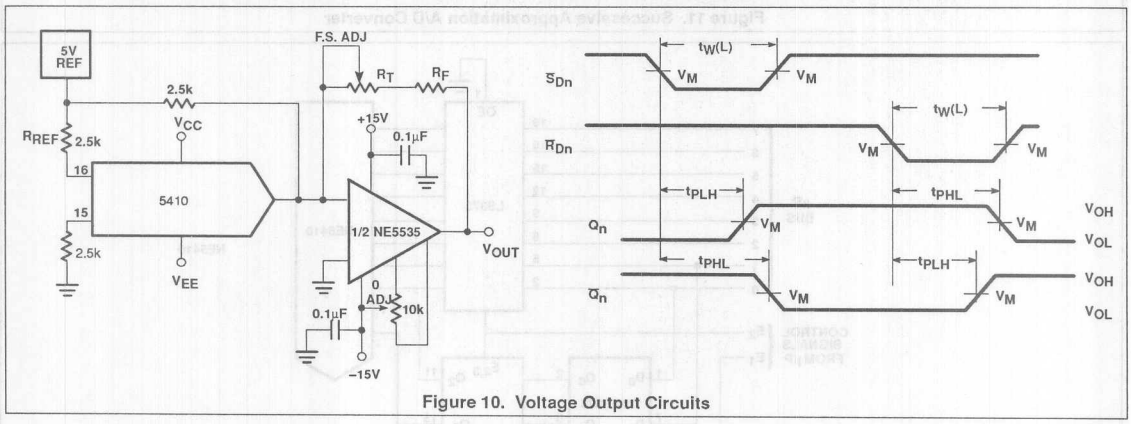
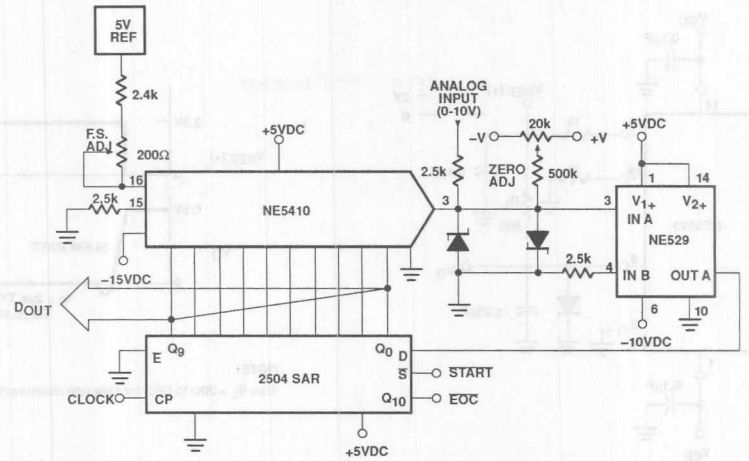
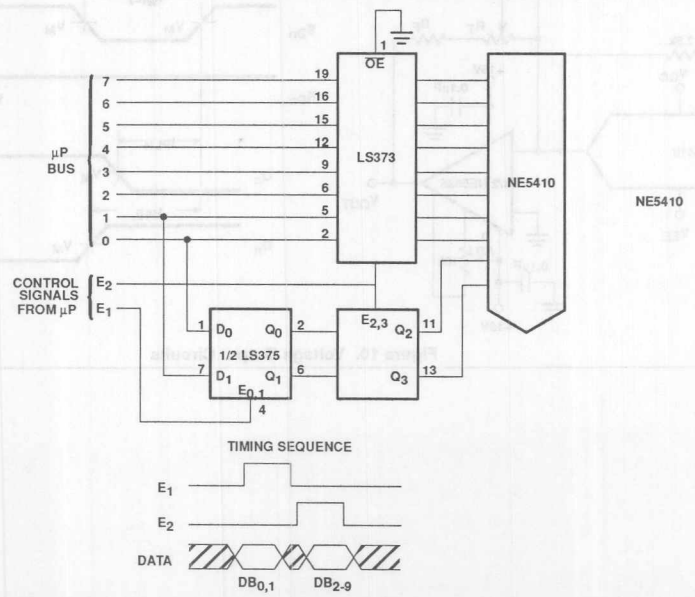


Figure 10. Voltage Output Circuits



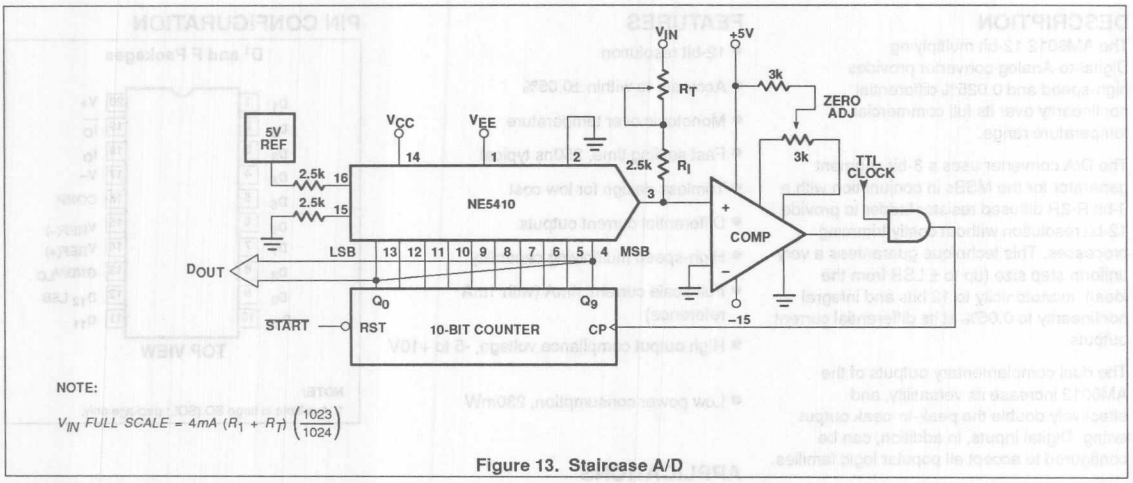
NOTES:
10-bit conversion time = 3.3μs with 3MHz clock.
This converter uses a 2504 12-bit successive approximation register in the short cycle operating mode where the end of conversion signal is taken from the first unused bit of the SAR (Q_{10}).

Figure 11. Successive Approximation A/D Converter



NOTES:
With this double latch technique, valid data will be latched to the DAC until updated with the E_2 pulse. Timing will depend on the processor used.

Figure 12. 8-Bit μP Bus Interface



NOTE:

V_{IN} FULL SCALE = $4mA\ (R_1 + R_T)\left(\frac{1023}{1024}\right)$

Figure 13. Staircase A/D

DESCRIPTION

The AM6012 12-bit multiplying Digital-to-Analog converter provides high-speed and 0.025% differential nonlinearity over its full commercial temperature range.

The D/A converter uses a 3-bit segment generator for the MSBs in conjunction with a 9-bit R-2R diffused resistor ladder to provide 12-bit resolution without costly trimming processes. This technique guarantees a very uniform step size (up to ± LSB from the ideal), monotonicity to 12 bits and integral nonlinearity to 0.05% at its differential current outputs.

The dual complementary outputs of the AM6012 increase its versatility, and effectively double the peak-to-peak output swing. Digital inputs, in addition, can be configured to accept all popular logic families.

While the device requires a reference input of 1mA for a 4mA full-scale current, operation is nearly independent of power supply voltage shifts. The power supply rejection ratio is ±0.001% FS/% ΔV. The devices will work from +5, -12V to ±18V rails, with as low as 230mW power consumption typical.

FEATURES

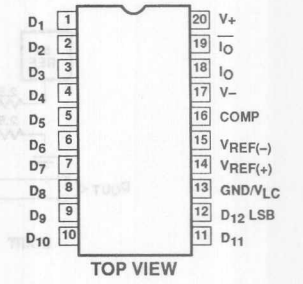
- 12-bit resolution
- Accurate to within ±0.05%
- Monotonic over temperature
- Fast settling time, 250ns typical
- Trimless design for low cost
- Differential current outputs
- High-speed multiplying capability
- Full-scale current, 4mA (with 1mA reference)
- High output compliance voltage, -5 to +10V
- Low power consumption, 230mW

APPLICATIONS

- CRT displays, computer graphics
- Robotics and machine tools
- Automatic test equipment
- Programmable power supplies
- CAD/CAM systems
- Data acquisition and control systems
- Analog-to-digital converter systems

PIN CONFIGURATION

D[1] and F Packages



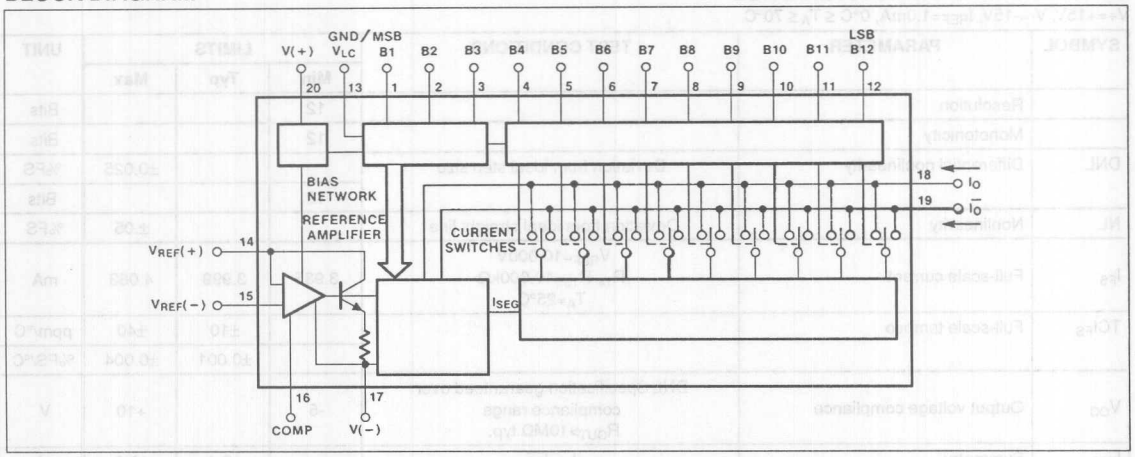
TOP VIEW

NOTE:
1. Available in large SO (SOL) package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Cerdip	0 to +70°C	AM6012F
20-Pin Plastic SOL	0 to +70°C	AM6012D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating temperature		
	AM6012F	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature 10sec max	300	°C
V_S	Power supply voltage	±18	V
	Logic inputs	-5V to +18	V
	Voltage across current outputs	-8V to +12	V
V_{REF}	Reference inputs V_{14}, V_{15}	V- to V+	
V_{REF}	Reference input differential voltage (V_{14} to V_{15})	±18	V
I_{REF}	Reference input current (I_{14})	1.25	mA
P_D	Maximum power dissipation, T_A=25°C, (still-air)[1]		
	F package	1560	mW
	D package	1390	mW

NOTES:
1. Derate above 25°C, at the following rate:
   F package at 12.5mW/°C
   D package at 11.1mW/°C

DC ELECTRICAL CHARACTERISTICS

$V+=+15V$, $V-=-15V$, $I_{REF}=1.0mA$, $0°C \leq T_A \leq 70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		12			Bits
	Monotonicity		12			Bits
DNL	Differential nonlinearity	Deviation from ideal step size			±0.025	%FS
			12			Bits
NL	Nonlinearity	Deviation from ideal straight line			±.05	%FS
I_{FS}	Full-scale current	$V_{REF}=10.000V$ R_{14}-$R_{15}=10.000k\Omega$ $T_A=25°C$	3.935	3.999	4.063	mA
TCI_{FS}	Full-scale tempco			±10	±40	ppm/°C
				±0.001	±0.004	%FS/°C
V_{OC}	Output voltage compliance	DNL Specification guaranteed over compliance range $R_{OUT}>10M\Omega$ typ.	-5		+10	V
I_{FSS}	Symmetry	I_{FS}-$\overline{I_{FS}}$		±0.4	±2.0	µA
I_{ZS}	Zero-scale current				0.10	µA
V_{IL} V_{IH}	Logic input levels — Logic "0"				0.8	V
	Logic input levels — Logic "1"		2.0			
I_{IN}	Logic input current	$V_{IN}=-5$ to $+18V$			40	µA
V_{IS}	Logic input swing	$V-=-15V$	-5		+18	V
I_{REF}	Reference current range		0.2	1.0	1.1	mA
I_{15}	Reference bias current		0	-0.5	-2.0	µA
dI/dt	Reference input slew rate	$R_{14(eq)}=800\Omega$ $C_C=0pF$	4.0	8.0		mA/µs
$PSSI_{FS+}$	Power supply sensitivity	$V+=+13.5V$ to $+16.5V$, $V-=-15V$		±0.0005	±0.001	%FS/%
$PSSI_{FS-}$		$V-=-13.5V$ to $-16.5V$, $V+=+15V$		±0.00025	±0.001	
V+	Power supply range	$V_{OUT}=0V$	4.5		18	V
V-			-18		-10.8	
I+	Power supply current	$V+=+5V$, $V-=-15V$		5.7	8.5	mA
I-				-13.7	-18.0	
I+		$V+=+15V$, $V-=-15V$		5.7	8.5	
I-				-13.7	-18.0	
P_D	Power dissipation	$V+=+5V$, $V-=-15V$		234	312	mW
		$V+=+15V$, $V-=-15V$		291	397	

AC ELECTRICAL CHARACTERISTICS

$V+=+15V$, $V-=-15V$, $I_{REF}=1.0mA$, $0°C \leq T_A \leq 70°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
t_S	Settling time	To ± 1/2LSB, all bits ON or OFF, $T_A=25°C$		250	500	ns
t_{PLH} t_{PHL}	Propagation delay—all bits	50% to 50%		25	50	ns
C_{OUT}	Output capacitance			20		pF

CIRCUIT DESCRIPTION

The AM6012 is a 12-bit DAC which uses diffused resistors and requires no trimming to guarantee monotonicity over the temperature range. A segmented DAC design guarantees a more uniform step size over the temperature range than is normally available with trimmed 12-bit converters. The converter features differential high compliance current outputs, wide supply range, and a multiplying reference input.

In many converter applications, uniform step size is more important than conformance to an ideal straight line. Many 12-bit converters are used for high resolution rather than high linearity, since few transducers are more linear than ±0.1%. All classic binarily weighted converters require ±1/2LSB (±0.012%) linearity in order to guarantee monotonicity, which requires very tight resistor matching and tracking. The AM6012 uses conventional bipolar processing to achieve high differential linearity and monotonicity without requiring correspondingly high linearity, or conformance to an ideal straight line.

One design approach which provides monotonicity without requiring high linearity is the MOS switch-resistor string. This circuit is actually a full complement to a current-switched R-2R DAC since it is slower, has a voltage output, and, if implemented at the 12-bit level, would use 4096 low tolerance resistors rather than a minimum number of high tolerance resistors as in the R-2R network. Its lack of speed and density for 12 bits are its drawbacks.

With the segmented DAC approach, the 4096 required output levels are composed of 8 groups of 512 steps each. Each step group is generated by a 9-bit DAC, and each of the segment slopes is determined by one of 8 equal current sources. The resistors which determine monotonicity are in the 9-bit DAC. The major carry of the 9-bit DAC is repeated in each of the 8 segments, and requires eight times lower initial resistor accuracy and tracking to maintain a given differential nonlinearity over temperature.

The operation of the segmented DAC may be visualized by assuming an input code of all zeroes. The first segment current I_O is divided into 512 levels by the 9-bit multiplying DAC and fed to the output, I_{OUT}. As the input code increases, a new segment current is selected for each 512 counts. The previous segment is fed to output I_{OUT} where the new step group is added to it, thus ensuring monotonicity independent of segment resistor values. All higher order segments feed $\overline{I_{OUT}}$.

With the segmented DAC approach, the precision of the 8 main resistors determines linearity only. The influence of each of these resistors on linearity is four times lower than that of the MSB resistor in an R-2R DAC. Hence, assuming the same resistor tolerances for both, the linearity of the segmented approach would actually be higher than that of an R-2R design.

The step generator or 9-bit DAC is composed of a master and a slave ladder. The slave ladder generates the four least significant bits from the remainder of the master ladder by active current splitting utilizing scaled emitters. This saves ladder resistors and greatly reduces the range of emitter scaling required in the 9-bit DAC. All current switches in the step generator are high-speed fully-differential switches which are capable of switching low currents at high speed. This allows the use of a binary scaled network all the way to the least significant bit which saves power and simplifies the circuitry.

Diffused resistors have advantages over thin film resistors beyond simple economy and bipolar process compatibility. The resistors are fabricated in single crystal rather than amorphous material which gives them better long term stability and tracking and much higher moisture resistance. They are diffused at 1000°C and so are resistant to changes in value due to thermal and chemical causes. Also, no burn-in is required for stability. The contact resistance between aluminum and silicon is more predictable than between aluminum and an amorphous thin film, and no sandwich metals are required to enhance or protect the contact or limit alloying. The initial match between two diffused resistors is similar to that of thin film since both are defined by photomasks and chemical etching. Since the resistors are not trimmed or altered after fabrication, their tracking and long-term characteristics are not degraded.

DIFFERENTIAL VS INTEGRAL NONLINEARITY

Integral nonlinearity, for the purposes of the discussion, refers to the "straightness" of the line drawn through the individual response points of a data converter. Differential nonlinearity, on the other hand, refers to the deviation of the spacing of the adjacent points from a 1 LSB ideal spacing. Both may be expressed as either a percentage of full-scale output or as fractional LSBs or both. The graphs in Figure 1 define the manner in which these parameters are specified. The left graph shows a portion of the transfer curve of a DAC with 1/2LSB INL and the (implied) DNL spec of 1 LSB. Below this is a graphic representation of the way this would appear on a CRT screen where the AM6012 is used as a display driver. On the right is a portion of the transfer curve of a DAC specified for 1/2LSB INL with LSB DNL specified and the graphic display below it.

One of the characteristics of an R-2R DAC in standard form is that any transition which causes a zero LSB change (i.e., the same output for two different codes) will exhibit the same output each time that transition occurs. The same holds true for transitions causing a 2 LSB change. These two problem transitions are allowable for the standard definition of monotonicity and also allow the device to be specified very tightly for INL. The major problem arising from this error type is in A/D converter implementations. Inputs producing the same output are now represented by ambiguous output codes for an identical input. Also, two LSB gaps can cause large errors at those input levels (assuming 1/2LSB quantizing levels). It can be seen from the two figures that the DNL-specified D/A converter will yield much finer grained data than the INL-specified part, thus improving the ability of the A/D to resolve changes in the analog input.

DIFFERENTIAL LINEARITY COMPARISON

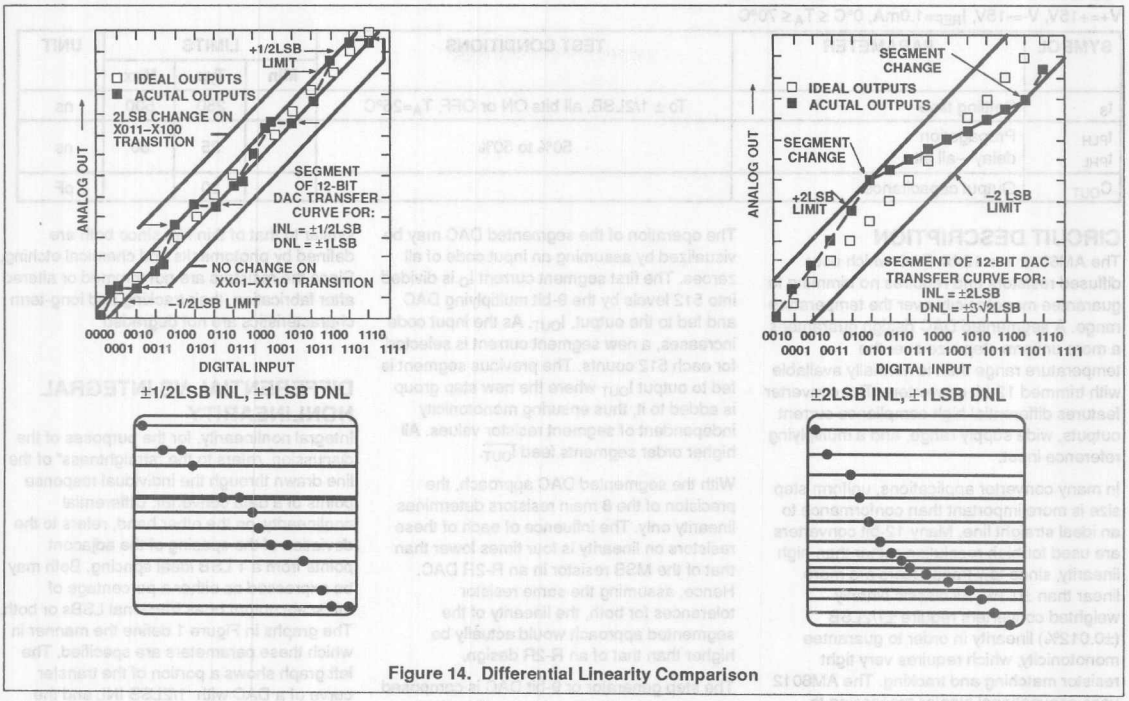


Figure 14. Differential Linearity Comparison

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O+\overline{I_O}=I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at Pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at Pin 18 and turned on at Pin 19. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required, it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V- and is independent of the positive supply. Negative compliance is +10V above V-.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The AM6012 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V- supplies of -10V or less, $I_{REF}\leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -9V with $I_{REF}=1mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the AM6012 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc., remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the AM6012 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full-scale drift.

SETTLING TIME

The AM6012 is capable of extremely fast settling times, typically 250ns at $I_{REF}=1.0mA$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within LSB of the

LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ns. The output capacitance of the AM6012 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if R_L>500Ω.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±2μA, therefore a 2.5kΩ load is needed to provide adequate drive for most oscilloscopes. At I_{REF} values of less than 0.5mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 011111111111 to 100000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.1% of the final value, and thus settling times may be observed at lower values of I_{REF}.

AM6012 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

APPLICATIONS INFORMATION

Reference Amplifier Setup

The AM6012 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999\ I_{REF}$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (Pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at Pin 15. Reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at Pin 15. The voltage at Pin 14 is equal to and tracks the voltage at Pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors (Figure 2a).

Bipolar references may be accommodated by offsetting V_{REF} or Pin 15. The negative common-mode range of the reference amplifier is given by: V_{CM}=V- plus (I_{REF}×3kΩ) plus 1.8V. The positive common-mode range is V+ less 1.23V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}.

MULTIPLYING OPERATION

The AM6012 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 1.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V-. The value of this capacitor depends on the impedance presented to Pin 14. For R14 values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 5, 12 and 25pF. Larger values of R14 require proportionately increased values of CC for proper phase margin (see Figure 2b).

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If Pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14}=1kΩ and C_C=5pF, the reference amplifier slews at 4mA/ms enabling a transition from I_{REF}=0 to I_{REF}=1mA in 250ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF}=0) condition. Full-scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at Pin 14 is 800Ω and C_C=0. This yields a reference slew rate of 8mA/μs which is relatively independent of R_{IN} and V_{IN} values.

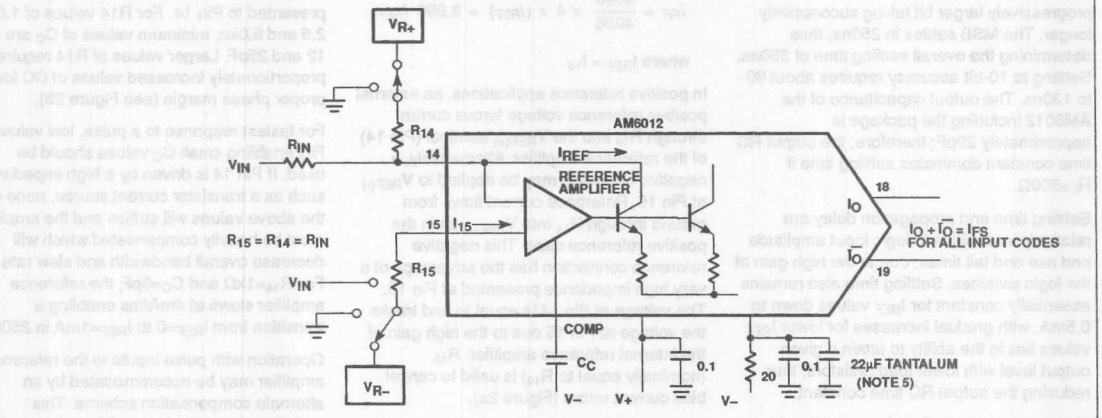
LOGIC INPUTS

The AM6012 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40μA logic input current, and completely adjustable logic threshold voltage. For V-=-15V, the logic inputs may swing between -5 and +10V. This enables direct interface with +15V CMOS logic, even when the AM6012 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by:

V- plus (I_{REF}×3kΩ) plus 1.8V.

The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (Pin 13, V_{LC}). For TTL interface, simply ground Pin 13. When interfacing ECL, an I_{REF}≤1mA is recommended. For general setup of the logic control circuit, it should be noted that Pin 13 will sink 1.1mA typical. External circuitry should be designed to accommodate this current (Figure 3).

12-Bit multiplying D/A converter | AM6012



REFERENCE CONFIGURATION	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive reference	V_{R+}	0V	N/C	0.01µF	V_{R+}/R_{14}
Negative reference	0V	V_{R-}	N/C	0.01µF	$-V_{R-}/R_{14}$
Lo impedance bipolar reference	V_{R+}	0V	V_{IN}[1]		$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})^2$
Hi impedance bipolar reference	V_{R+}	V_{IN}	N/C[1]		$(V_{R+} - R_{IN}) / R_{14}$[3]
Pulsed reference[4]	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

NOTES:

1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least 5pF x $R_{14(eq)}$ in kΩ. For R_{14} < 800Ω no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+} / R_{14} must be greater than $-V_{IN}$ max / R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than $-V_{IN}$ max so the amplifier is not turned off.
4. For pulsed opeartion, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at Pin 14 should be 800Ω or less.
5. For optimum settling time, decouple V– with 20Ω and bypass with 22µF tantulum capacitor.
6. Reference current and reference resistor — there is a 1-to-4 scale factor between the reference current (I_{REF}) and the full-scale output current (IFS).
   If V_{REF} = +10V and I_{FS} = 4mA, the value of the R_{14} is:

$$R_{14} = \frac{4\ x\ 10V}{4mA} = 10k\Omega \qquad R_{14} = R_{15}$$

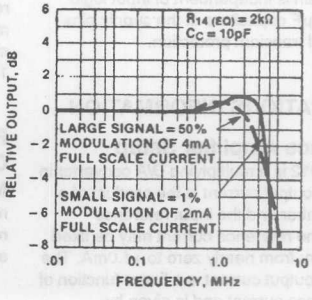
a. Reference Amplifier Biasing

Minimum Size Compensation Capacitor
(I_{FS} = 4mA, I_{REF} = 1.0mA)

$R_{14(EQ)}$ (kΩ)	C_C (pF)
10	50
5	25
2	10
1	5
.5	0

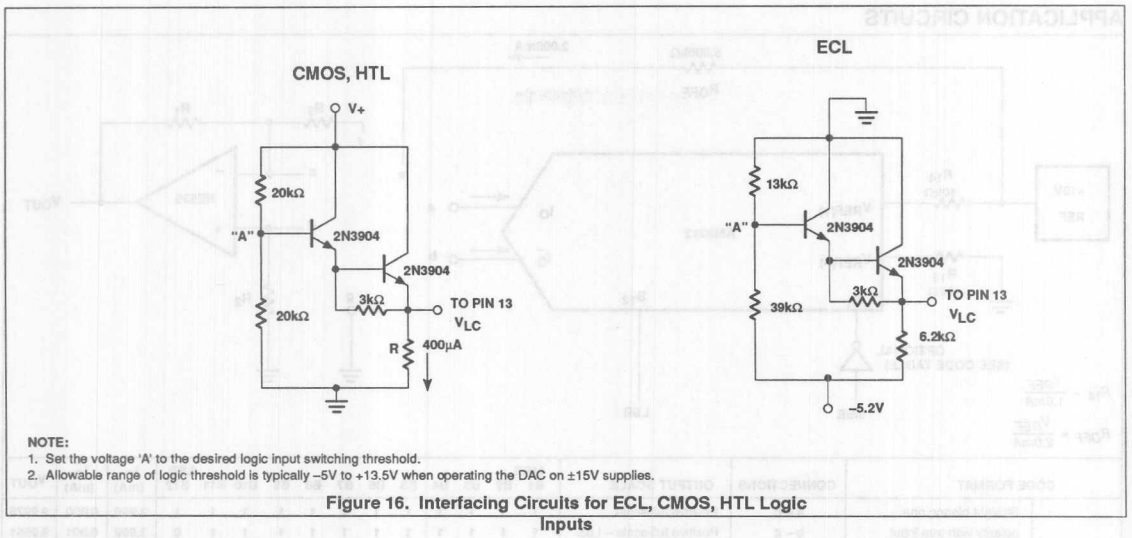
NOTE:
A 0.01µF capacitor is recommended for fixed reference operation.

Reference Amplifier Frequency Response



b.

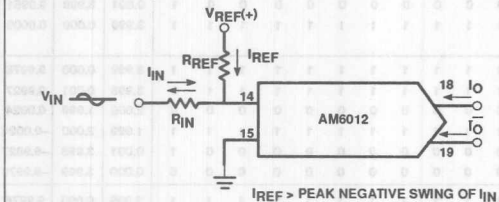
Figure 15.



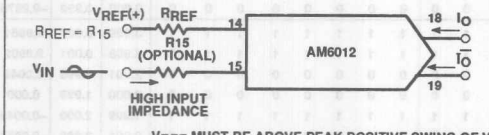
NOTE:
1. Set the voltage 'A' to the desired logic input switching threshold.
2. Allowable range of logic threshold is typically –5V to +13.5V when operating the DAC on ±15V supplies.

Figure 16. Interfacing Circuits for ECL, CMOS, HTL Logic Inputs

ACCOMMODATING BIPOLAR REFERENCE

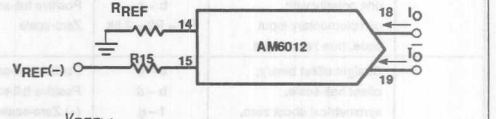


NOTE:
I_{REF} > Peak negative swing of I_{IN}.



NOTE:
$V_{REF(+)}$ Must be above peak positive swing of V_{IN}.

BASIC NEGATIVE REFERENCE OPERATION



$$I_{FS} \approx \frac{V_{REF(-)}}{R_{REF}} \times 4$$

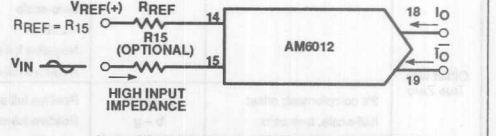
NOTE:
R_{REF} SETS I_{FS}; R15 IS FOR A BIAS CURRENT CANCELLATION

NOTE:

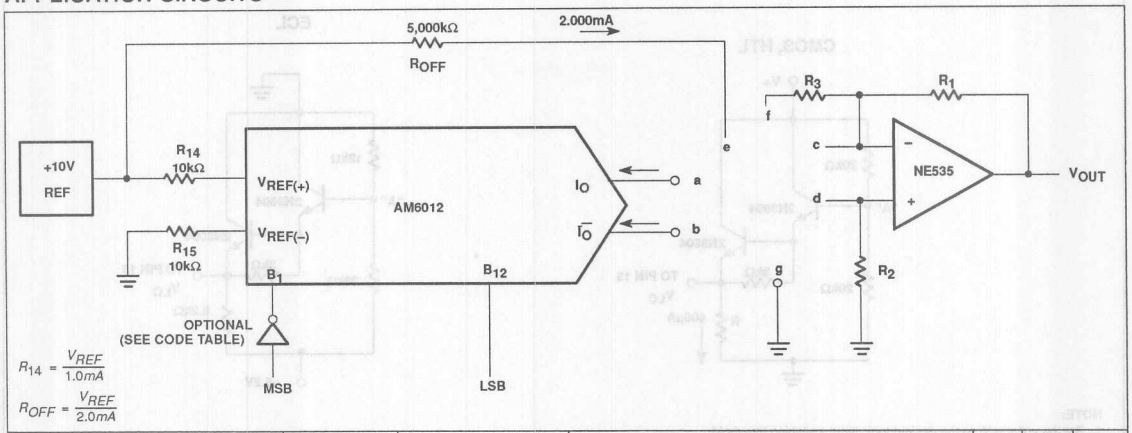
$$I_{FS} \approx \frac{V_{REF(-)}}{R_{REF}} \times 4$$

R_{REF} sets I_{FS}; R15 is for a bias current cancellation.

RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT



APPLICATION CIRCUITS



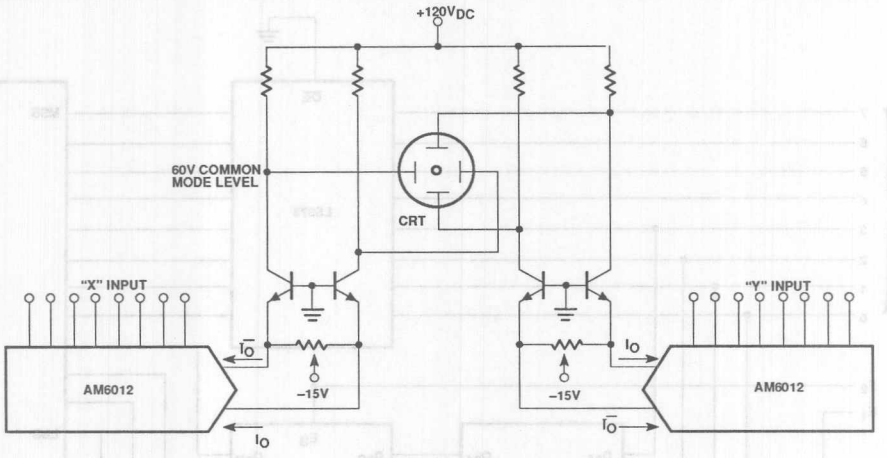
CODE FORMAT		CONNECTIONS	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	IO (mA)	$\overline{IO}$ (mA)	VOUT
Unipolar	Straight binary; one polarity with true input code, true zero output.	a – c	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
		b – g	Positive full-scale – LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
		R1 = R2 = 2.5k	Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
	Complementary binary; one polarity with complementary input code, true zero output.	a – g	Positive full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
		b – c	Positive full-scale – LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
		R1 = R2 = 2.5k	Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000
Symmetrical Offset	Straight offset binary; offset half-scale, symmetrical about zero, no true zero output.	a – c	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
		b – d	Positive full-scale – LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
		f – g	(+) Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
		R1 = R3 = 2.5k	(–) Zero-scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0024
		R2 = 1.25k	Negative full-scale – LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9927
			Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–9.9976
	1's complement; offset half-scale, symmetrical about zero, no true zero output, MSB complemented (need inverter at B1).	a – c	Positive full-scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
		b – d	Positive full-scale – LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
		f – g	(+) Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
		R1 = R3 = 2.5k	(–) Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0024
		R2 = 1.25k	Negative full-scale – LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9927
			Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–9.9976
Offset with True Zero	Offset binary; offset half-scale, true zero output.	e – a – c	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
		b – g	Positive full-scale – LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
		R1 = R2 = 5k	+ LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
			Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
			– LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.0049
			Negative full-scale + LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9951
			Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–10.000
	2's complement; offset half-scale, true zero output, MSB complemented (need inverter at B1).	e – a – c	Positive full-scale	0	1	1	1	1	1	1	1	1	1	1	1			
		b – g	Positive full-scale – LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
		R1 = R2 = 5k	+ 1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
			Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000
			– 1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	–0.049
			Negative full-scale + LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	–9.9951
			Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	–10.000

Figure 17. AM6012 Logic Inputs

ADDITIONAL CODE MODIFICATIONS

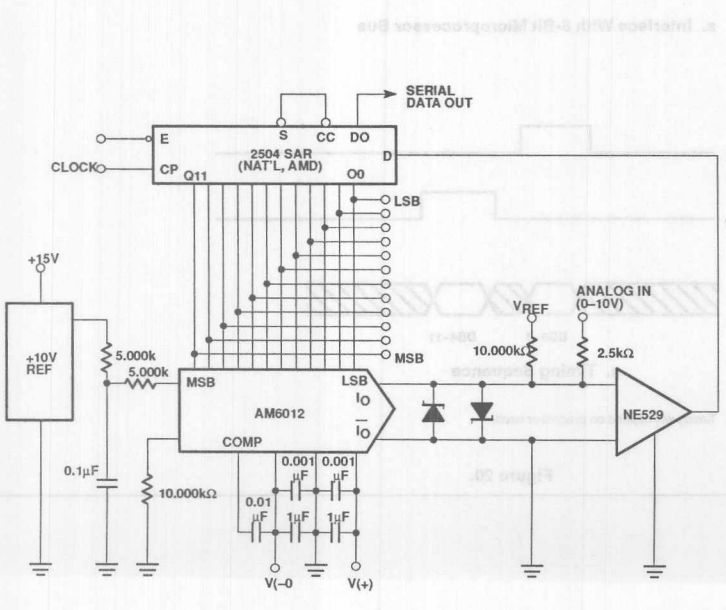
1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

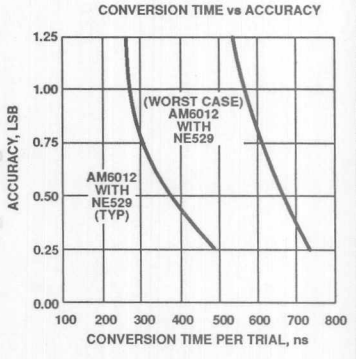
APPLICATION CIRCUITS



NOTES:
1. Full differential drive lowers power supply voltage.
2. Eliminates inverting amplifiers and transformers.
3. Independent beam centering controls.

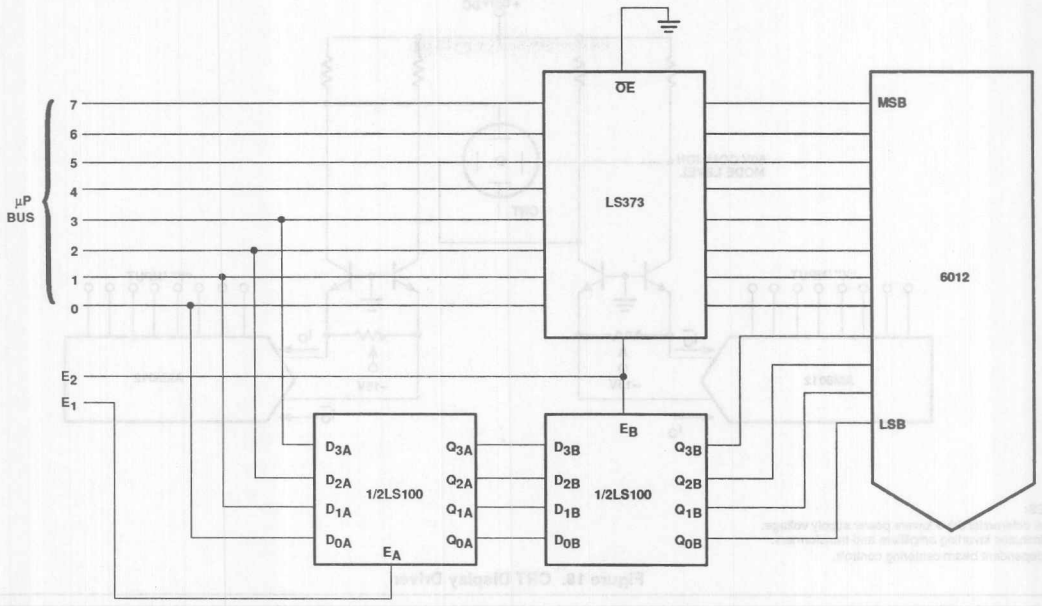
Figure 18. CRT Display Driver



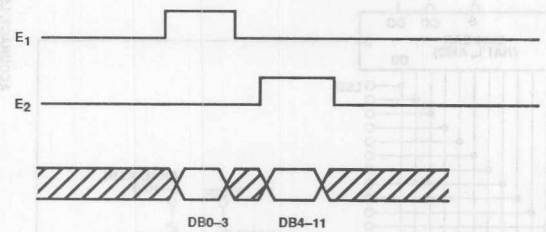


CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
NE529	100	150
TOTAL	383ns	705ns
X 13	5.0μs	9.1μs

Figure 19. 12-Bit High-Speed A/D Converter



a. Interface With 8-Bit Microprocessor Bus



a. Timing Sequence

NOTE:
Data remains on inputs of DAC until updated by E2 pulse. Timing will depend on processor used.

Figure 20.

Stereo high-performance 16-bit DAC

TDA1541A

FEATURES

- High sound quality
- High performance: low noise and distortion, wide dynamic range
- 4 x or 8 x oversampling possible
- Selectable two-channel input format
- TTL compatible inputs

GENERAL DESCRIPTION

The TDA1541A is a stereo 16-bit digital-to-analog converter (DAC). The ingenious design of the electronic circuit guarantees a high performance and superior sound quality. The TDA1541A is therefore extremely suitable for use in top-end high-fi digital audio equipment such as high quality Compact Disc players or digital amplifiers.

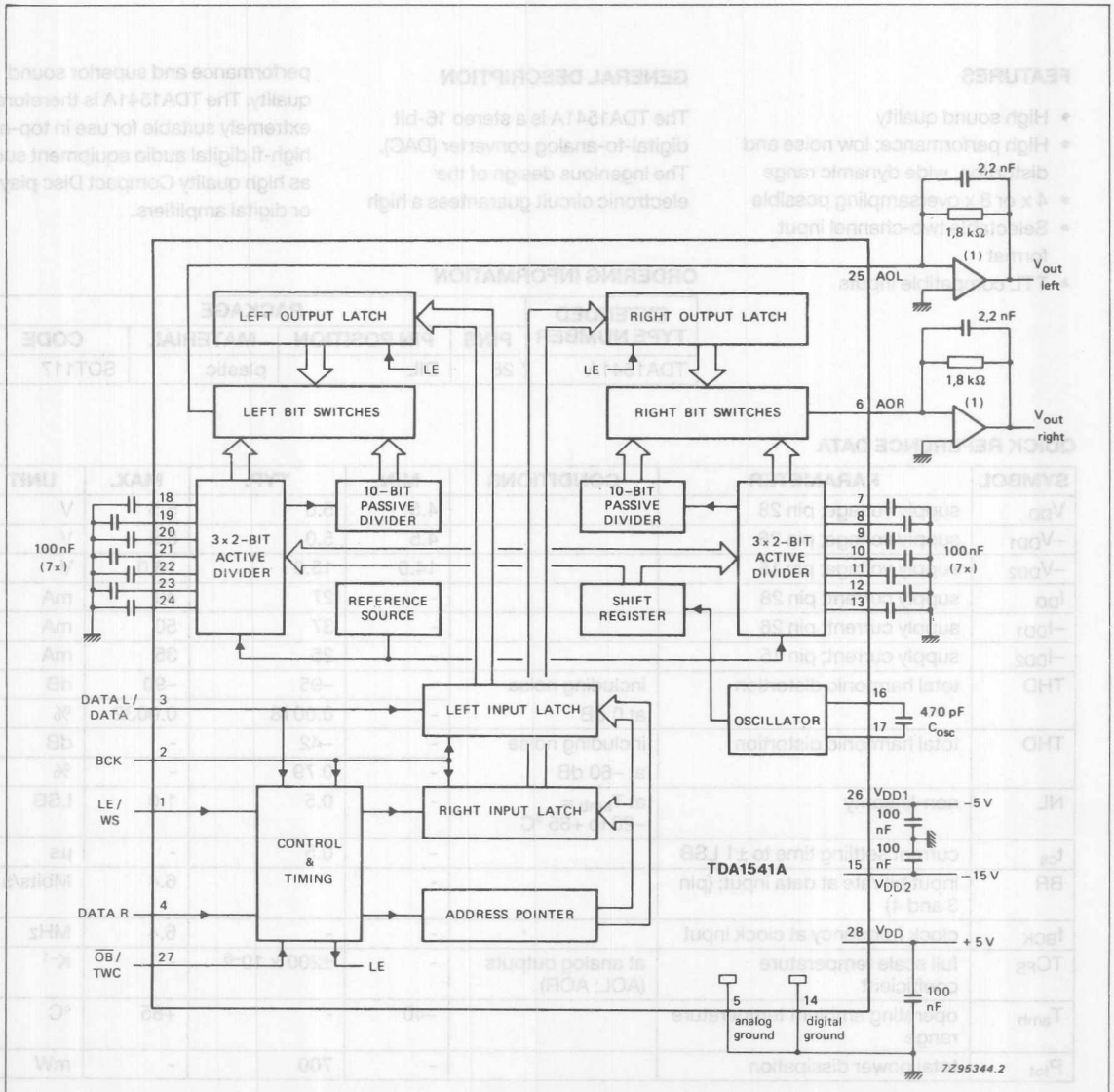
ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1541A	28	DIL	plastic	SOT117

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage; pin 28		4.5	5.0	5.5	V
$-V_{DD1}$	supply voltage; pin 26		4.5	5.0	5.5	V
$-V_{DD2}$	supply voltage; pin 15		14.0	15.0	16.0	V
I_{DD}	supply current; pin 28		-	27	40	mA
$-I_{DD1}$	supply current; pin 26		-	37	50	mA
$-I_{DD2}$	supply current; pin 15		-	25	35	mA
THD	total harmonic distortion	including noise	-	−95	−90	dB
		at 0 dB	-	0.0018	0.0032	%
THD	total harmonic distortion	including noise	-	−42	-	dB
		at −60 dB	-	0.79	-	%
NL	non-linearity	at T_{amb} = −20 to +85 °C	-	0.5	1.0	LSB
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input; (pin 3 and 4)		-	-	6.4	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	6.4	MHz
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 200 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−40	-	+85	°C
P_{tot}	total power dissipation		-	700	-	mW

Stereo high performance 16-bit DAC TDA1541A



(1) TDA1542
(2) 2 x NE5534 or equivalent

Fig.1 Block diagram.

Stereo high performance 16-bit DAC TDA1541A

PINNING

SYMBOL	PIN	DESCRIPTION
LE/WS*	1	latch enable input / word select input
BCK*	2	bit clock input
DATA L /DATA*	3	data left channel input / data input (selected format)
DATA R*	4	data right channel input
GND(A)	5	analog ground
AOR	6	right channel output
DECOU	7 to 13	decoupling
GND (D)	14	digital ground
V_{DD2}	15	–15 V supply voltage
COSC	16,17	oscillator
DECOU	18 to 24	decoupling
AOL	25	left channel output
V_{DD1}	26	–5 V supply voltage
$\overline{OB}$/TWC*	27	mode select input
V_{DD}	28	+5 V supply voltage

* See Table 1 data selection input.

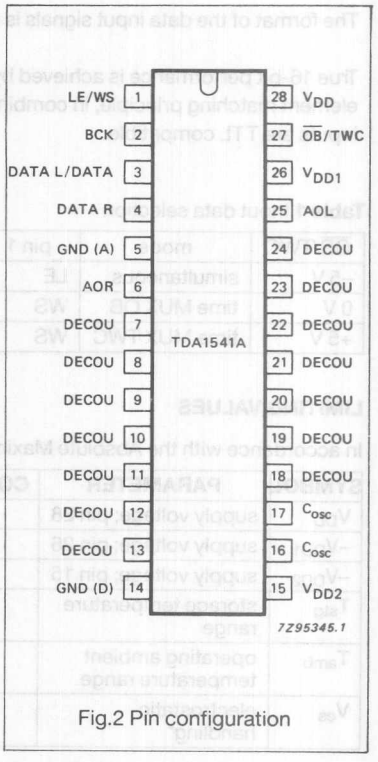


Fig.2 Pin configuration

FUNCTIONAL DESCRIPTION

The TDA1541A accepts input sample formats in time multiplexed mode or simultaneous mode up to 16-bit word length. The most significant bit (MSB) must always be first. This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit-rate and fast settling facilitates application in 8 x oversampling systems (44.1 kHz to 352.8 kHz or 48 kHz to 384 kHz) with the associated simple analog filtering function (low order, linear phase filter).

Input data selection (see also Table 1)

With the input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. The converted samples appear at the output, at the first positive going transition of the bit clock signal after a negative going transition of the word select signal.

With $\overline{OB}$/TWC connected to V_{DD} the mode is the same but the data format must be in the two's complement.

When input $\overline{OB}$/TWC input is connected to V_{DD1} the two channels of data (L/R) are input simultaneously via DATA L and DATA R, accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary. The converted samples appear at the output at the positive going transition of the latch enable signal.

The format of the data input signals is shown in fig.4 and 5.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current divider, based on emitter scaling. All digital inputs are TTL compatible.

Table 1 Input data selection

$\overline{OB}$/TWC	mode	pin 1	pin 2	pin 3	pin 4
–5 V	simultaneous	LE	BCK	DATA L	DATA R
0 V	time MUX OB	WS	BCK	DATA OB	not used
+5 V	time MUX TWC	WS	BCK	DATA TWC	not used

Where:

LE = latch enable
WS = word select, LOW = left channel; HIGH = right channel
BCK = bit clock
DATA L = data left
DATA R = data right
DATA OB = data offset binary
DATA TWC = data two's complement
MUX OB = mulitplexed offset binary
MUX TWC = multiplexed two's complement = I²S-format

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage; pin 28		0	7	V
$-V_{DD1}$	supply voltage; pin 26		0	7	V
$-V_{DD2}$	supply voltage; pin 15		0	17	V
T_{stg}	storage temperature range		–65	+150	°C
T_{amb}	operating ambient temperature range		–40	+85	°C
V_{es}	electrostatic handling*		–1000	+1000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	30	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; $-V_{DD1}$ = 5 V; $-V_{DD2}$ = 15 V; T_{amb} = +25 °C; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage; pin 28		4.5	5.0	5.5	V
$-V_{DD1}$	supply voltage; pin 26		4.5	5.0	5.5	V
$-V_{DD2}$	supply voltage; pin 15		14.0	15.0	16.0	V
$V_{GND(A)}$ $-V_{GND(D)}$	voltage difference between analog and digital ground		−0.3	0	+0.3	V
I_{DD}	supply current; pin 28		-	27	40	mA
$-I_{DD1}$	supply current; pin 26		-	37	50	mA
$-I_{DD2}$	supply current; pin 15		-	25	35	mA
Inputs						
$-I_{IL}$	input current pins (1, 2, 3 and 4) digital inputs LOW	V_I = 0.8 V	-	-	0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
$\lvert I_{\overline{OB/TWC}} \rvert$	Digital input currents (pin 27) +5 V		-	-	1	µA
$\lvert I_{\overline{OB/TWC}} \rvert$	0 V		-	-	20	µA
$\lvert I_{\overline{OB/TWC}} \rvert$	−5 V		-	-	40	µA
f_{BCK}	input frequency/bit rate clock input pin 2		-	-	6.4	MHz
BR	bit rate data input pin 3 and 4		-	-	6.4	Mbits/s
f_{WS}	word select input pin 2		-	-	200	kHz
f_{LE}	latch enable input 1		-	-	200	kHz
C_I	input capacitance of digital inputs		-	12	-	pF
Analog outputs (AOL; AOR; see note 1)						
Res	resolution		-	16	-	bits
I_{FS}	full scale current		3.4	4.0	4.6	mA
$\lvert I_{ZS} \rvert$	zero scale current		-	25	50	nA
T_{CFS}	full scale temperature coefficient	T_{amb} = −20 to +85 °C	-	±200 x 10^{-6}	-	K^{-1}
Analog outputs (V_{ref})						
E_L	integral linearity error	T_{amb} = 25 °C	-	0.5	1.0	LSB
E_L	integral linearity error	T_{amb} = −20 to +85°C	-	-	1.0	LSB
E_{dL}	differential linearity error	T_{amb} = 20°C, note 2	-	0.5	1.0	LSB
E_{dL}	differential linearity error	T_{amb} = −20 to +85°C	-	-	1.0	LSB
THD	total harmonic distortion	at 0 dB; note 3	−100	-	dB	
			-	0.0010	-	%
THD	total harmonic distortion	including noise at 0 dB;	-	−95	−90	dB
		note 3, Fig.3	-	0.0018	0.0032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−42	-	dB
		note 3, Fig.3	-	0.79	-	%

Stereo high performance 16-bit DAC TDA1541A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		90	98	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.1	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	-	0.2	µs
SSVR	supply voltage ripple rejection	V_{DD} = +5 V; note 4	-	–76	-	dB
SSVR	supply voltage ripple rejection	V_{DD1} = –5 V; note 4	-	–84	-	dB
SSVR	supply voltage ripple rejection	V_{DD2} = –15 V; note 4	-	–58	-	dB
S/N	signal-to-noise ratio	at bipolar zero	-	110	-	dB
S/N	signal-to-noise ratio	at full scale	98	104	-	dB
Timing (Fig.4 and 5)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		156	-	-	ns
t_{HB}	bit clock HIGH time		46	-	-	ns
t_{LB}	bit clock LOW time		46	-	-	ns
t_{FBRL}	bit clock fall time to latch enable rise time		0	-	-	ns
t_{RBFL}	bit clock rise time to latch enable fall time		0	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock		0	-	-	ns
$t_{HD;WS}$	word select hold time		0	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. To ensure no performance losses, permitted output voltage compliance is ±25 mV maximum.

2. Selections have been made with respect to the maximum differential linearity error (E_{dL}):

   TDA1541A/N2 bit 1-16 $E_{dL} < 1$ LSB

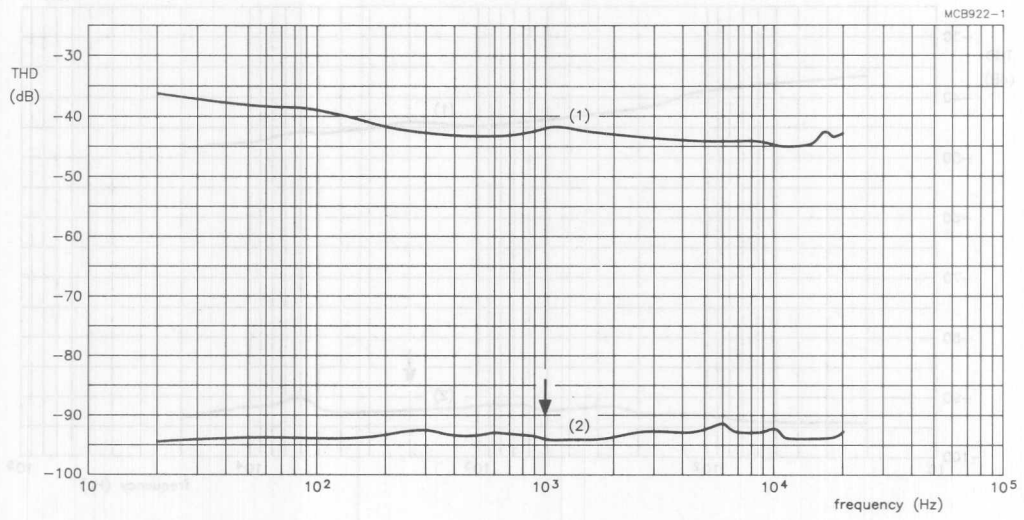
   TDA1541A/N2/R1 bit 1-16 $E_{dL} < 2$ LSB

   TDA1541A/N2/S1 bit 1-7 $E_{dL} < 0.5$ LSB
   bit 8-15 $E_{dL} < 1$ LSB
   bit 16 $E_{dL} < 0.75$ LSB

   The S1 version has been specially selected to achieve extremely good performance even for small signals.

3. Measured using a 1 kHz sinewave generated at a sampling rate of 176.4 kHz.

4. V_{ripple} = 100 mV and f_{ripple} = 100 Hz.

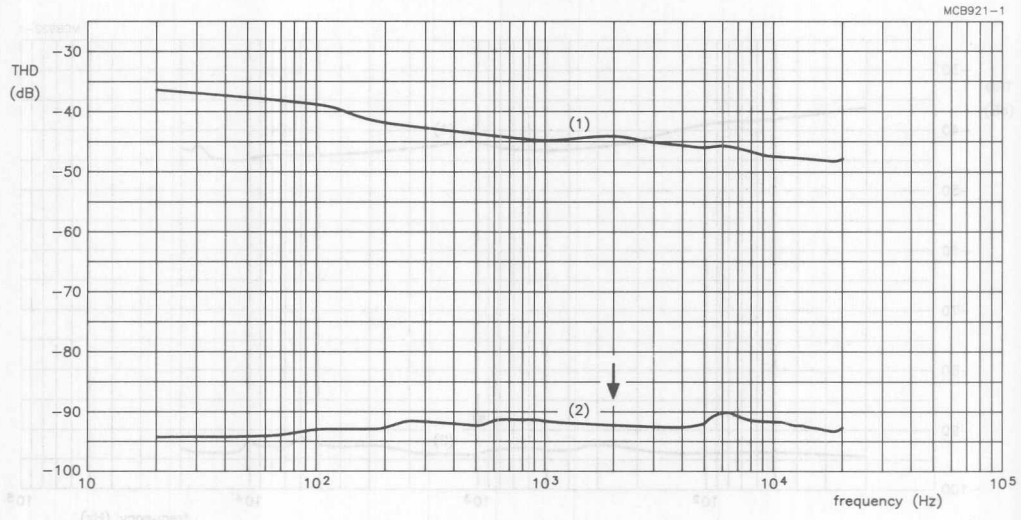


(1) Measured including all distortion plus noise at a signal level of −60 dB
(2) Measured including all distortion plus noise at a signal level of −0 dB

Fig.3a Distortion as a function of frequency (4FS)

Notes to Fig.3a

- The sample frequency 4FS: 176.4 kHz.
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.



(1) Measured including all distortion plus noise at a signal level of –60 dB
(2) Measured including all distortion plus noise at a signal level of –0 dB

Fig.3b Distortion as a function of frequency (8FS)

Notes to Fig.3b

- The sample frequency 8FS: 352.8 kHz.
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.

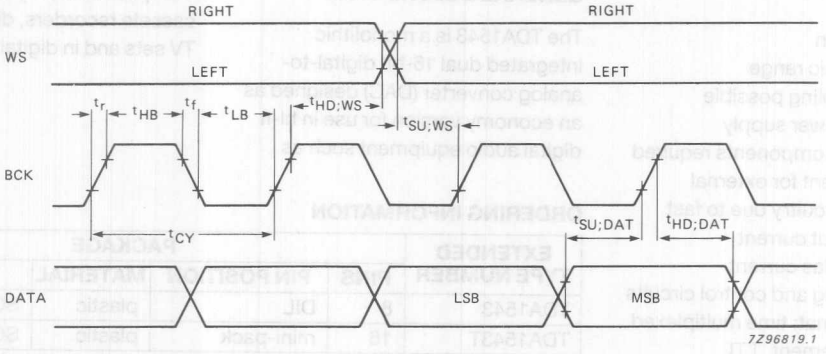


Fig.4 Format of input signals; time multiplexed (I^2S format).

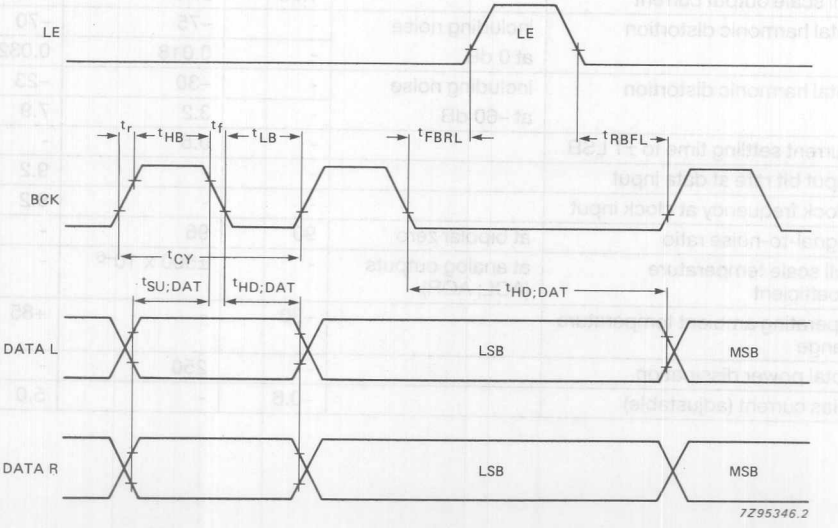


Fig.5 Format of input signals; simultaneous data.

Dual 16-bit DAC (economy version) (I^2S input format) TDA1543

FEATURES

- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- I^2S input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

The TDA1543 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders, digital sound in TV sets and in digital amplifiers.

ORDERING INFORMATION

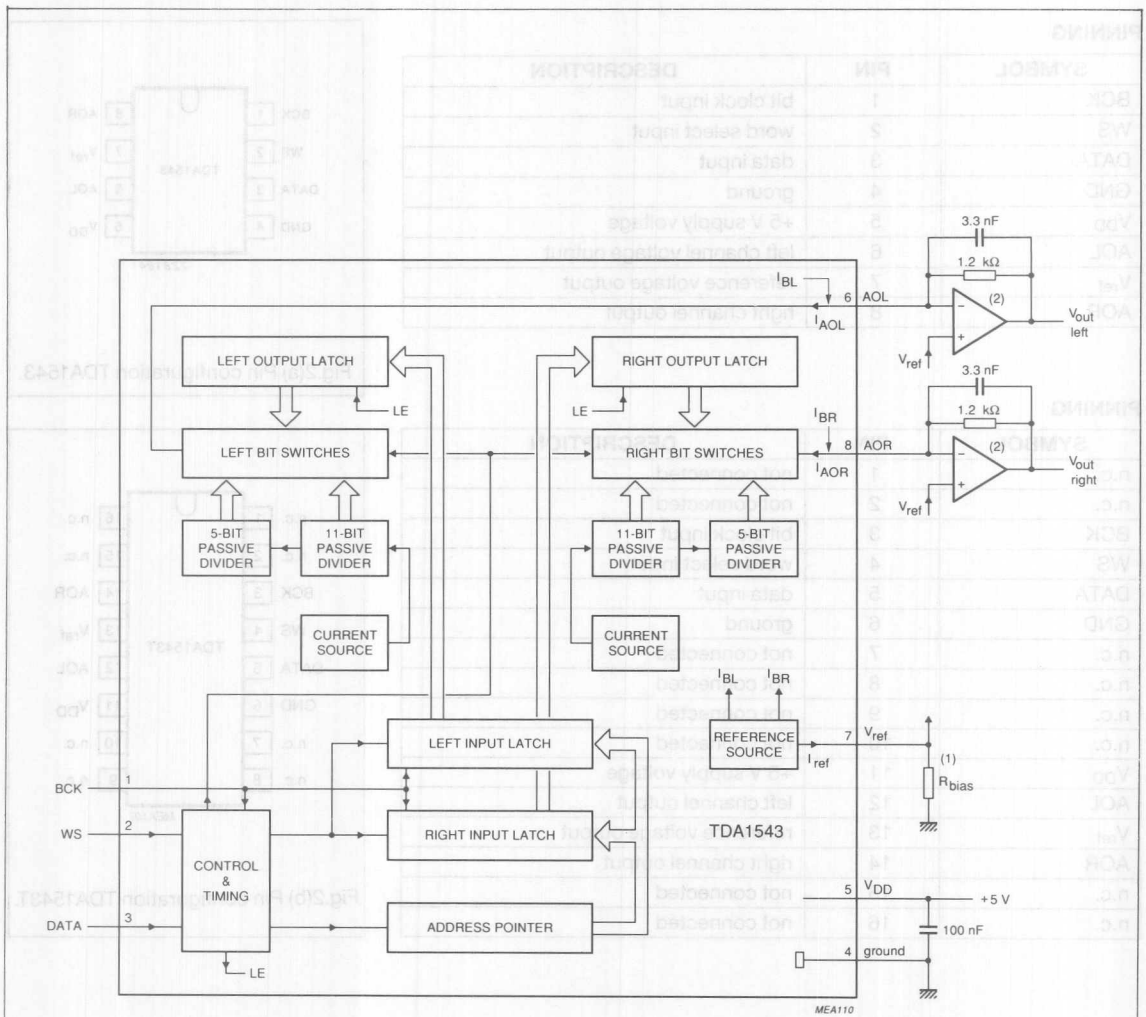
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1543	8	DIL	plastic	SOT97
TDA1543T	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		1.95	2.30	2.65	mA
THD	total harmonic distortion	including noise	-	–75	–70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	–30	–23	dB
		at –60 dB	-	3.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio	at bipolar zero	90	96	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		–30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		–0.6	-	5.0	mA

Dual 16-bit DAC (economy version) (I²S input format)

TDA1543



(1) Optional
(2) 2 x 1/2 NE5532

Fig.1 Block diagram.

Dual 16-bit DAC (economy version) (I²S input format)

TDA1543

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel voltage output
V_{ref}	7	reference voltage output
AOR	8	right channel output

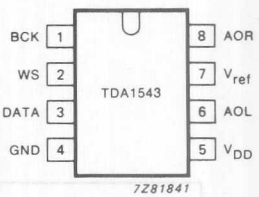


Fig.2(a) Pin configuration TDA1543.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

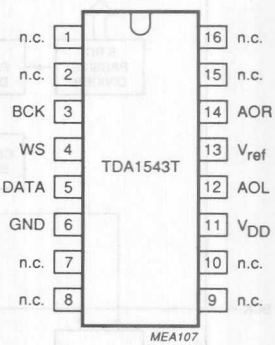
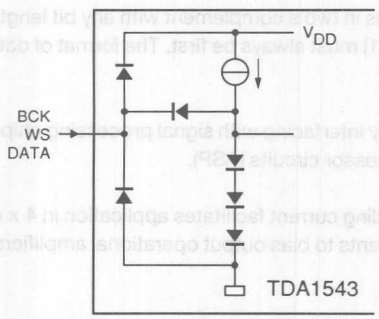


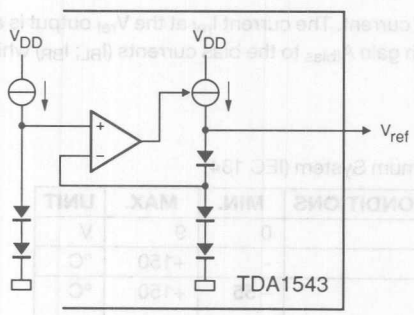
Fig.2(b) Pin configuration TDA1543T.

Dual 16-bit DAC (economy version) (I²S input format)

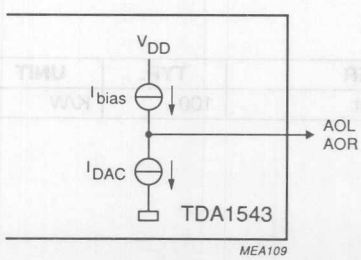
TDA1543



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

Dual 16-bit DAC (economy version) (I^2S input format) TDA1543

FUNCTIONAL DESCRIPTION

The TDA1543 accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

This flexible input data format (I^2S) allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits and audio signal processor circuits (ASP).

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the left input register and with a HIGH level on the WS input data is placed in the right input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		0	9	V
T_{XTAL}	crystal temperature		-	+150	°C
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−30	+85	°C
V_{es}	electrostatic handling*		−2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	100	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.0	5.0	8.0	V
I_{DD}	supply current	note 1	-	50	60	mA
RR	ripple rejection	note 2	-	50	-	dB
Digital inputs						
	input current pins (1, 2 and 3)					
I_{IL}	digital inputs LOW	V_I = 0.8 V	-	-	−0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
f_{BCK}	input frequency/bit rate clock input pin 1		-	-	9.2	MHz
BR	bit rate data input pin 3		-	-	9.2	Mbits/s
f_{WS}	word select input pin 2		-	-	192	kHz
Analog outputs (AOL; AOR)						
Res	resolution		-	-	16	bits
	output voltage compliance					
$V_{OC(AC)}$	AC		-	±25	-	mV
$V_{OC(DC)}$	DC		1.8	-	V_{DD}−1.2	V
I_{FS}	full scale current		1.95	2.30	2.65	mA
T_{CFS}	full scale temperature coefficient		-	±500 x 10^{-6}	-	K^{-1}
I_{offset}	offset current	I_{ref} = 0 mA	−0.1	0.0	0.1	mA
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA
AI_{bias}	bias current gain		1.9	2.0	2.1	
Analog outputs (V_{ref})						
V_{ref}	reference voltage output		2.10	2.20	2.30	V
I_{ref}	reference current output		−0.3	-	2.5	mA
THD	total harmonic distortion	including noise at 0 dB;		−75	−70	dB
		note 3, Fig.6		0.018	0.032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−30	−23	dB
		note 3, Fig.6	-	3.2	7.9	%
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		85	90	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	< 0.2	-	µs
S/N	signal-to-noise ratio	at bipolar zero; note 5	90	96	-	dB

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (Fig.4)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		108	-	-	ns
t_{HB}	bit clock HIGH time		22	-	-	ns
t_{LB}	bit clock LOW time		22	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock	note 6	2	-	-	ns
$t_{HD;WS}$	word select hold time	note 6	2	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point $t_{HD;DAT}$ = 0 ns, this value has been fixed on 2 ns due to tolerances.

Dual 16-bit DAC (economy version) (I²S input format)

TDA1543

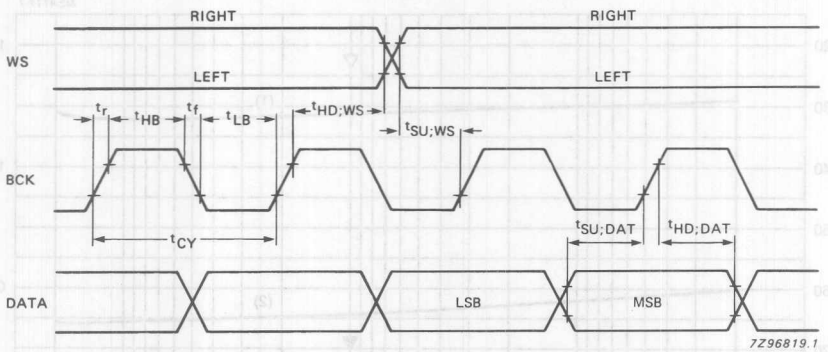


Fig.4 Format of input signals (I²S format).

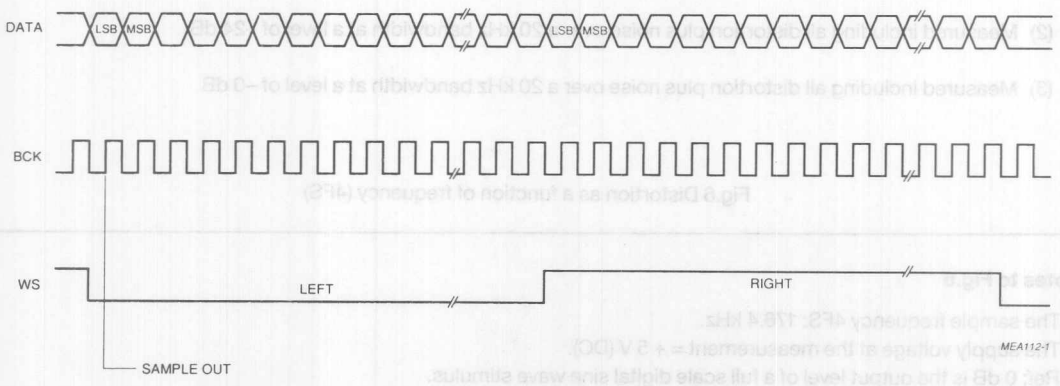
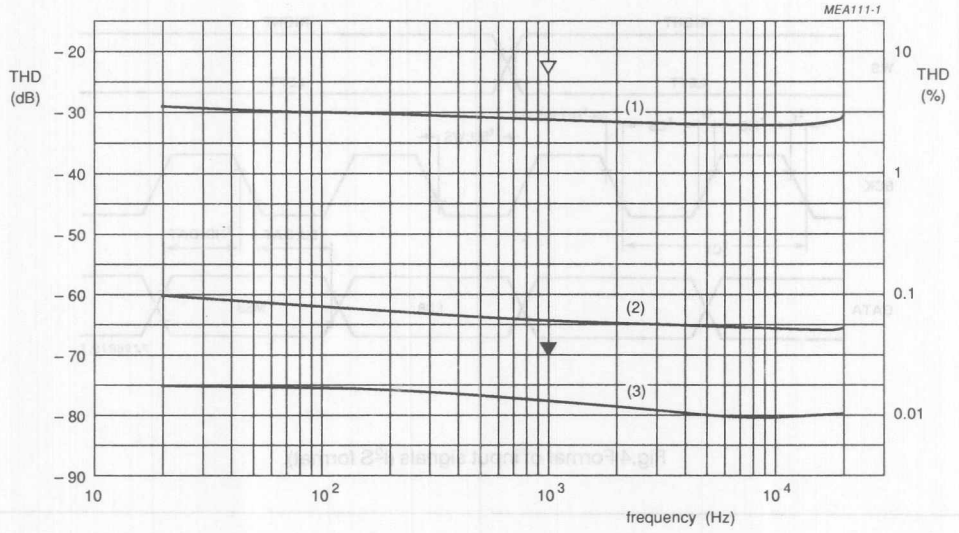


Fig.5 Format of input signals.

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543



(1) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –60 dB

(2) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –24 dB

(3) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –0 dB

Fig.6 Distortion as a function of frequency (4FS)

Notes to Fig.6

- The sample frequency 4FS: 176.4 kHz.
- The supply voltage at the measurement = + 5 V (DC).
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.
- The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied.
- The arrows indicate the specification limits for 0 dB and –60 dB level signals.

Dual 16-bit DAC (economy version) (Japanese input format) TDA1543A

GENERAL DESCRIPTION

The TDA1543A is a monolithic integrated dual 16-bit digital-to-analogue converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders, digital sound in television systems and digital amplifiers.

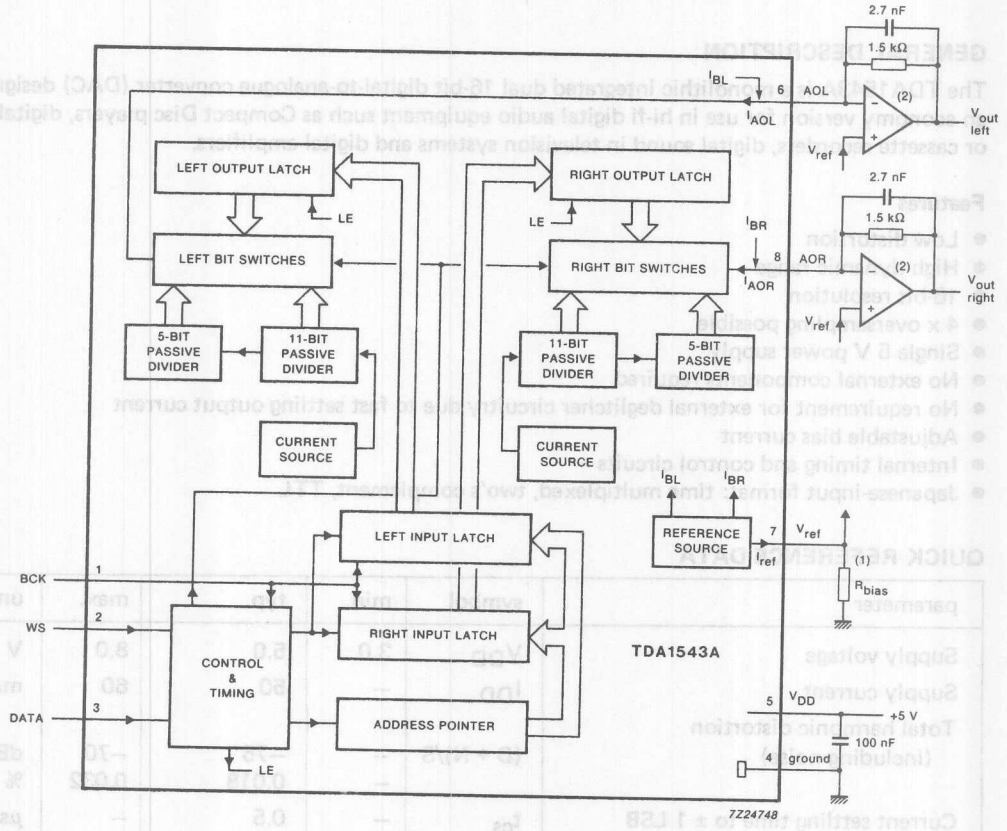
Features

- Low distortion
- High dynamic range
- 16-bit resolution
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- Japanese-input format: time multiplexed, two's complement, TTL

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	3.0	5.0	8.0	V
Supply current	I_{DD}	–	50	60	mA
Total harmonic distortion (including noise)	(D + N)/S	–	–75	–70	dB
		–	0.018	0.032	%
Current settling time to ± 1 LSB	t_{cs}	–	0.5	–	μs
Input bit rate at data input (pin 3)	BR	–	–	9.2	Mbits/s
Clock frequency at clock input (pin 1)	f_{BCK}	–	–	9.2	MHz
Signal-to-noise ratio at bipolar zero	S/N	90	95	–	dB
Full scale temperature coefficient at analogue outputs (AOL; AOR)	TC_{FS}	–	-500×10^{-6}	–	K^{-1}
Operating ambient temperature range	T_{amb}	–30	–	+ 85	°C
Total power dissipation	P_{tot}	–	250	–	mW
Bias current	I_{bias}	–0.6	–	5.0	mA

Dual 16-bit DAC (economy version) (Japanese input format) TDA1543A



(1) Optional.
(2) 2 x 1/2 NE5532.

Fig.1 Block diagram.

Dual 16-bit DAC (economy version) (Japanese input format) TDA1543A

PINNING

1	BCK	bit clock input
2	WS	word select input
3	DATA	data input
4	GND	ground
5	V_{DD}	+ 5 V supply voltage
6	AOL	left channel output
7	V_{ref}	reference voltage output
8	AOR	right channel output

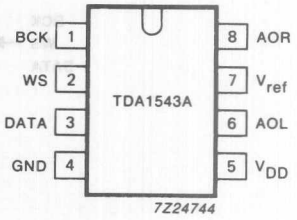
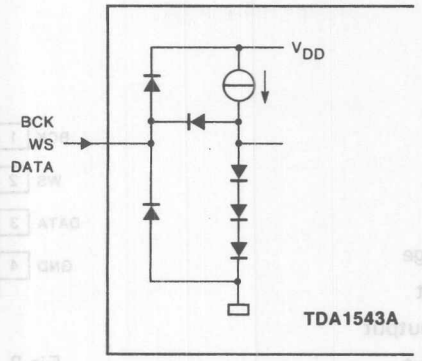
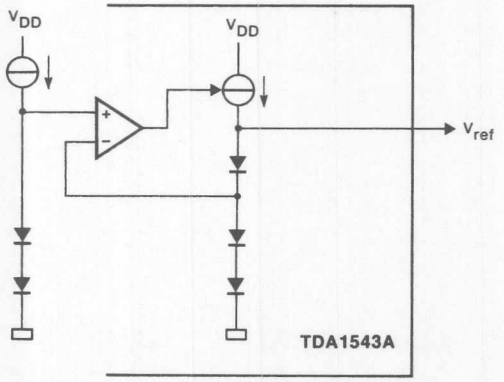


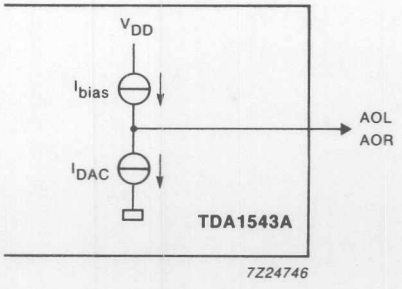
Fig.2 Pinning diagram.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

Dual 16-bit DAC (economy version) (Japanese input format) TDA1543A

FUNCTIONAL DESCRIPTION

The TDA1543A accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	0	9	V
Crystal temperature	T_{XTAL}	–	150	°C
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 85	°C
Electrostatic handling *	V_{es}	−1000	+ 1000	V

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	100	K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = + 25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	3.0	5.0	8.0	V
Supply current	note 1	I_{DD}	–	50	60	mA
Ripple rejection	note 2	RR	–	50	–	dB
Inputs						
Input current pins (1, 2 and 3)						
digital inputs LOW	V_I = 0.8 V	I_{IL}	–	–	–0.4	mA
digital inputs HIGH	V_I = 2.0 V	I_{IH}	–	–	20	μA
Input frequency/bit rate						
clock input pin 1		f_{BCK}	–	–	9.2	MHz
bit rate data input pin 3		BR	–	–	9.2	Mbits/s
word select input pin 2		f_{WS}	–	–	192	kHz
Input capacitance of digital inputs		C_I	–	*	–	pF
Analogue outputs (AOL; AOR)						
Resolution		Res	–	–	16	bits
Output voltage compliance						
AC		$V_{OC(AC)}$	–	± 25	–	mV
DC		$V_{OC(DC)}$	1.8	–	V_{DD}–1.2	V
Full scale current		I_{FS}	1.95	2.3	2.65	mA
Full scale temperature coefficient		TC_{FS}	–	-500×10^{-6}	–	K^{-1}
Offset current	I_{ref} = 0 mA; $V_{AO} = V_{ref}$	I_{offset}	–0.1	0	0.1	mA
Bias current (adjustable)		I_{bias}	–0.6	–	5.0	mA
Bias current gain		AI_{bias}	1.9	2.0	2.1	

Dual 16-bit DAC (economy version) (Japanese input format) TDA1543A

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output (V_{ref})						
Reference voltage output		V_{ref}	2.1	2.2	2.3	V
Reference current output		I_{ref}	−0.3	−	2.5	mA
Total harmonic distortion (including noise)	note 3	(D + N)/S	−	−75	−70	dB
			−	0.018	0.032	%
Settling time ± 1 LSB		t_{cs}	−	0.5	−	μs
Channel separation		α	84	90	−	dB
Unbalance between outputs	note 3	$\lvert d_{IO} \rvert$	−	< 0.2	0.3	dB
Time delay between outputs		t_d	−	< 0.2	−	μs
Signal-to-noise ratio at bipolar zero	note 4	S/N	90	95	−	dB
Timing	Fig.4					
Rise time		t_r	−	−	32	ns
Fall time		t_f	−	−	32	ns
Bit clock cycle time		t_{CY}	108	−	−	ns
Bit clock HIGH time		t_{HB}	22	−	−	ns
Bit clock LOW time		t_{LB}	22	−	−	ns
Data set-up time		$t_{SU;DAT}$	32	−	−	ns
Data hold time to bit clock		$t_{HD;DAT}$	2	−	−	ns
Word select hold time		$t_{HD;WS}$	2	−	−	ns
Word select set-up time		$t_{SU;WS}$	32	−	−	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. With 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
4. At code 0000H.

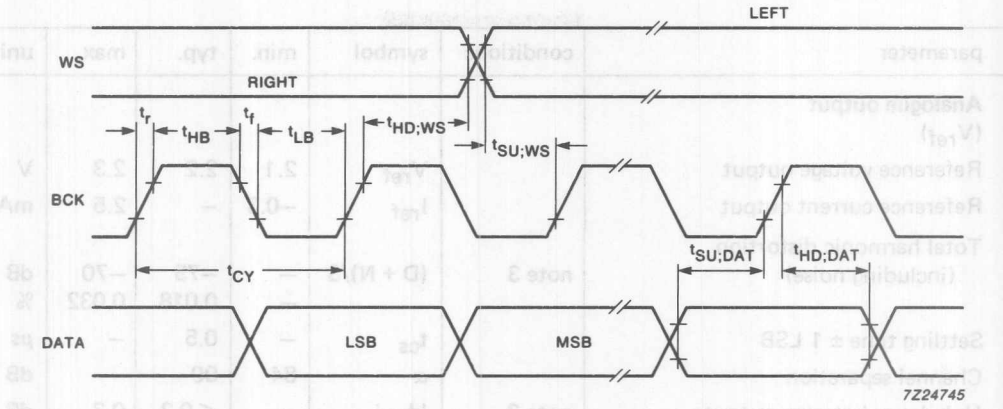


Fig.4 Format of input signals (Japanse format).

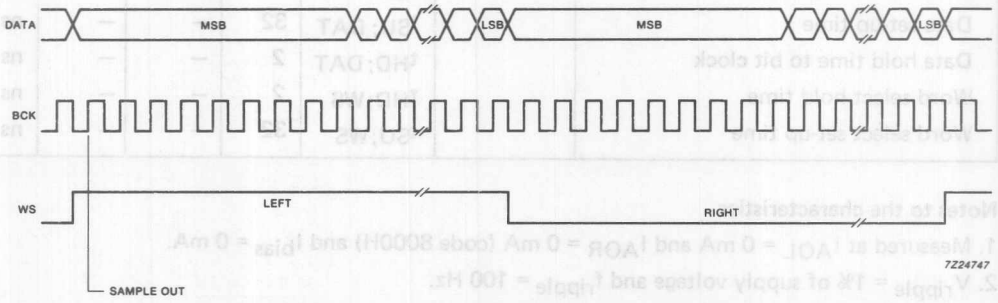


Fig.5 Format of input signals.

Stereo continuous calibration DAC

TDA1545

GENERAL DESCRIPTION

The TDA1545 is the first device of a new generation of the digital-to-analog convertors which embodies the innovative technique of continuous calibration. The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle having an accuracy insensitive to ageing, temperature, matching and process variations. The TDA1545 is fabricated in a 1.0 µm CMOS process and features an extremely low power dissipation, small package size and easy application. Furthermore, the accuracy of the high coarse current combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensures high quality audio reproduction. Therefore, the continuous calibration digital-to-analog convertor is eminently suitable for use in (portable) digital audio equipment.

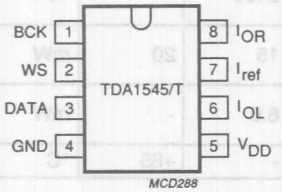


Fig.1 Pinning diagram.

FEATURES

- Space saving package (SO8 or DIL8)
- Low power consumption
- Low total harmonic distortion
- Wide dynamic range (16-bit resolution)
- Continuous calibration concept
- Easy application: single 3 to 5.5 V rail power supply and output- and bias current are proportional to the supply voltage
- Fast settling time permits 2 x, 4 x and 8 x oversampling (serial input) or double speed operation at 4 x oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range of –40 °C to 85 °C
- Internal timing and control circuits
- Compatible with most of the Japanese input formats: time multiplexed, two's complement, TTL
- No zero crossing distortion

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1545	8	DIL	plastic	SOT97
TDA1545T	8	mini-pack	plastic	SO8; SOT96A

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	positive supply voltage
I_{OL}	6	left channel output
V_{ref}	7	reference voltage output
I_{OR}	8	right channel output

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient		
	DIL8	100	K/W
	SO8	210	K/W

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3	5	5.5	V
I_{DD}	supply current	V_{DD} = 5 V, at code 0000H	-	3.0	4.0	mA
I_{FS}	full scale output current	V_{DD} = 5 V	0.9	1.0	1.1	mA
I_{FS}	full scale output current	V_{DD} = 3 V	-	0.6	-	mA
THD	total harmonic distortion	including noise at 0 dB	-	–85	–78	dB
			-	0.005	0.01	%
THD	total harmonic distortion	including noise at –60 dB	-	–30	–24	dB
			-	3	6	%
THD	total harmonic distortion	including noise at –60 dB, A-weigthing	-	–33	-	dB
			-	2	-	%
		R3 = R4 = 11 kΩ see Fig.2; I_{FS} = 2 mA	-	1	-	%
S/N	signal-to-noise ratio at bipolar zero	A-weighting, at code 0000H	86	92	-	dB
S/N	signal-to-noise ratio at bipolar zero	R3 = R4 = 11 kΩ see Fig.1; I_{FS} = 2 mA	-	95	-	dB
t_{cs}	current settling time to ±1 LSB		-	0.2	-	µs
BR	input bit rate at data input		-	-	18.4	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (I_{OL}; I_{OR})		-	±400	-	10^{-6}
P_{tot}	total power dissipation	V_{DD} = 5 V, at code 0000H	-	15	20	mW
P_{tot}	total power dissipation	V_{DD} = 3 V, at code 0000H	-	6.0	-	mW
T_{amb}	operating ambient temperature range		–40	-	+85	°C

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		-	-	6	V
T_{stg}	storage temperature range		–55	-	+150	°C
T_{XTAL}	maximum crystal temperature		-	-	+150	°C
T_{amb}	operating ambient temperature range		–40	-	+85	°C
V_{es}	electrostatic handling	see note 1	–2000	-	+2000	V

Note to the limiting values

1 Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

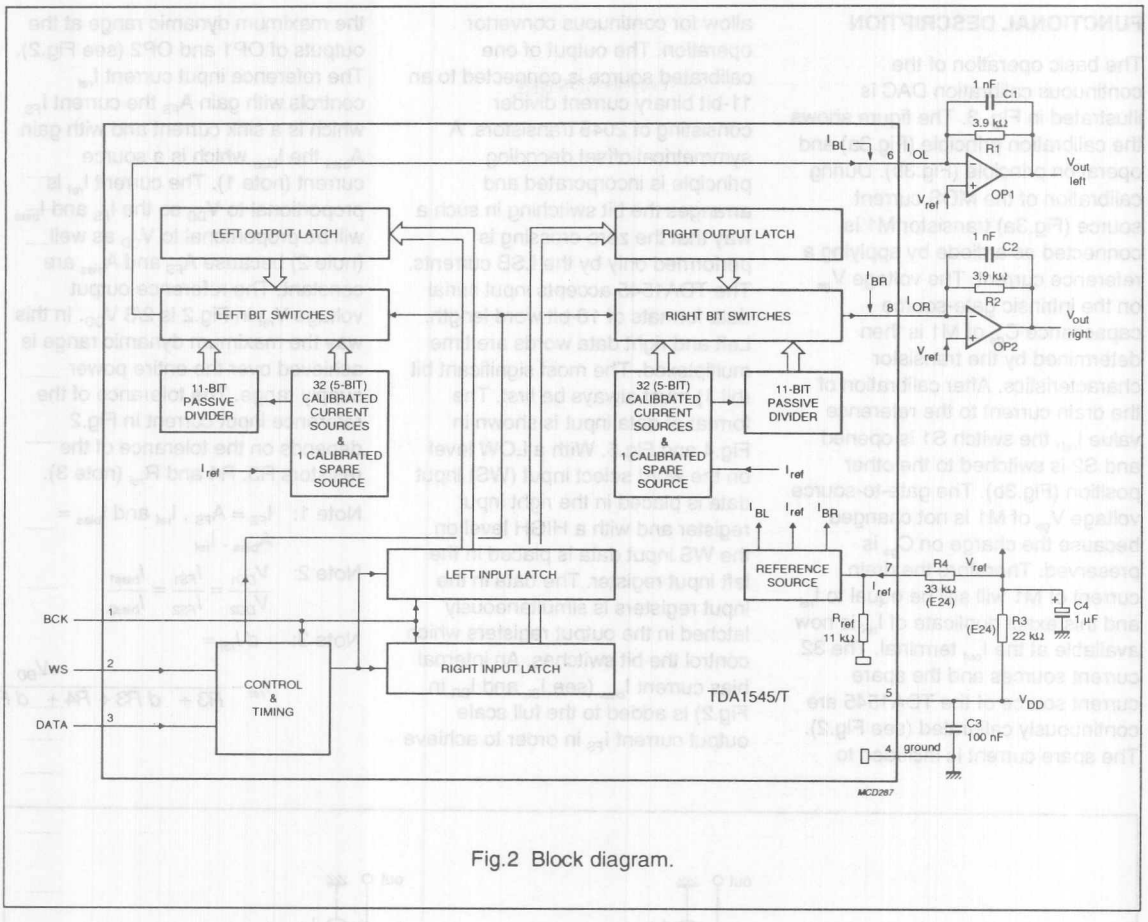


Fig.2 Block diagram.

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig. 3. The figure shows the calibration principle (Fig.3a) and operation principle (Fig.3b). During calibration of the MOS current source (Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After calibration of the drain current to the reference value I_{ref}, the switch S1 is opened and S2 is switched to the other position (Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore the drain current of M1 will still be equal to I_{ref} and this exact duplicate of I_{ref} is now available at the I_{out} terminal. The 32 current sources and the spare current source of the TDA1545 are continuously calibrated (see Fig.2). The spare current is included to allow for continuous convertor operation. The output of one calibrated source is connected to an 11-bit binary current divider consisting of 2048 transistors. A symmetrical offset decoding principle is incorporated and arranges the bit switching in such a way that the zero-crossing is performed only by the LSB currents. The TDA1545 accepts input serial data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5. With a LOW level on the word select input (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches. An internal bias current I_{bias} (see I_{BL} and I_{BR} in Fig.2) is added to the full scale output current I_{FS} in order to achieve the maximum dynamic range at the outputs of OP1 and OP2 (see Fig.2). The reference input current I_{ref} controls with gain A_{FS} the current I_{FS} which is a sink current and with gain A_{bias} the I_{bias} which is a source current (note 1). The current I_{ref} is proportional to V_{DD} so the I_{FS} and I_{bias} will be proportional to V_{DD} as well (note 2) because A_{FS} and A_{bias} are constant. The reference output voltage V_{ref} in Fig.2 is 2/3 V_{DD}. In this way the maximum dynamic range is achieved over the entire power supply range. The tolerance of the reference input current in Fig.2 depends on the tolerance of the resistors R3, R4 and R_{ref} (note 3).

Note 1: $I_{FS} = A_{FS} \cdot I_{ref}$ and $I_{bias} = A_{bias} \cdot I_{ref}$

Note 2: $$\frac{V_{DD1}}{V_{DD2}} = \frac{I_{FS1}}{I_{FS2}} = \frac{I_{bias1}}{I_{bias2}}$$

Note 3: $$d\,I_{ref} = I_{ref} - \frac{V_{DD}}{R3 + d\,R3 + R4 + d\,R4 + R}$$

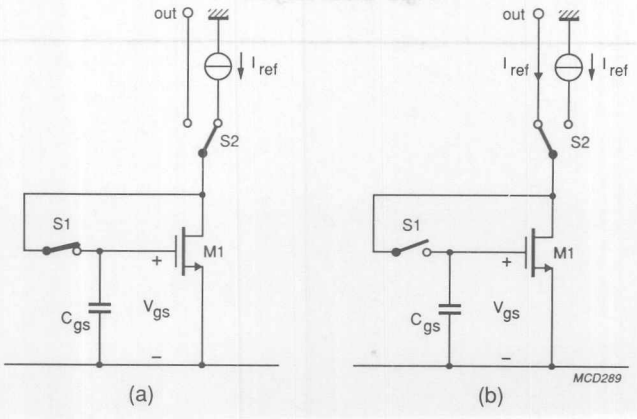


Fig.3 Calibration principle: (a) calibration, (b) operation.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range		3.0	5.0	5.5	V
I_{DD}	supply current	note 1	-	3.0	4.0	mA
RR	ripple rejection	note 2	-	30	-	dB
Digital inputs (WS; BCK; DATA)						
$\lvert I_{IL} \rvert$	input leakage current LOW	V_I = 0.8 V	-	-	10	µA
$\lvert I_{IH} \rvert$	input leakage current HIGH	V_I = 2.4 V	-	-	10	µA
f_{BCK}	clock input pin 1		-	-	18.4	MHz
BR	bit rate data input pin 3		-	-	18.4	Mbits/s
f_{WS}	word select input pin 2		-	-	384	kHz
Timing (Fig.4)						
t_r	rise time		-	-	12	ns
t_f	fall time		-	-	12	ns
t_{CY}	bit clock cycle time		54	-	-	ns
t_{HB}	bit clock HIGH time		15	-	-	ns
t_{LB}	bit clock LOW time		15	-	-	ns
$t_{SU;DAT}$	data set-up time		12	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock		2	-	-	ns
$t_{HD;WS}$	word select hold time		2	-	-	ns
$t_{SU;WS}$	word select set-up time		12	-	-	ns
Analog input (I_{ref})						
R_{ref}	reference resistor (see Fig.2)		7.4	11.0	14.6	kΩ
Analog outputs (I_{OL}; I_{OR})						
Res	resolution		-	-	16	bits
V_{DCC}	DC output voltage compliance		2.0	-	V_{DD}−1	V
I_{FS}	full scale current		0.9	1.0	1.1	mA
T_{CFS}	full scale temperature coefficient		-	±400	-	10^{-6}
I_{bias}	bias current (adjustable)		643	714	785	µA
A_{FS}	reference input current to full scale output current gain		12.8	13.2	13.6	
A_{bias}	reference input current to bias current gain		9.14	9.42	9.7	
THD	total harmonic distortion	including noise at 0 dB; note 3, Fig.6	- -	−85 0.005	−78 0.01	dB %
THD	total harmonic distortion	including noise at −60 dB; note 3, Fig.6	- -	−30 3	−24 6	dB %

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	including noise at –60 dB, A-weigthing	-	–33	-	dB
			-	2	-	%
		R3 = R4 = 11 kΩ see Fig.2; I_{FS} = 2 mA	-	1	-	%
THD	total harmonic distortion	including noise at 0 dB; note 4	-	–81	–70	dB
			-	0.009	0.03	%
t_{cs}	settling time ±1 LSB		-	0.2	-	µs
α	channel separation		86	95	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 3	-	0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	±0.2	-	µs
S/N	signal-to-noise ratio (A-weighting)	at bipolar zero; note 1	86	92	-	dB
S/N	signal-to-noise ratio (A-weighting)	at bipolar zero; note 5	-	95	-	dB

Notes to the characteristics

1 At code 0000H

2 V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.

3 Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.

4 Measured with 1 kHz sinewave over a 20 Hz to 20 kHz bandwidth generated at a sampling rate of 192 kHz.

5 R3 = R4 = 11 kΩ; see Fig.2; I_{FS} = 2 mA

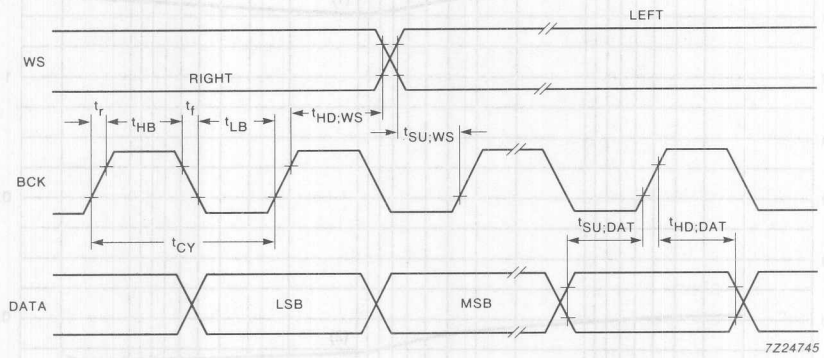


Fig.4 Format of input signals (Japanese format).

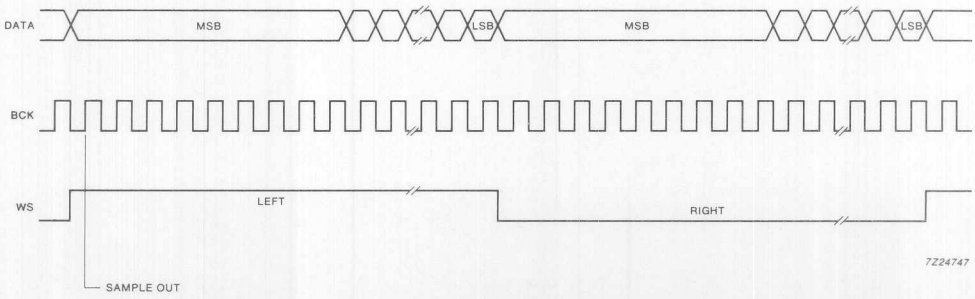
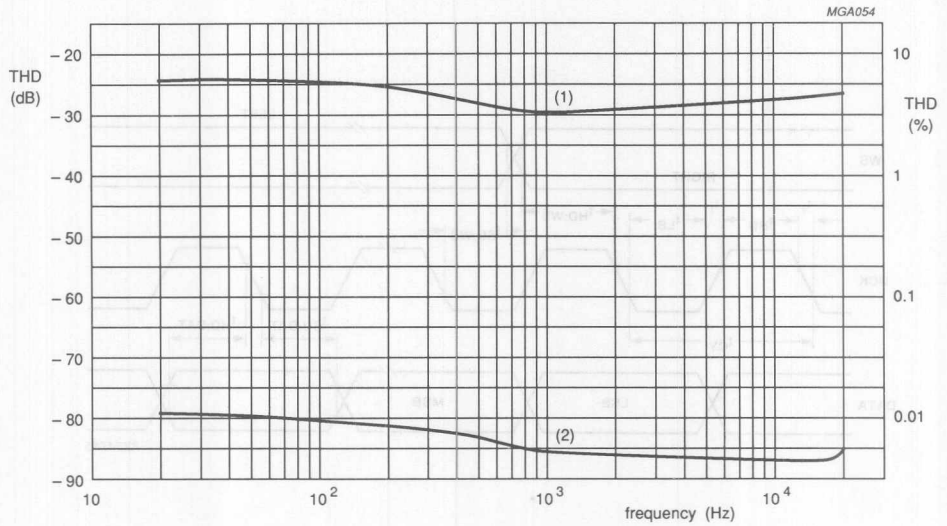


Fig.5 Format of input signals.



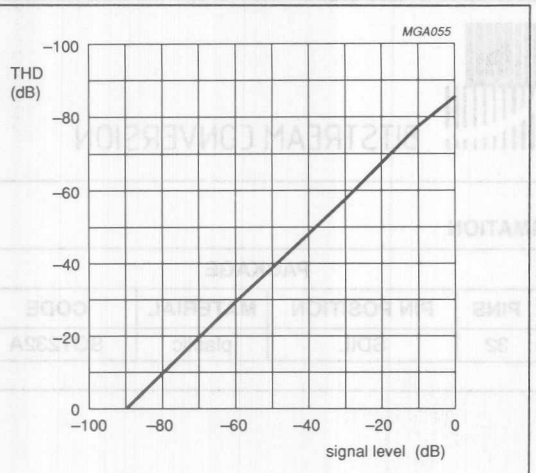
(1) Measured including all distortion plus noise at a level of –60 dB

(2) Measured including all distortion plus noise at a level of –0 dB

The sample frequency 4FS: 176.4 kHz

The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

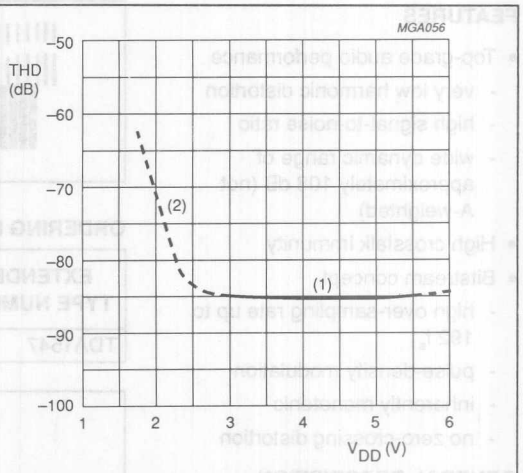
Fig.6 Distortion as a function of frequency (4FS).



The sample frequency 4FS: 176.4 kHz

The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

Fig.7 Distortion as a function of signal level (4FS).



(1) Measured within the specified operating supply voltage range

(2) Measured outside the specified operating supply voltage range

The sample frequency 4FS: 176.4 kHz

The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

Fig.8 Distortion as a function of supply voltage V_{DD} (4FS).

Dual top-performance bitstream DAC

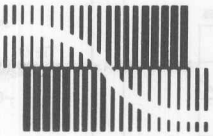
TDA1547

FEATURES

- Top-grade audio performance
  - very low harmonic distortion
  - high signal-to-noise ratio
  - wide dynamic range of approximately 108 dB (not A-weighted)
- High crosstalk immunity
- Bitstream concept
  - high over-sampling rate up to 192 f_s
  - pulse-density modulation
  - inherently monotonic
  - no zero-crossing distortion

GENERAL DESCRIPTION

The TDA1547 is a dedicated one-bit digital-to-analog converter to facilitate a high fidelity sound reproduction of digital audio. The TDA1547 is extremely suitable for use in high quality audio systems such as Compact Disc and DAT players, or in digital amplifiers and digital signal processing systems. The TDA1547 is used in combination with the SAA7350 bitstream circuit, which includes the third-order noise shaper. The excellent performance of the SAA7350 and TDA1547 bitstream conversion system is obtained by separating the noise shaping circuit and the one-bit conversion circuit over two IC's, thereby reducing the crosstalk between the digital and analog parts. The TDA1547 one-bit converter is processed in BIMOS. In the digital logic and drivers bipolar transistors are used to optimize speed and to reduce digital noise generation. In the analog part the bipolar transistors are used to obtain high performance of the operational amplifiers. Special layout precautions have been taken to achieve a high crosstalk immunity. The layout of the TDA1547 has fully separated left and right channels and supply voltage lines between the digital and analog sections.



ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1547	32	SDIL	plastic	SOT232A

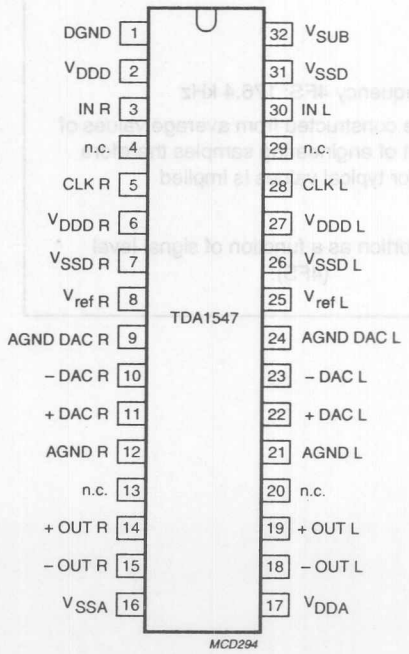


Fig.1 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DGND	1	0 V digital supply
V_{DDD}	2	5 V digital supply for both channels
IN R	3	serial one-bit data input for the right channel
n.c.	4	pin not connected; should preferably be connected to digital ground
CLK R	5	clock input for the right channel
$V_{DDD\ R}$	6	5 V digital supply for the right channel; this voltage determines the internal logic HIGH level in the right channel
$V_{SSD\ R}$	7	–3.5 V digital supply for the right channel; this voltage determines the internal logic LOW level in the right channel
$V_{ref\ R}$	8	–4 V reference voltage for the right channel switched capacitor DAC
AGND DAC R	9	0 V reference voltage for the right channel switched capacitor DAC; this pin should be connected to analog ground
–DAC R	10	output from the right negative switched capacitor DAC; feedback connection for the right negative operational amplifier
+DAC R	11	output from the right positive switched capacitor DAC; feedback connection for the right positive operational amplifier
AGND R	12	0 V reference voltage for both right channel operational amplifiers
n.c.	13	pin not connected; should preferably be connected to analog ground
+OUT R	14	+ output of the switched capacitor operational amplifier
–OUT R	15	– output of the switched capacitor operational amplifier
V_{SSA}	16	–5 V analog supply
V_{DDA}	17	5 V analog supply
–OUT L	18	– output of the switched capacitor operational amplifier
+OUT L	19	+ output of the switched capacitor operational amplifier
n.c.	20	pin not connected; should preferably be connected to analog ground
AGND L	21	0 V reference voltage for both left channel operational amplifiers
+DAC L	22	output from the left positive switched capacitor DAC; feedback connection for the left positive operational amplifier
–DAC L	23	output from the left negative switched capacitor DAC; feedback connection for the left negative operational amplifier
AGND DAC L	24	0 V reference voltage for the left channel switched capacitor DAC; this pin should be connected to analog ground
$V_{ref\ L}$	25	–4 V reference voltage for the left channel switched capacitor DAC
$V_{SSD\ L}$	26	–3.5 V digital supply for the left channel; this voltage determines the internal logic LOW level in the left channel
$V_{DDD\ L}$	27	5 V digital supply for the left channel; this voltage determines the internal logic HIGH level in the left channel

SYMBOL	PIN	DESCRIPTION
CLK L	28	clock input for the left channel
n.c.	29	pin not connected; should preferably be connected to digital ground
IN L	30	serial one-bit data input for the left channel
V_{SSD}	31	–5 V digital supply for both channels
V_{SUB}	32	–5 V substrate voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply voltages						
$V_{DDD\ L.\ R}$	positive digital supply voltage for one channel; pins 27 and 6		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage for both channels; pin 2		4.5	5.0	5.5	V
$V_{SSD\ L.\ R}$	negative digital supply voltage for one channel; pins 26 and 7		–4.0	–3.5	–3.0	V
V_{SSD}	negative digital supply voltage for both channels; pin 31		–5.5	–5.0	–4.5	V
V_{DDA}	positive analog supply voltage; pin 17		4.5	5.0	6	V
V_{SSA}	negative analog supply voltage ; pin 16		–6.0	–5.0	–4.5	V
Supply current						
$I_{DDD\ L.\ R}$	positive digital supply current for one channel; pins 27 and 6		-	0.1	-	mA
I_{DDD}	digital supply current for both channels; pin 2		-	29.0	-	mA
$I_{SSD\ L.\ R}$	negative digital supply current for one channel; pins 26 and 7		-	–0.1	-	mA
I_{SSD}	negative supply current for both channels; pin 31		-	–28.0	-	mA
I_{DDA}	positive analog supply current; pin 17		-	51.0	-	mA
I_{SSA}	negative analog supply current; pin 16		-	–51.0	-	mA
P_{tot}	total power dissipation		-	800	-	mW
$V_{OUT(RMS)}$	output voltage (RMS value)	f_{CLK} = 8.46 MHz; notes 1 and 2	0.85	1.0	1.15	V

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply current						
(THD + N)/S	THD + Noise; 0 dB	1 kHz; notes 2 and 3	-	–101	–96	dB
			-	0.0009	0.0016	%
(THD + N)/S	THD + Noise; 0 dB	f = 20 Hz to 20 kHz; notes 2 and 4	-	–101	-	dB
			-	0.0009	-	%
(THD + N)/S	THD + Noise; –20 dB	f = 1 kHz; notes 2 and 3	-	–88	–84	dB
(THD + N)/S	THD + Noise; –60 dB	f = 1 kHz; notes 2 and 3	-	–48	–44	dB
S/N	signal-to-noise ratio	pattern 0101..; notes 2 and 5	109	111	-	dB
S/N	signal-to-noise ratio; "A"-weighting	pattern 0101..; notes 2 and 5	-	113	-	dB
f_{CLK}	maximum clock frequency		-	-	10	MHz
α	channel separation	f = 1 kHz	101	115	-	dB
T_{amb}	operating ambient temperature		–20	-	70	°C

Notes to the quick reference data

1. Output level tracks linearly with both the clock frequency and the reference voltage ($V_{ref\ L}$ or $V_{ref\ R}$)
2. Device measured in differential mode with external components as shown in Fig.5.
3. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 1 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
4. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 20 Hz to 20 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
5. The specified signal-to-noise ratio includes noise introduced by the application components as shown in Fig.5.

FUNCTIONAL DESCRIPTION

Both channels are completely separated to reach the desired high crosstalk suppression level.
Each channel consists of the following functional parts:

- One-bit input, which latches the incoming data to the system clock.
- Switch driver circuit, which generates the non-overlapping clock- and data-signals that control the DAC switched capacitor networks.
- Switched capacitor network, this forms the actual DAC function, it supplies charge packets to the low-pass filter, under control of the incoming one-bit code.
- Two high performance operational amplifiers, that perform the charge packet to voltage conversion and deliver a differential output signal. The first pole of the low-pass filter is built around them.

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	60	K/W

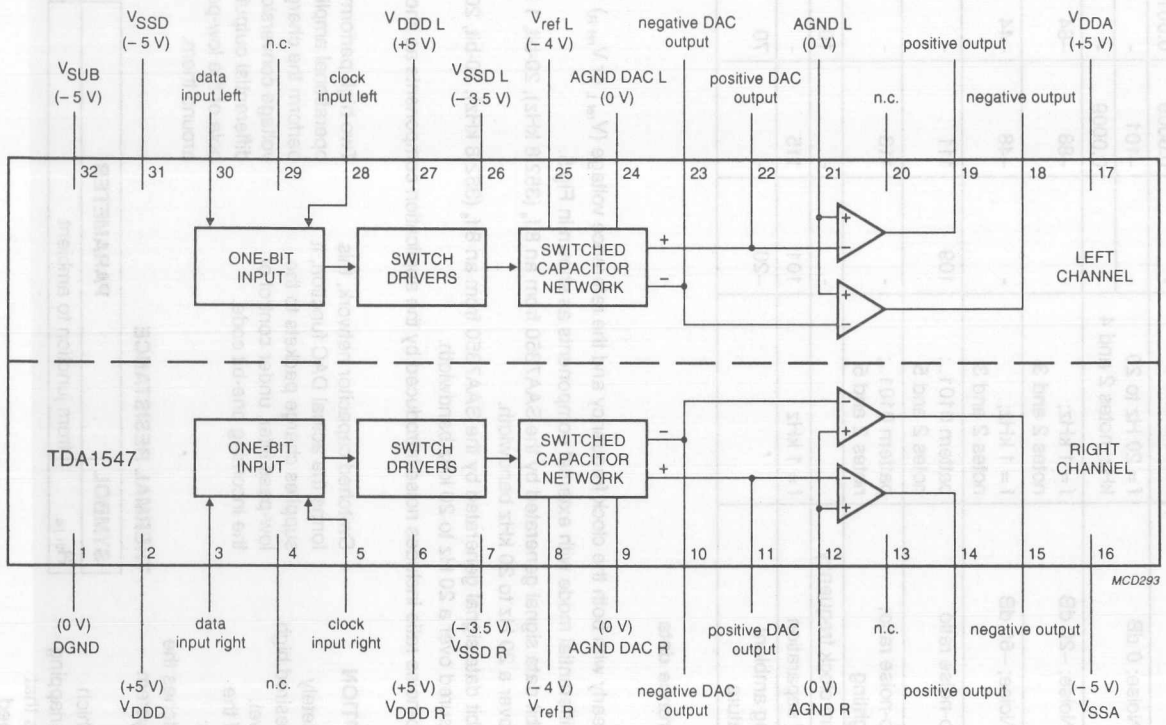


Fig.2 Block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX.	UNIT
V_{SUB}	negative substrate voltage; pin 32	note 1	–7.0	-	V
$V_{DDD\ L,\ R}$	positive digital supply voltage; pins 27 and 6		-	5.5	V
V_{DDD}	positive digital supply voltage; pin 2		-	5.5	V
$V_{SSD\ L,\ R}$	negative digital supply voltage; pins 26 and 7		–4.0	-	V
V_{SSD}	negative digital supply voltage; pin 31		–5.5	-	V
V_{DDA}	positive analog supply voltage; pin 17		-	6.0	V
V_{SSA}	negative analog supply voltage; pin 16		–6.0	-	V
$V_{DDD\ L,\ R} - V_{SSD\ L,\ R}$	supply voltage difference between pins 27, 6 and pins 26, 7		-	9.0	V
P_{tot}	total power dissipation	T_{amb} = 70 °C	-	1300	mW
$V_{ref\ L,\ R}$	input reference voltage; pins 25 and 8		–6.0		V
$V_{CLK\ L,\ R}$	input voltage clock; pins 28 and 5		–0.5	V_{DDD}+0.5	V
$V_{I\ L}$	input voltage channel; pin 30		–0.5	V_{DDD}+0.5	V
$V_{I\ R}$	input voltage channel; pin 3		–0.5	V_{DDD}+0.5	V
T_{amb}	operating ambient temperature		–20	70	°C
T_{stg}	storage temperature		–40	150	°C
T_{XTAL}	maximum crystal temperature		-	150	°C
V_{ES}	electrostatic handling	note 2	-	2000	V

Notes to the limiting values

1. The substrate voltage must be lower than or equal to the lowest supply voltage.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DDD}, $V_{DDD\ L.\ R}$, V_{DDA} = +5 V; V_{SSD}, V_{SSA} = −5 V, $V_{SSD\ L.\ R}$ = −3.5 V; $V_{ref\ L.\ R}$ = −4 V; T_{amb} = 25°C; f_{CLK} = 8.46 MHz; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{SUB}	negative substrate voltage; pin 32	note 1	−7.0	-	−4.5	V
$V_{DDD\ L.\ R}$	positive digital supply voltage for one channel; pins 27 and 6		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage for both channels; pin 2		4.5	5.0	5.5	V
$V_{SSD\ L.\ R}$	negative digital supply voltage for one channel; pins 26 and 7		−4.0	−3.5	−3.0	V
V_{SSD}	negative digital supply voltage for both channels; pin 31		−5.5	−5.0	−4.5	V
V_{DDA}	positive analog supply voltage; pin 17		4.5	5.0	6.0	V
V_{SSA}	negative analog supply voltage; pin 16		−6.0	−5.0	−4.5	V
$V_{DDD\ L.\ R}$ - $V_{SSD\ L.\ R}$	supply voltage difference between pins 27, 6 and pins 26, 7		-	-	9.0	V
$V_{SSD\ L.\ R}$ - V_{SSD}	supply voltage difference between pins 26, 7 and pin 31		1.3	-	-	V
$I_{DDD\ L.\ R}$	positive digital supply current for one channel; pins 27 and 6		-	0.1	-	mA
I_{DDD}	digital supply current for both channels; pin 2			29.0	46	mA
$I_{SSD\ L.\ R}$	negative digital supply current for one channel; pins 26 and 7		-	−0.1	-	mA
I_{SSD}	negative supply current for both channels; pin 31		−45	−28.0	-	mA
$-I_{DDA}$	positive analog supply current; pin 17		-	51.0	63	mA
I_{SSA}	negative analog supply current; pin 16		−63.0	−51.0	-	mA
P_{SSR1}	power supply rejection ratio	$V_{DDD\ L.\ R}$; note 6	50	-	-	dB
P_{SSR2}	power supply rejection ratio	V_{DDD}; note 6	50	-	-	dB
P_{SSR3}	power supply rejection ratio	$V_{SSD\ L.\ R}$; note 6	60	-	-	dB
P_{SSR4}	power supply rejection ratio	V_{SSD}; note 6	50	-	-	dB
P_{SSR5}	power supply rejection ratio	V_{DDA}; note 6	60	-	-	dB
P_{SSR6}	power supply rejection ratio	V_{SSA}; note 6	60	-	-	dB
P_{tot}	total power dissipation		-	800	-	mW
Clock - Input						
V_{IL}	input voltage LOW		-	-	0.5	V
V_{IH}	input voltage HIGH		4.5	-	-	V
I_{IL}	input current LOW	V_i = 0.5 V	−10	-	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Clock - Input						
I_{IH}	input current HIGH	V_i = 4.5 V	−10	-	10	µA
C_i	clock input capacitance		-	5	-	pF
f_{CLK}	clock input frequency		-	-	10	MHz
Channel left/right inputs						
V_{IL}	input voltage LOW		-	-	0.5	V
V_{IH}	input voltage HIGH		-	4.5	-	V
I_{IL}	input current LOW	V_i = 0.5 V	−10	-	10	µA
I_{IH}	input current HIGH	V_i = 4.5 V	−10	-	10	µA
C_i	channel input capacitance; pins 3, 30		-	5	-	pF
V_{ref}	reference input voltage; pins 8, 25	note 2	-	−4 ±0.4	-	V
Audio outputs						
$V_{OUT(RMS)}$	output voltage (RMS value); pins 14, 19; pins 15, 18	notes 2 and 3	0.85	1.0	1.15	V
(THD + N)/S	THD + Noise; 0 dB	f = 1 kHz; notes 3 and 4	-	−101	−96	dB
			-	0.0009	0.0016	%
(THD + N)/S	THD + Noise; 0 dB	20 Hz - 20 kHz; notes 3 and 5	-	−101	-	dB
			-	0.0009	-	%
(THD + N)/S	THD + Noise; −20 dB	f = 1 kHz; notes 3 and 4	-	−88	−84	dB
(THD + N)/S	THD + Noise; −60 dB	f = 1 kHz; notes 3 and 4	-	−48	−44	dB
S/N	signal-to-noise ratio	pattern 0101; notes 3 and 7	109	111	-	dB
S/N	signal-to-noise ratio; "A"-weighting	pattern 0101; notes 3 and 7	-	113	-	dB
α	channel separation	f = 1 kHz	101	115	-	dB
Timing						
t_r	rise time clock input	C_L = 20 pF	-	5	10	ns
t_f	fall time clock input	C_L = 20 pF	-	5	10	ns
$t_{CLK\ L}$	clock input LOW time		45	-	-	ns
$t_{CLK\ H}$	clock input HIGH time		45	-	-	ns
t_r	channel input rise time	C_L = 20 pF	-	10	15	ns
t_f	channel input fall time	C_L = 20 pF	-	10	15	ns
t_{HD}	channel input hold time		25	-	-	ns
t_{SU}	channel input set-up time		0	-	-	ns

Notes to the characteristics

1. The substrate voltage must be lower than or to equal than the lowest supply voltage.
2. Output level tracks linearly with both the clock frequency and the reference voltage ($V_{ref\ L}$ or $V_{ref\ R}$).
3. Device measured in differential mode with external components as shown in Fig.5.
4. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 1 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
5. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 20 Hz to 20 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
6. Power supply rejection ratio measured with f_{ripple} = 1 kHz and v_{ripple} = 100 mV.
7. The specified signal-to-noise ratio includes noise introduced by the application components as shown in Fig.5.

TIMING

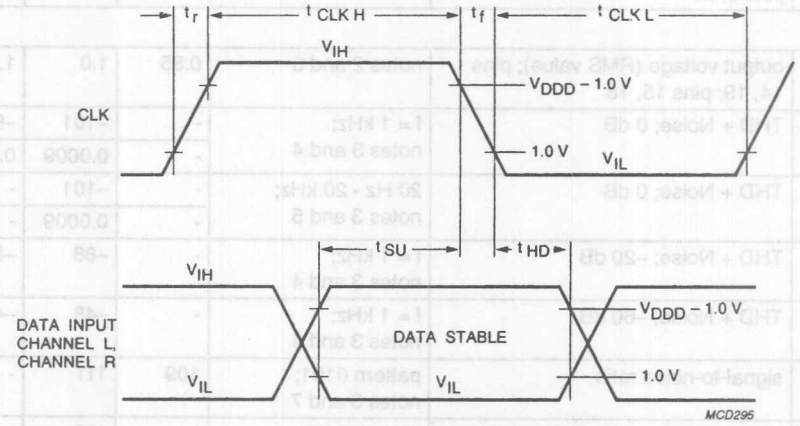


Fig.3 Timing waveform.

APPLICATION INFORMATION

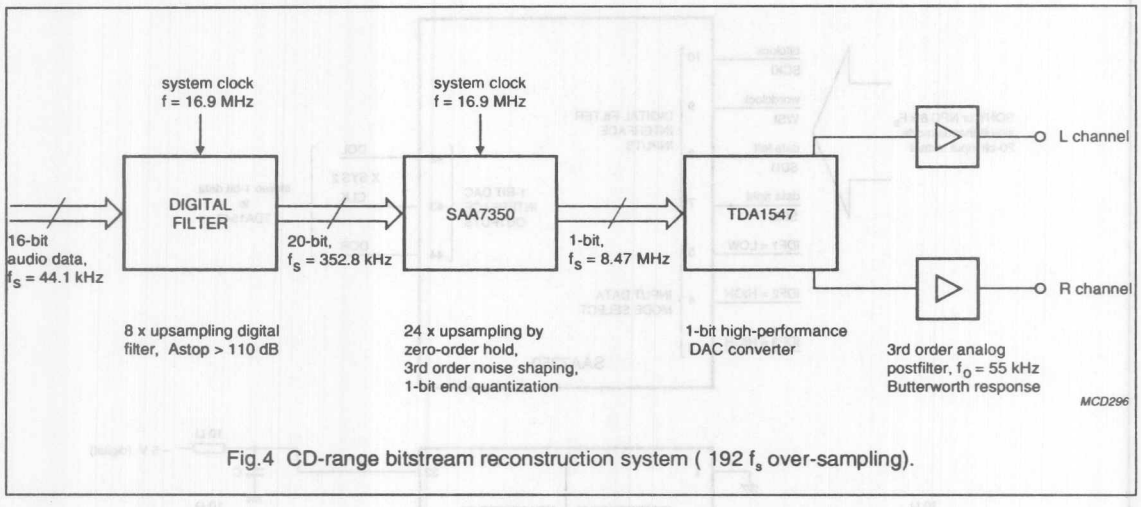


Fig.4 CD-range bitstream reconstruction system (192 f_s over-sampling).

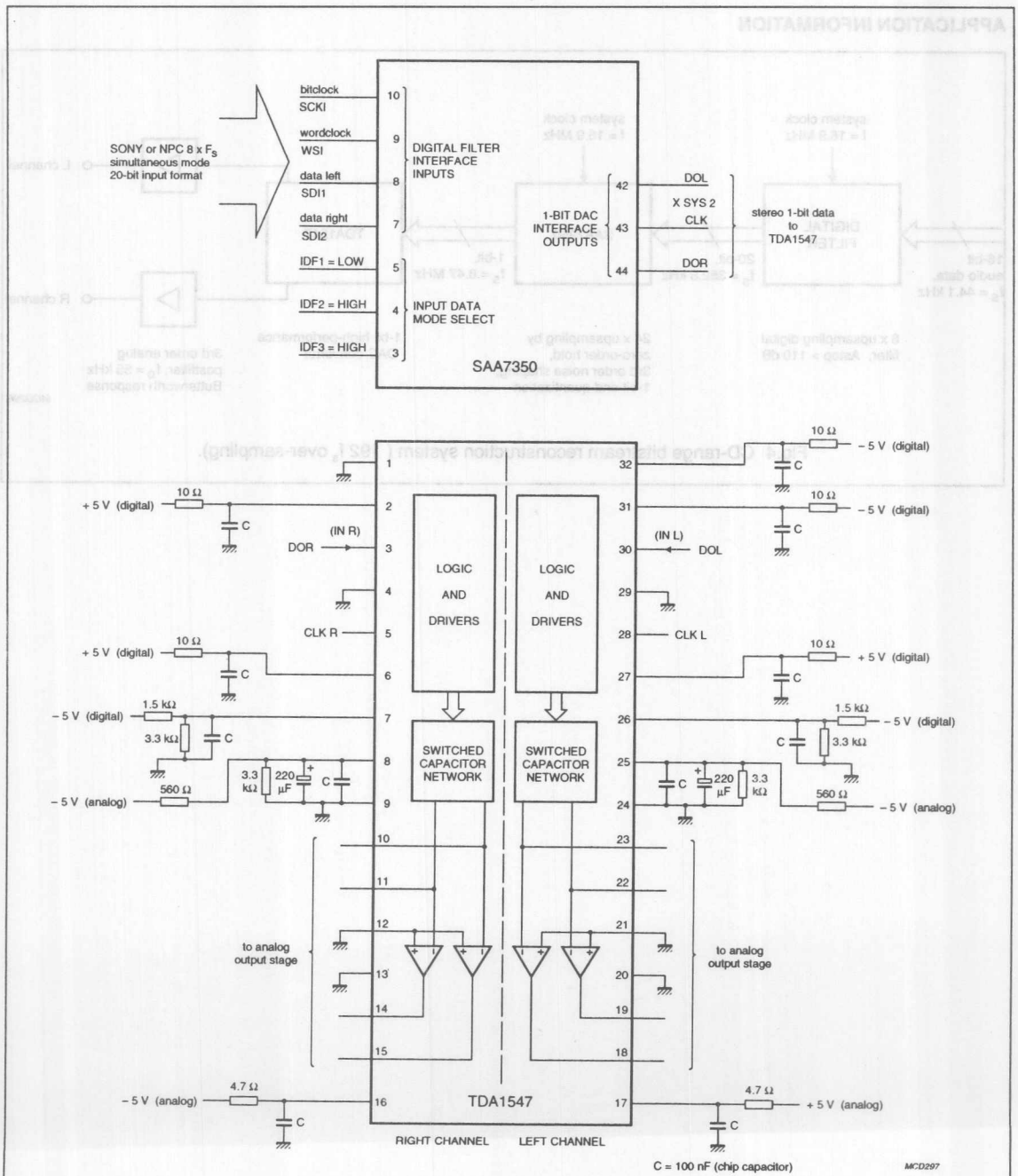


Fig.5 Application diagram.

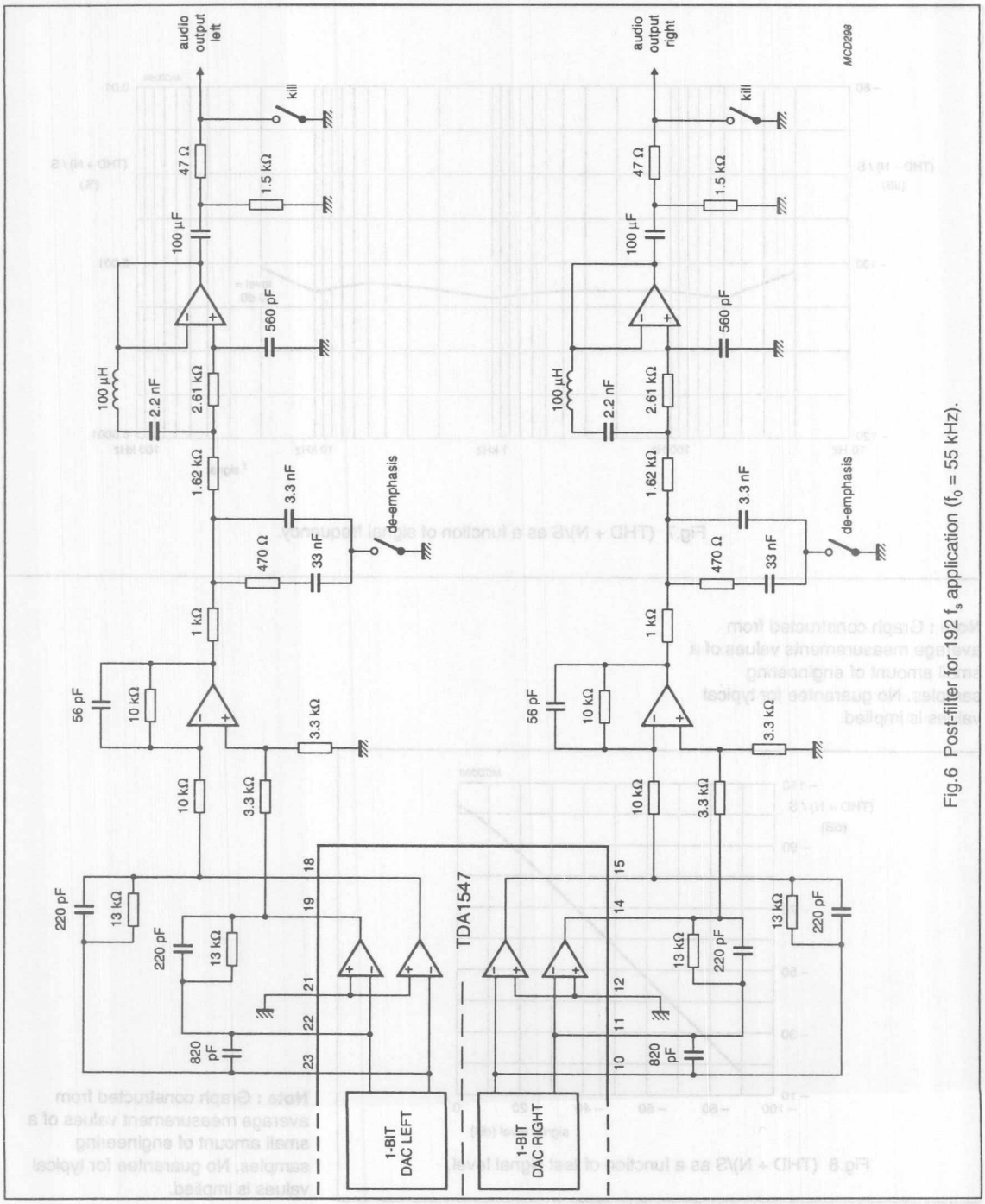


Fig.6 Post-filter for 192 f_s application (f_0 = 55 kHz).

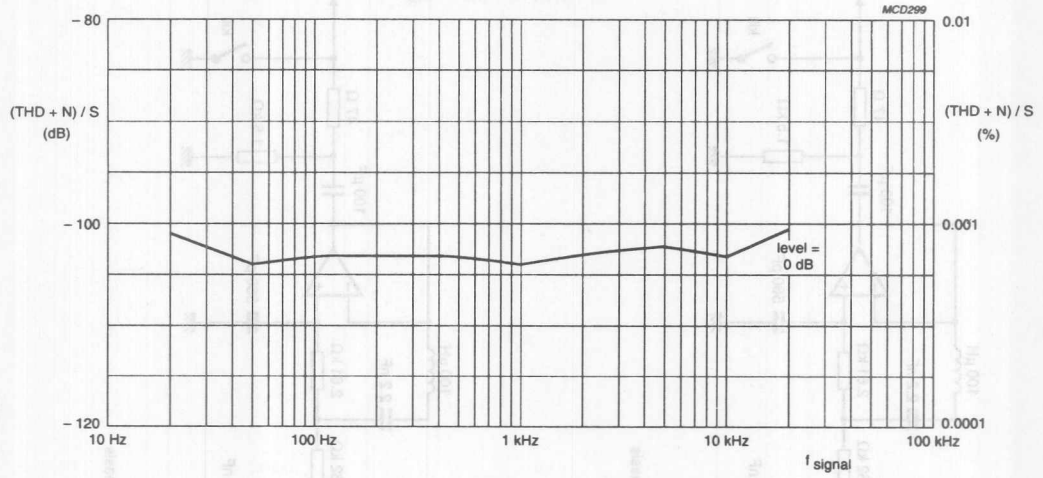


Fig.7 (THD + N)/S as a function of signal frequency.

Note : Graph constructed from average measurements values of a small amount of engineering samples. No guarantee for typical values is implied.

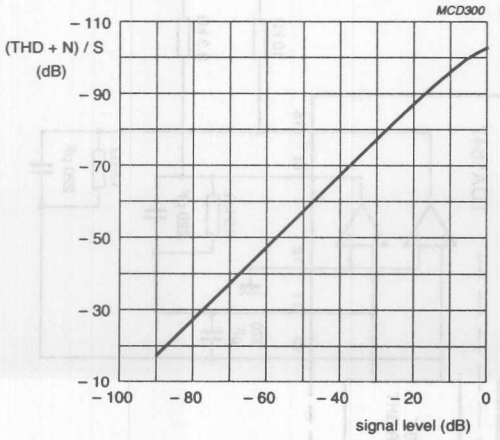


Fig.8 (THD + N)/S as a function of test signal level.

Note : Graph constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.

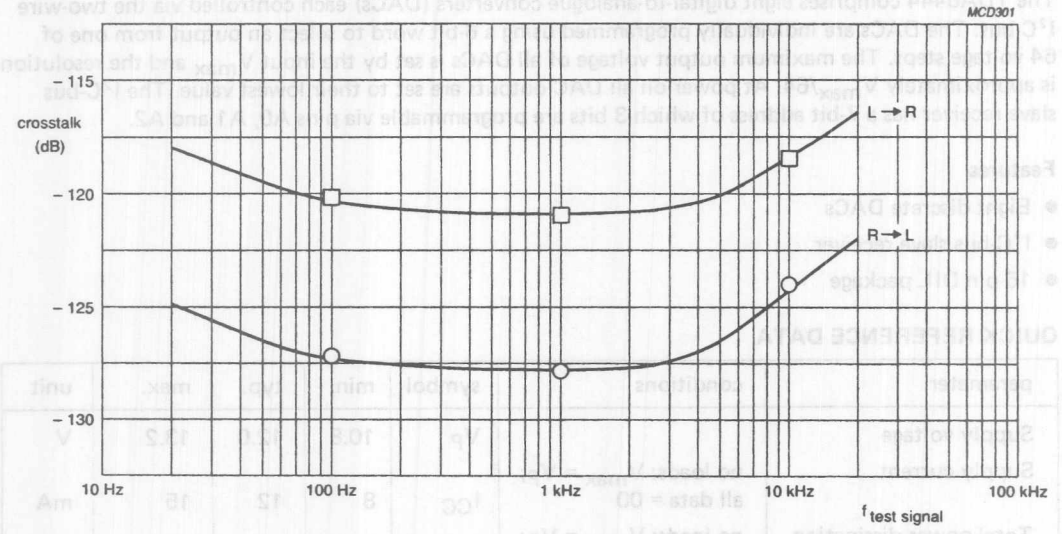


Fig.9 Inter-channel crosstalk as a function of signal frequency.

Note : Graph constructed from average measurements values of a small amount of engineering samples. No guarantee for typical values is implied.

Octuple 6-bit DAC with I²C-bus

TDA8444/AT/T

GENERAL DESCRIPTION

The TDA8444 comprises eight digital-to-analogue converters (DACs) each controlled via the two-wire I²C-bus. The DACs are individually programmed using a 6-bit word to select an output from one of 64 voltage steps. The maximum output voltage of all DACs is set by the input V_{max} and the resolution is approximately $V_{max}/64$. At power-on all DAC outputs are set to their lowest value. The I²C-bus slave receiver has a 7-bit address of which 3 bits are programmable via pins A0, A1 and A2.

Features

- Eight discrete DACs
- I²C-bus slave receiver
- 16-pin DIL package

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	I_{CC}	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input	V_P = 12 V	V_{max}	1	–	10.5	V
DAC output voltage range		V_O	0.1	–	V_P–0.5	V
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

Octuple 6-bit DAC with I²C-bus TDA8444/AT/T

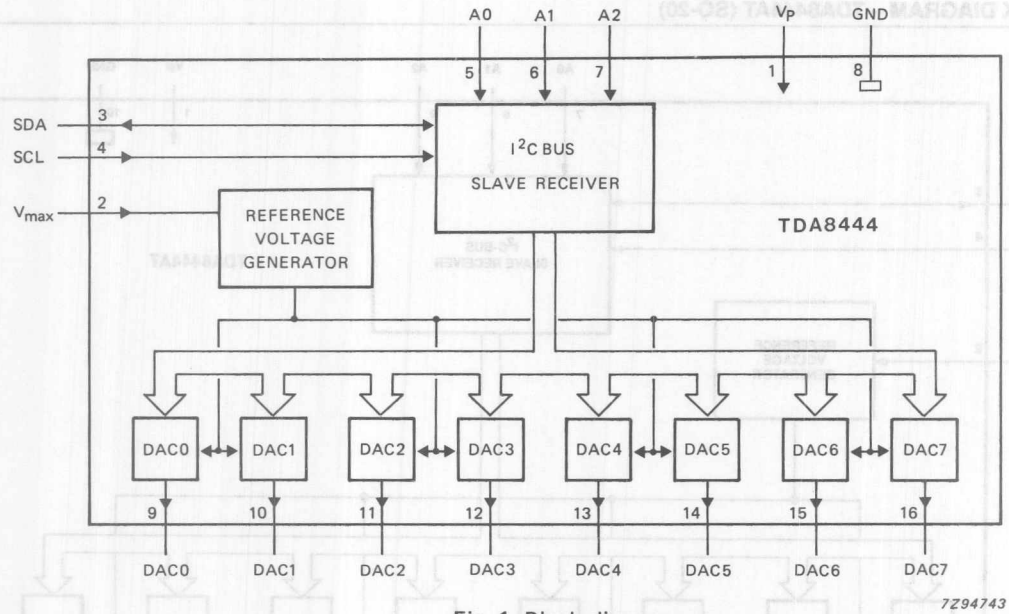


Fig. 1 Block diagram.

PINNING

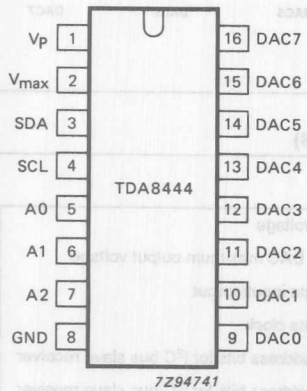
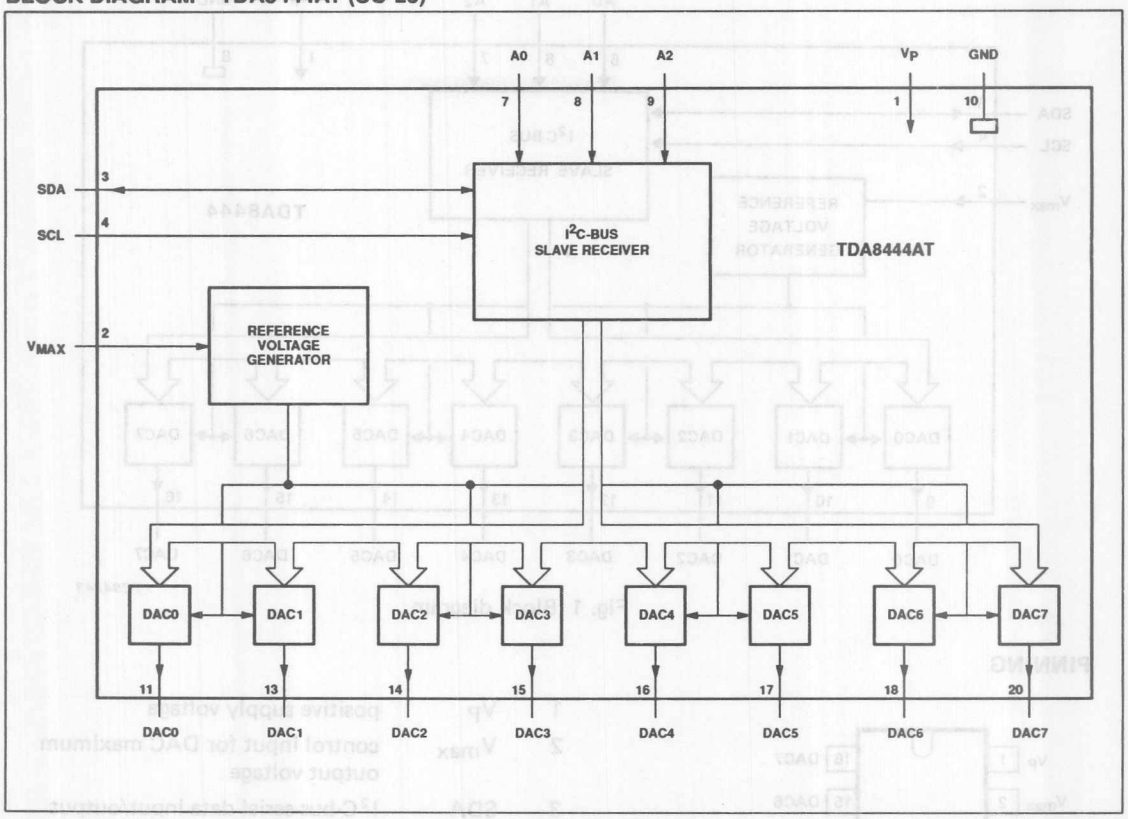


Fig. 2 Pinning diagram.

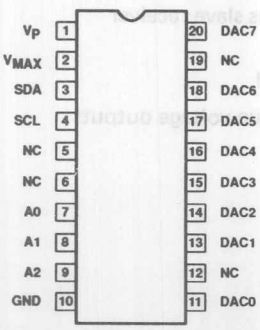
1	V_P	positive supply voltage
2	V_{max}	control input for DAC maximum output voltage
3	SDA	I²C-bus serial data input/output
4	SCL	I²C-bus serial data clock
5	A0	programmable address bits for I²C-bus slave receiver
6	A1	
7	A2	
8	GND	ground
9-16	DAC0-7	analogue voltage outputs

Octuple 6-bit DAC with I²C-bus TDA8444/AT/T

BLOCK DIAGRAM – TDA8444AT (SO-20)



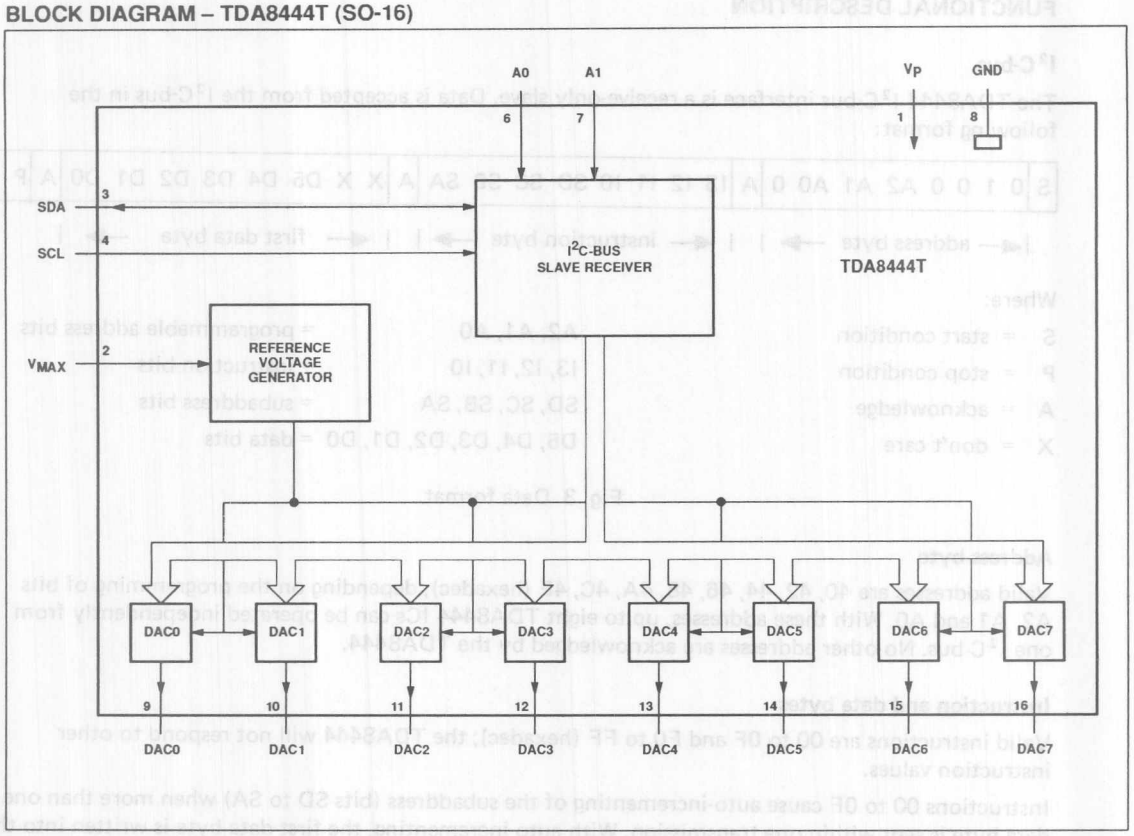
PIN CONFIGURATION AND DESCRIPTION – TDA8444AT (SO-20, SOT-163)



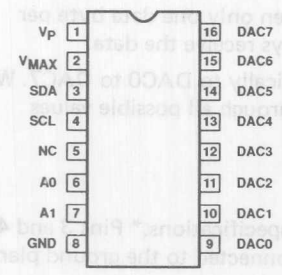
1	V_P	Positive supply voltage
2	V_{MAX}	Control input for DAC maximum output voltage
3	SDA	I²C bus serial data input/output
4	SCL	I²C bus serial data clock
7	A0	Programmable address bits for I²C bus slave receiver
8	A1	Programmable address bits for I²C bus slave receiver
9	A2	Programmable address bits for I²C bus slave receiver
10	GND	Ground
11, 13-18, 20	DAC0-7	Analog voltage outputs

Octuple 6-bit DAC with I²C-bus TDA8444/AT/T

BLOCK DIAGRAM – TDA8444T (SO-16)



PIN CONFIGURATION AND DESCRIPTION – TDA8444T (SO-16, SOT-162)



1	V_p	Positive supply voltage
2	V_{MAX}	Control input for DAC maximum output voltage
3	SDA	I²C bus serial data input/output
4	SCL	I²C bus serial data clock
6	A0	Programmable address bits for I²C bus slave receiver
7	A1	Programmable address bits for I²C bus slave receiver
8	GND	Ground
9-16	DAC0-7	Analog voltage outputs

FUNCTIONAL DESCRIPTION

I²C-bus

The TDA8444 I²C-bus interface is a receive-only slave. Data is accepted from the I²C-bus in the following format:

S	0 1 0 0 A2 A1 A0 0	A	I3 I2 I1 I0 SD SC SB SA	A	X X D5 D4 D3 D2 D1 D0	A	P
	← address byte →		← instruction byte →		← first data byte →		

Where:

S	= start condition	A2, A1, A0	= programmable address bits
P	= stop condition	I3, I2, I1, I0	= instruction bits
A	= acknowledge	SD, SC, SB, SA	= subaddress bits
X	= don't care	D5, D4, D3, D2, D1, D0	= data bits

Fig. 3 Data format.

Address byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E (hexadec), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight TDA8444 ICs can be operated independently from one I²C-bus. No other addresses are acknowledged by the TDA8444.

Instruction and data bytes

Valid instructions are 00 to 0F and F0 to FF (hexadec); the TDA8444 will not respond to other instruction values.

Instructions 00 to 0F cause auto-incrementing of the subaddress (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addressed by bits SD to SA and then the subaddress is automatically incremented by one position for the next data byte in the series.

Auto-incrementation does not occur with instructions F0 to FF. Other than auto-incrementation there is no difference between instructions 00 to 0F and F0 to FF. When only one data byte per transmission is present, the DAC addressed by the subaddress will always receive the data.

Valid subaddresses (bits SD to SA) are 0 to 7 (hexadec) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the subaddress will sequence through all possible values (0 to F, 0 to F, etc.).

I²C-bus

Input SCL (pin 3) and input/output SDA (pin 4) conform to I²C-bus specifications.* Pins 3 and 4 are protected against positive voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1, A2 are programmed by a connection to GND for An = 0 or to V_P for An = 1. If the inputs are left floating, An = 1 will result.

FUNCTIONAL DESCRIPTION (continued)

Input V_{max}

Input V_{max} (pin 2) provides a means of compressing the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately V_{max} while the 6-bit resolution is maintained, so giving a finer voltage resolution of smaller output swings.

Digital-to-analogue converters

Each DAC comprises a 6-bit data latch, current switches and an output driver. Current sources with values weighted by 2^0 up to 2^5 are switched according to the data input so that the sum of the selected currents gives the required analogue voltage from the output driver. The range of the output voltage is approximately 0.5 to 10.5 V when $V_{max} = V_P$.

The DAC outputs are protected against short-circuits to V_P and GND.

To avoid the possibility of oscillations, capacitive loading at the DAC outputs should not exceed 2 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		$V_P = V_1$	−0.5	18	V
Supply current (source)		$I_p = I_1$	–	−10	mA
		$I_P = I_I$	–	40	mA
I²C-bus line voltage		$V_{3,4}$	−0.5	5.9	V
Input voltage		V_I	−0.5	V_P + 0.5	V
Output voltage		V_O	−0.5	V_P + 0.5	V
Maximum current on any pin (except pins 1 and 8)		$\pm I_{max}$	–	10	mA
Total power dissipation		P_{tot}	–	500	mW
Operating ambient temperature range		T_{amb}	−20	+ 70	°C
Storage temperature range		T_{stg}	−65	+ 150	°C

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 75 K/W

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

All voltages are with respect to GND; T_{amb} = 25 °C; V_P = 12 V unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10.8	12.0	13.2	V
Voltage level for power-on reset		V_1	1	–	4.8	V
Supply current	no loads; $V_{max} = V_P$; all data = 00	$I_P = I_1$	8	12	15	mA
Total power dissipation	no loads; $V_{max} = V_P$; all data = 00	P_{tot}	–	150	–	mW
Effective range of V_{max} input (pin 2)	V_P = 12 V	$V_{max} = V_2$	1.0	–	10.5	V
Pin 2 current	V_2 = 1 V	I_2	–	–	−10	μA
	$V_2 = V_P$	I_2	–	–	10	μA
SDA, SCL inputs (pins 3 and 4)						
Input voltage range		V_I	0	–	5.5	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	–	V
Input current LOW	$V_{3;4}$ = 0.3 V	I_{IL}	–	–	−10	μA
Input current HIGH	$V_{3;4}$ = 6 V	I_{IH}	–	–	±10	μA
SDA output (pin 3)						
Output voltage LOW	I_3 = 3 mA	V_{OL}	–	–	0.4	V
Sink current		I_O	3	8	–	mA
Address inputs (pins 5 to 7)						
Input voltage range		V_I	0	–	V_P	V
Input voltage LOW		V_{IL}	–	–	1	V
Input voltage HIGH		V_{IH}	2.1	–	–	V
Input current LOW		I_{IL}	–	−7	−12	μA
Input current HIGH		I_{IH}	–	–	1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
DAC outputs (pins 9 to 16)						
Output voltage range		V_O	0.1	–	V_P–0.5	V
Minimum output voltage	data = 00; I_O = –2 mA	V_{Omin}	0.1	0.4	0.8	V
Maximum output voltage	data = 3F; I_O = –2 mA					
at $V_{max} = V_P$		V_{Omax}	10	10.5	11.5	V
at $1 < V_{max} < 10.5$ V		V_{Omax}		see note		V
Output sink current	V = V_P; data = 1F	I_O	2	8	15	mA
Output source current	V = 0V; data = 1F	I_O	–2	–	–6	mA
Output impedance	data = 1F; $-2 < I_O < +2$ mA	Z_O	–	4	50	Ω
Step value of 1 LSB	$V_{max} = V_P$; I_O = –2 mA	V_{LSB}	70	160	250	mV
Deviation from linearity	I_O = –2 mA; N ≠ 32		0	–	50	mV
Deviation from linearity	I_O = –2 mA; N = 32		0	–	70	mV

Note to the characteristics

$V_O = 0.95\ V_{max} + V_{Omin}$.

APPLICATION INFORMATION

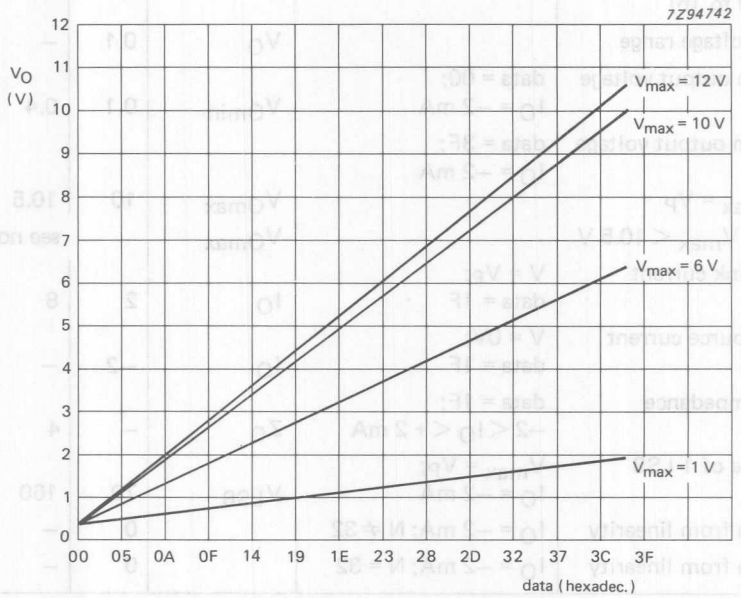


Fig. 4 Graph showing output voltage as a function of the input data value for V_{max} values of 1, 6, 10 and 12 V; V_P = 12 V.

8-bit video digital-to-analog converter

TDA8702/T

FEATURES

- 8-bit resolution
- Conversion rate up to 30 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High-speed digital-to-analog conversion
- Digital TV including:
  - field progressive scan
  - line progressive scan
- Subscriber TV decoders
- Satellite TV decoders
- Digital VCRs.

DESCRIPTION

The TDA8702 is a monolithic bipolar 8-bit digital-to-analog converter (DAC) for video and other applications. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 30 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	-	26	32	mA
I_{CCD}	digital supply current	note 1	-	23	30	mA
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltage (peak-to-peak value)	Z_L = 10 kΩ Z_L = 75 Ω	−1.45 −0.72	−1.60 −0.80	−1.75 −0.88	V V
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
f_{CLK}	maximum conversion rate		30	-	-	MHz
B	−3 dB bandwidth	f_{CLK} = 30 MHz	-	150	-	MHz
P_{tot}	total power dissipation		-	250	340	mW

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8702	16	DIL	plastic	SOT38GE1
TDA8702T	16	SO16	plastic	SOT162A

Notes to the Quick Reference Data

1. D0 to D7 connected to V_{CCD} and CLK connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

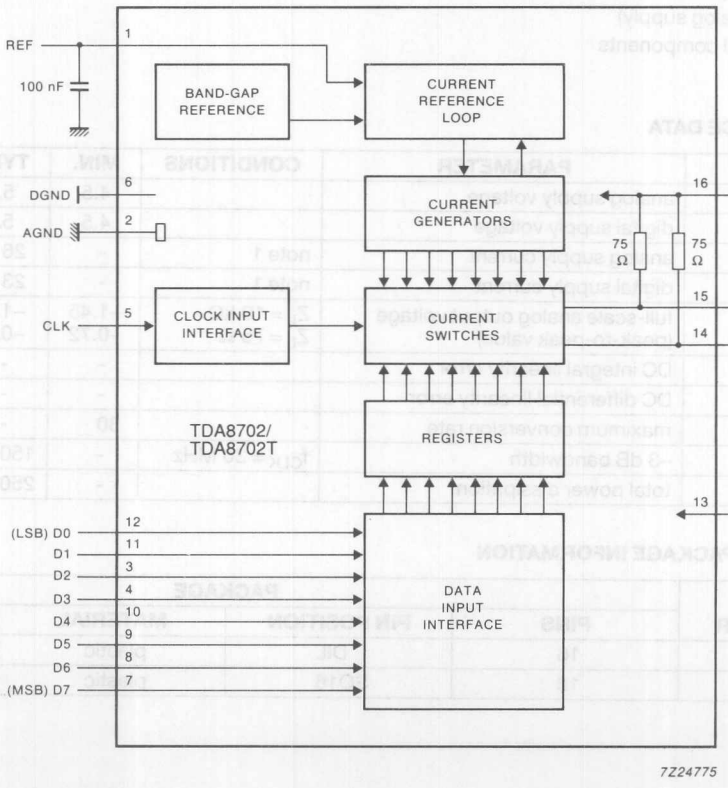


Fig.1 Block diagram.

8-bit video digital-to-analog converter TDA8702/TDA8702T

PIN CONFIGURATION

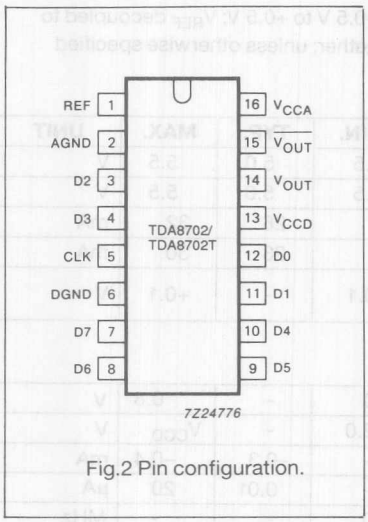


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input, bit 2
D3	4	data input, bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input, bit 7
D6	8	data input, bit 6
D5	9	data input, bit 5
D4	10	data input, bit 4
D1	11	data input, bit 1
D0	12	data input, bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$\overline{V_{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	− 0.3	+ 7.0	V
V_{CCD}	digital supply voltage range	− 0.3	+ 7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differential	− 0.5	+ 0.5	V
AGND – DGND	ground voltage differential	− 0.1	+ 0.1	V
V_I	input voltage range (pins 3 to 5 and 7 to 12)	− 0.3	V_{CCD}	V
I_{14}/I_{15}	total output current range (pins 14 and 15)	− 5	+ 26	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
T_j	junction temperature	-	+125	°C

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT38GE1	+ 85	K/W
$R_{th\ j\text{-}a}$	SOT162A	+110	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_{16} - V_2 = 4.5$ V to 5.5 V; $V_{CCD} = V_{13} - V_6 = 4.5$ V to 5.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; V_{REF} decoupled to AGND by a 100 nF capacitor; $T_{amb} = 0$ °C to 70 °C; AGND and DGND shorted together; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = 5.0$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	-	26	32	mA
I_{CCD}	digital supply current	note 1	-	23	30	mA
AGND – DGND	ground voltage differential		–0.1	-	+0.1	V
Inputs DIGITAL INPUTS (D7 – D0) AND CLOCK INPUT (CLK)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	-	–0.3	–0.4	mA
I_{IH}	input current HIGH	$V_I = 2.7$ V	-	0.01	20	µA
f_{CLK}	maximum clock frequency		30	-	-	MHz
Outputs (note 2; referenced to V_{CCA})						
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltages	$Z_L = 10$ kΩ	–1.45	–1.61	–1.75	V
	(peak- to-peak value)	$Z_L = 75$ Ω	–0.72	–0.80	–0.88	V
V_{offset}	analog offset output voltage	code = 0	-	–3	–25	mV
ΔV_{OUT}	full-scale analog output voltage temperature coefficient		-	-	200	µV/K
ΔV_{offset}	analog offset output voltage temperature coefficient		-	-	20	µV/k
B	–3 dB bandwidth	note 3; f_{CLK} = 30 MHz	-	150	-	MHz
G_d	differential gain		-	0.6	-	%
ϕd	differential phase		-	1	-	deg
Z_o	output impedance		-	75	-	Ω

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Transfer function (f_{CLK} = 30 MHz)						
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
Switching characteristics (f_{CLK} = 30 MHz; notes 4 and 5; see Figs 3 4 and 5)						
$t_{SU;\,DAT}$	data set-up time		−0.3	-	-	ns
$t_{HD;\,DAT}$	data hold time		2	-	-	ns
t_{PD}	propagation delay time		-	-	1.0	ns
t_{S1}	settling time	10% to 90% full-scale change to ±1 LSB	-	1.1	1.5	ns
t_{S2}	settling time	10% to 90% full-scale change to ±1 LSB	-	6.5	8.0	ns
t_d	input to 50% output delay time		-	3.0	5.0	ns
Output transients (glitches; f_{CLK} = 30 MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	-	-	30	ns

Notes to the characteristics

1. D0 to D7 connected to V_{CCD}, CLK connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The −3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).
4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $V_{\overline{OUT}}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data are latched at the rising-edge of the clock. The output voltage remains stable (independent of input data variations) during the high level of the clock (CLK = HIGH). During LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages, see Fig.5).
5. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising-edge of the clock and still be recognized. The data hold time ($t_{HD;\,DAT}$) is the minimum period following the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising-edge of the clock and still be recognized.
6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 to 128 and on the falling-edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of offset voltage)

CODE	BINARY INPUT DATA (D7 – D0)	DAC OUTPUT VOLTAGES			
		Z_L = 10 kΩ		Z_L = 75 Ω	
		V_{OUT} (V)	$\overline{V_{OUT}}$ (V)	V_{OUT} (V)	$\overline{V_{OUT}}$ (V)
0	000 00 00	0	−1.6	0	−0.8
1	000 000 01	−0.006	−1.594	−0.003	−0.797
.	. . . . .				
128	100 000 00	−0.8	−0.8	−0.4	−0.4
.	. . . . .				
254	111 111 10	−1.594	−0.006	−0.797	−0.003
255	111 111 11	−1.6	0	−0.8	0

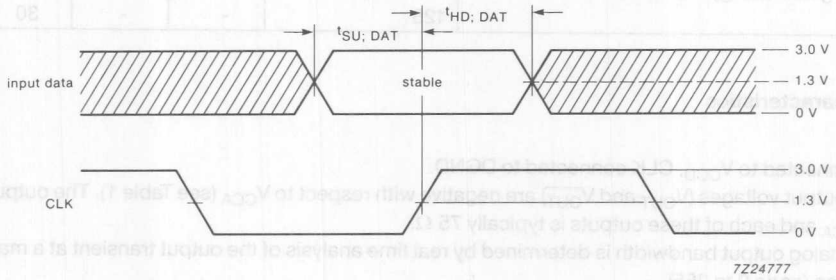


Fig.3 Data set-up and hold times.

Note to Fig.3

The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns, after the first rising-edge of the clock ($t_{SU;\ DAT}$ is negative; −0.3 ns). Data must be held at least 2 ns after the rising-edge ($t_{HD;\ DAT}$ = +2 ns).

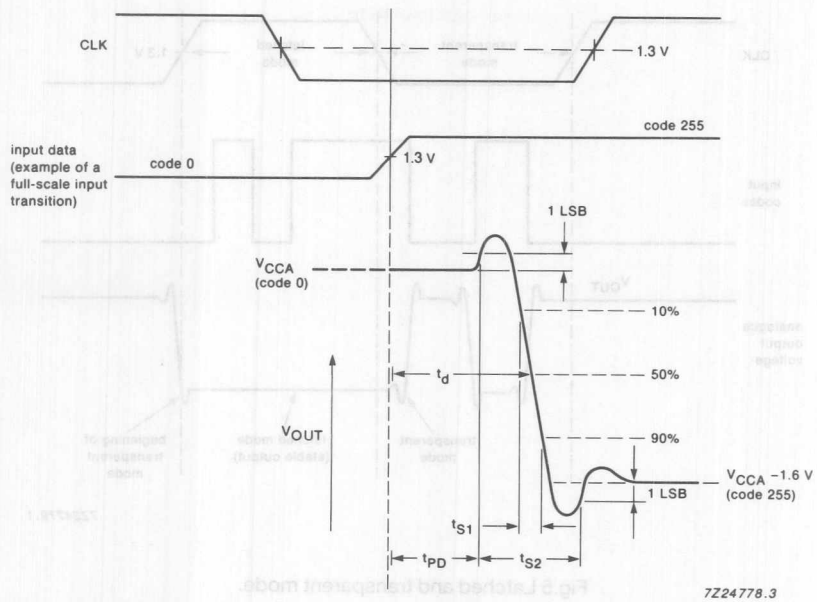


Fig.4 Switching characteristics.

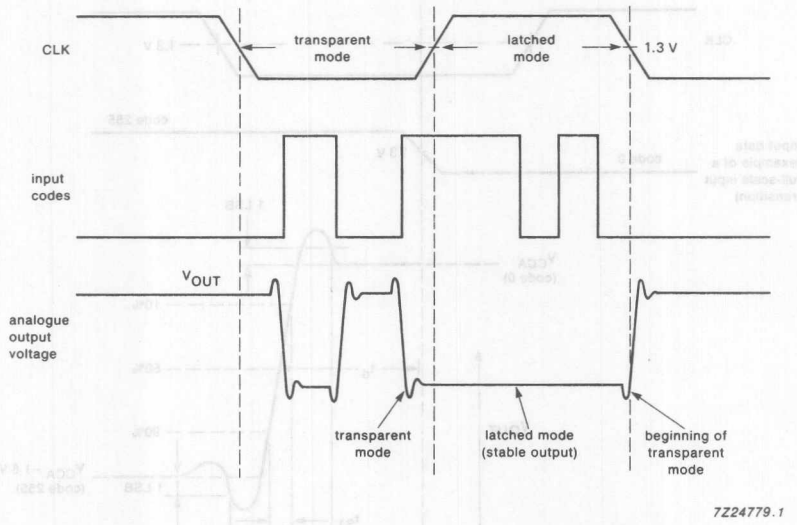


Fig.5 Latched and transparent mode.

Note to Fig.5

During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable, regardless of any changes at the input. A change of input data during the latched mode will be seen on the falling-edge of the clock (beginning of the transparent mode).

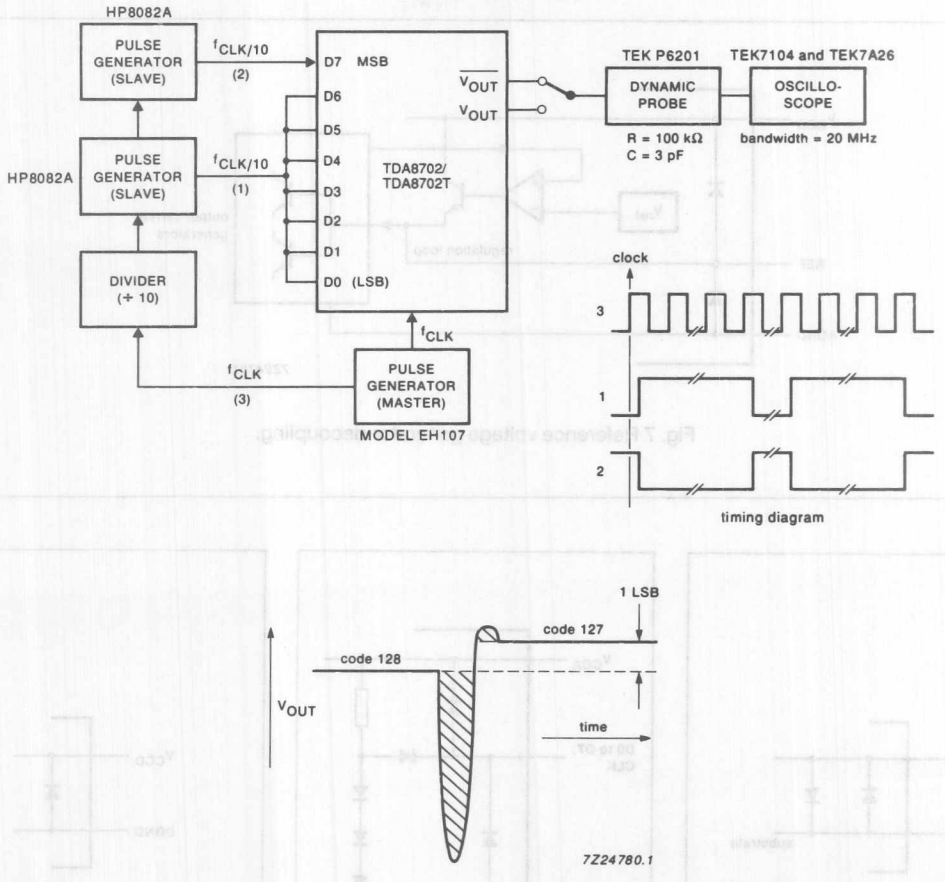


Fig.6 Glitch energy measurement.

Note to Fig.6

The value of the glitch energy is the sum of the shaded area measured in LSB.ns.

INTERNAL PIN CONFIGURATIONS

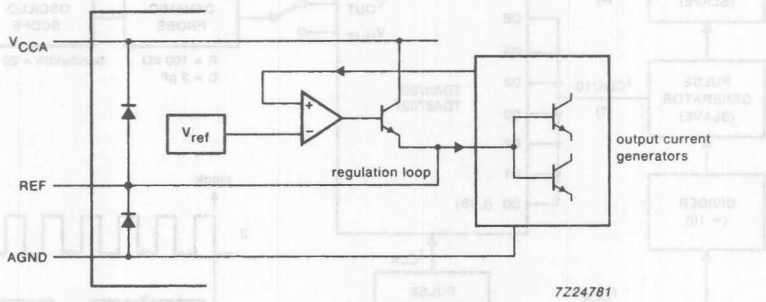


Fig. 7 Reference voltage generator decoupling.

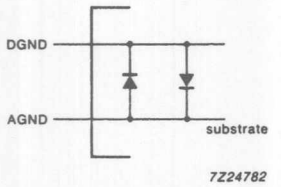


Fig.8 AGND and DGND.

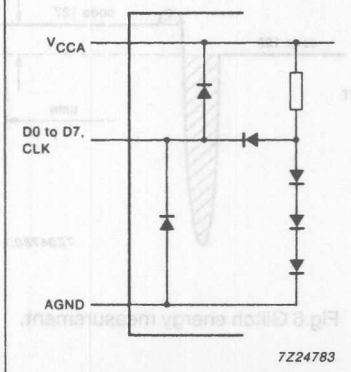


Fig.9 D7 to D0 and CLK.

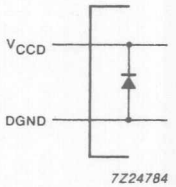


Fig.10 Digital supply.

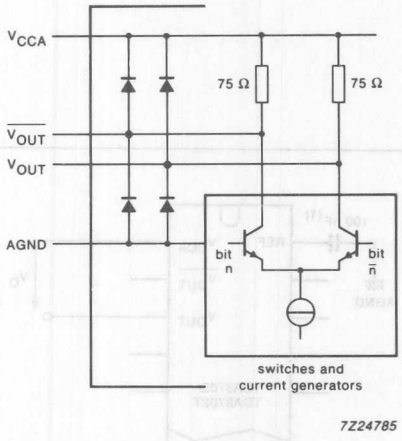


Fig.11 Analog outputs.

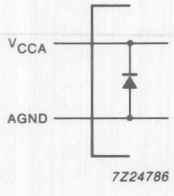


Fig.12 Analog supply.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

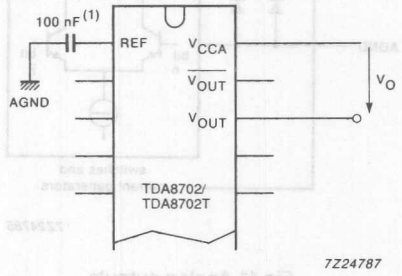


Fig.13 Analog output voltage without external load ($V_O = -\overline{V_{OUT}}$; see Table 1, Z_L = 10 kΩ).

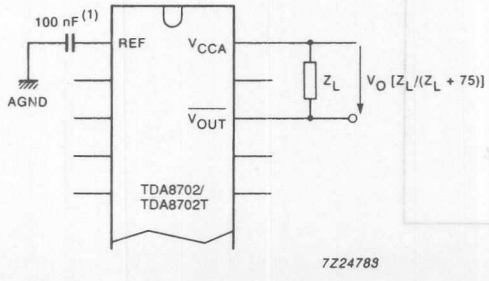


Fig.14 Analog output voltage with external load (external load Z_L = 75 Ω to ∞).

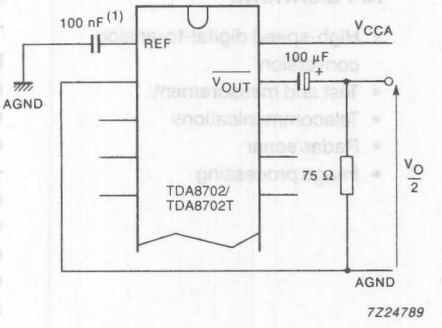


Fig.15 Analog output with AGND as reference.

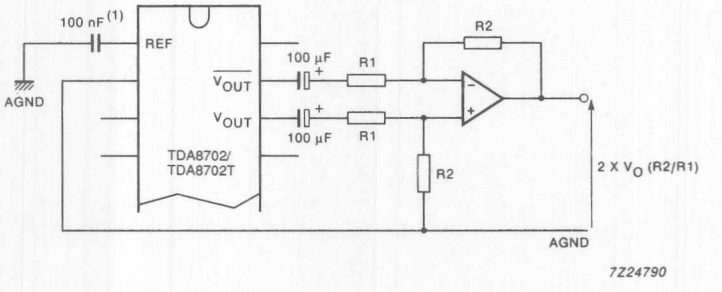


Fig.16 Differential mode (improved supply voltage ripple rejection).

Note to Figs 13, 14,15 and 16

1. This is a recommended value for decoupling pin 1.

8-bit video digital-to-analog converter (Mil. temp.) TDE8712D

FEATURES

- 8-bit resolution
- Conversion rate up to 50 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation (250 mW typical)
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High-speed digital-to-analog conversion
- Test and measurement
- Telecommunications
- Radar/sonar
- Image processing

DESCRIPTION

The TDE8712D is a monolithic bipolar 8-bit digital-to-analog converter (DAC) for professional video and other applications. The operating temperature range is -55 °C to +125 °C. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 50 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDE8712D	16	CERDIP	ceramic	SOT74

8-bit video digital-to-analog converter (Mil. temp.) TDE8712D

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current	note 1	20	26	32	mA
I_{CCD}	digital supply current	note 1	16	23	30	mA
V_{OUT} – $\overline{V_{OUT}}$	full-scale analog output voltage (peak-to-peak value)	Z_L = 10 kΩ	–1.45	–1.60	–1.75	V
		Z_L = 75 Ω	–0.72	–0.80	–0.88	V
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
f_{CLK}	maximum conversion rate		50	-	-	MHz
B	–3 dB bandwidth	f_{CLK} = 50 MHz	-	150	-	MHz
P_{tot}	total power dissipation		-	250	340	mW

Notes to the Quick Reference Data

1. D0 to D7 connected to V_{CCD} and CLK connected to DGND.
2. The analog output voltages (V_{OUT} and $\overline{V_{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

8-bit video digital-to-analog converter (Mil. temp.) TDE8712D

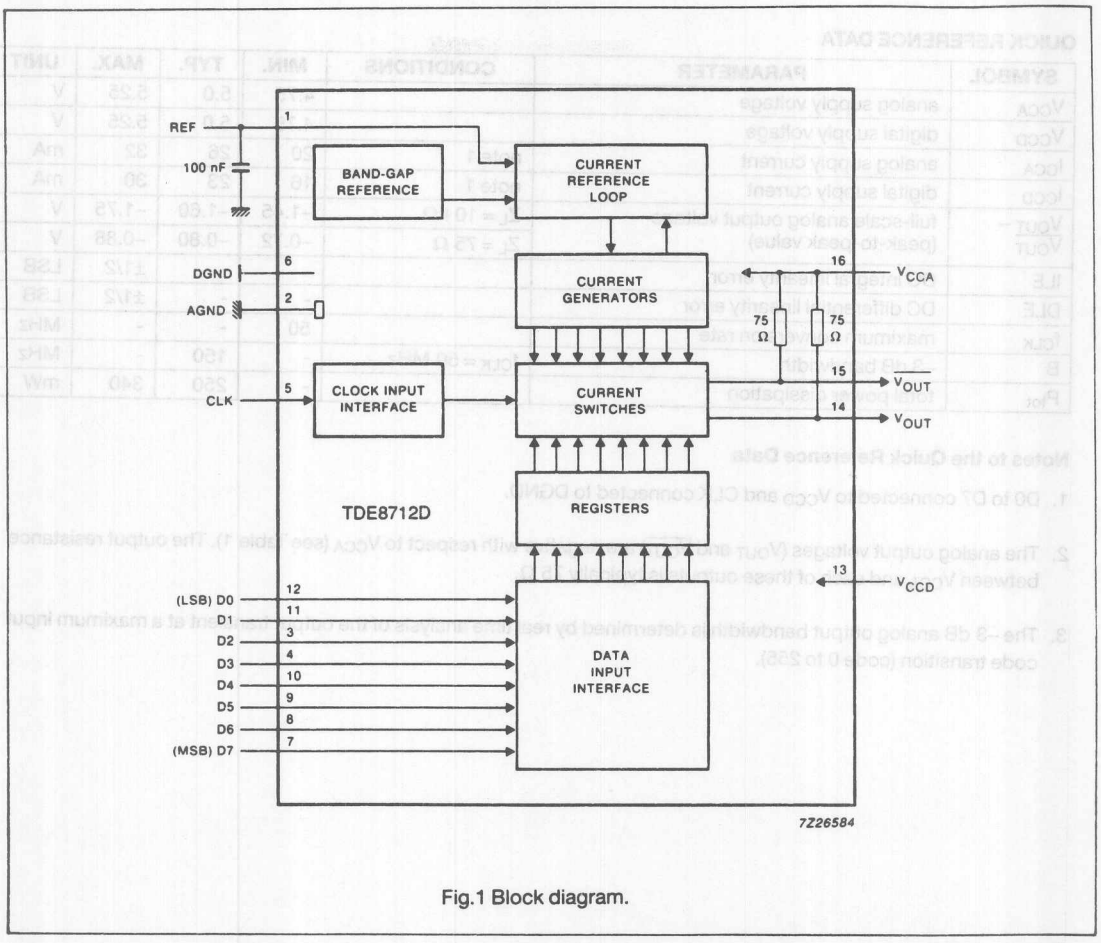


Fig.1 Block diagram.

8-bit video digital-to-analog converter (Mil. temp.) TDE8712D

PIN CONFIGURATION

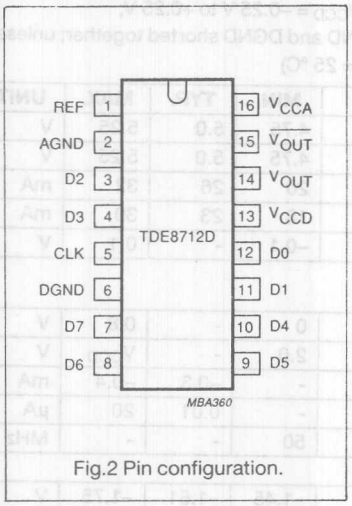


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input, bit 2
D3	4	data input, bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input, bit 7
D6	8	data input, bit 6
D5	9	data input, bit 5
D4	10	data input, bit 4
D1	11	data input, bit 1
D0	12	data input, bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$\overline{V_{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range	−0.3	+ 7.0	V
V_{CCD}	digital supply voltage range	−0.3	+ 7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differential	−0.5	+ 0.5	V
AGND – DGND	ground voltage differential	−0.1	+ 0.1	V
V_I	input voltage range (pins 3 to 5 and 7 to 12)	−0.3	V_{CCD}	V
I_{OUT}	total output current range (pin 14)	−5	+ 26	mA
$\overline{I_{OUT}}$	total output current range (pin 15)	−5	+ 26	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−55	+125	°C
T_j	junction temperature	-	+175	°C

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j\text{-}a}$	SOT74	112	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

$V_{CCA} = V_{16} - V_2 = 4.75$ V to 5.25 V; $V_{CCD} = V_{13} - V_6 = 4.75$ V to 5.25 V; $V_{CCA} - V_{CCD} = -0.25$ V to +0.25 V; V_{REF} decoupled to AGND by a 100 nF capacitor; $T_{amb} = -55$ °C to +125 °C; AGND and DGND shorted together; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = 5.0$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
I_{CCA}	analog supply current	note 1	20	26	32	mA
I_{CCD}	digital supply current	note 1	16	23	30	mA
AGND – DGND	ground voltage differential		–0.1	-	0.1	V
Inputs DIGITAL INPUTS (D7 - D0) AND CLOCK INPUT (CLK)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_I = 0.4$ V	-	–0.3	–0.4	mA
I_{IH}	input current HIGH	$V_I = 2.7$ V	-	0.01	20	µA
f_{CLK}	maximum clock frequency		50	-	-	MHz
Outputs (note 2; referenced to V_{CCA})						
$V_{OUT} - \overline{V_{OUT}}$	full-scale analog output voltages (peak- to-peak value)	$Z_L = 10$ kΩ	–1.45	–1.61	–1.75	V
		$Z_L = 75$ Ω	–0.72	–0.80	–0.88	V
V_{offset}	analog offset output voltage	code = 0	-	–3	–25	mV
ΔV_{OUT}	full-scale analog output voltage temperature coefficient		-	-	200	µV/K
ΔV_{offset}	analog offset output voltage temperature coefficient		-	-	20	µV/k
B	–3 dB bandwidth	note 3; $f_{CLK} = 50$ MHz	-	150	-	MHz
G_d	differential gain		-	0.6	-	%
ϕd	differential phase		-	1	-	deg
Z_o	output impedance		-	75	-	Ω
Transfer function ($f_{CLK} = 50$ MHz)						
ILE	DC integral linearity error		-	-	±1/2	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
Switching characteristics (fCLK = 50 MHz; notes 4 and 5; see Figs 3,4 and 5)						
$t_{SU;DAT}$	data set-up time		–0.3	-	-	ns
$t_{HD;DAT}$	data hold time		2	-	-	ns
t_{PD}	propagation delay time		-	-	1.0	ns
t_{S1}	settling time	10% to 90% full-scale change to ±1 LSB	-	1.1	1.5	ns
t_{S2}	settling time	10% to 90% full-scale change to ±1 LSB	-	6.5	8.0	ns
t_d	input to 50% output delay time		-	3.0	5.0	ns
Output transients (glitches; $f_{CLK} = 50$ MHz; note 6; see Fig.6)						
E_g	glitch energy from code	transition 127 to 128	-	-	30	ns

Notes to the characteristics

1. D0 to D7 connected to V_{CCD}, CLK connected to DGND.
2. The analog output voltages (V_{OUT} and $\overline{V_{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).
4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $\overline{V_{OUT}}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data are latched at the rising-edge of the clock. The output voltage remains stable (independent of input data variations) during the high level of the clock (CLK = HIGH). During LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages, see Fig.5).
5. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising-edge of the clock and still be recognized. The data hold time ($t_{HD;\ DAT}$) is the minimum period following the rising-edge of the clock, that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising-edge of the clock and still be recognized.
6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 to 128 and on the falling-edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of offset voltage)

DAC OUTPUT VOLTAGES					
CODE	BINARY INPUT DATA (D7 - D0)	Z_L = 10 kΩ	Z_L = 75 Ω		
		$\overline{V_{OUT}}$ (V)	$\overline{V_{OUT}}$ (V)	V_{OUT} (V)	V_{OUT} (V)
0	000 000 00	0	–1.6	0	–0.8
1	000 000 01	–0.006	–1.594	–0.003	–0.797
.	. . . . .	.	.	.	.
128	100 000 00	–0.8	–0.8	–0.4	–0.4
.	. . . . .	.	.	.	.
254	111 111 10	–1.594	–0.006	–0.797	–0.003
255	111 111 11	–1.6	0	–0.8	0

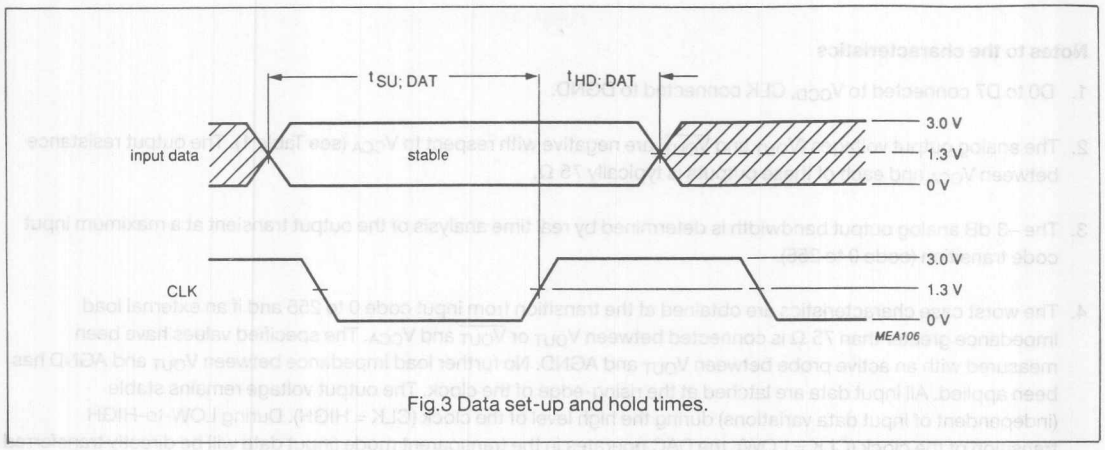


Fig.3 Data set-up and hold times.

Note to Fig.3

The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns, after the first rising-edge of the clock ($t_{SU;\,DAT}$ is negative; −0.3 ns). Data must be held at least 2 ns after the rising-edge ($t_{HD;\,DAT}$ = +2 ns).

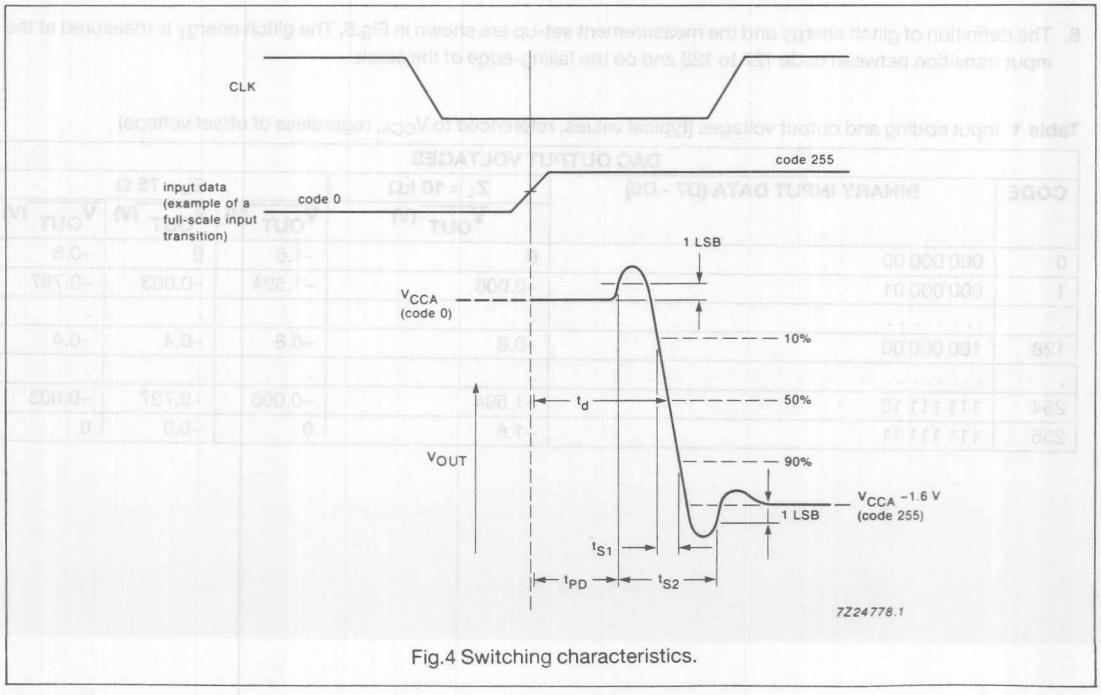


Fig.4 Switching characteristics.

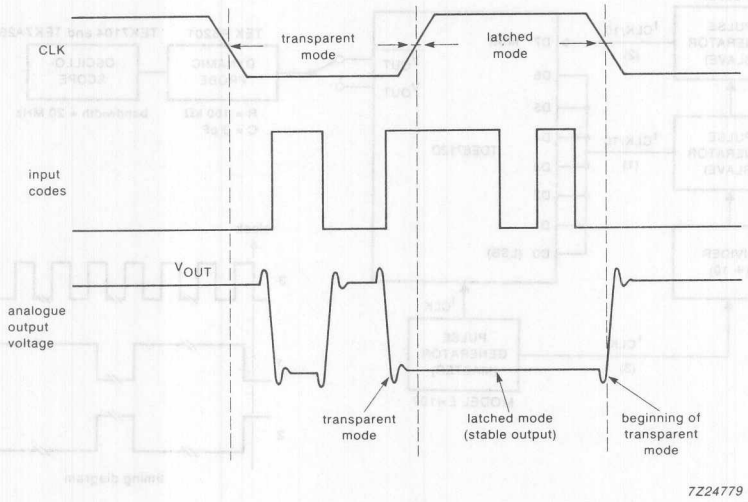


Fig.5 Latched and transparent mode.

Note to Fig.5

During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable, regardless of any changes at the input. A change of input data during the latched mode will be seen on the falling-edge of the clock (beginning of the transparent mode).

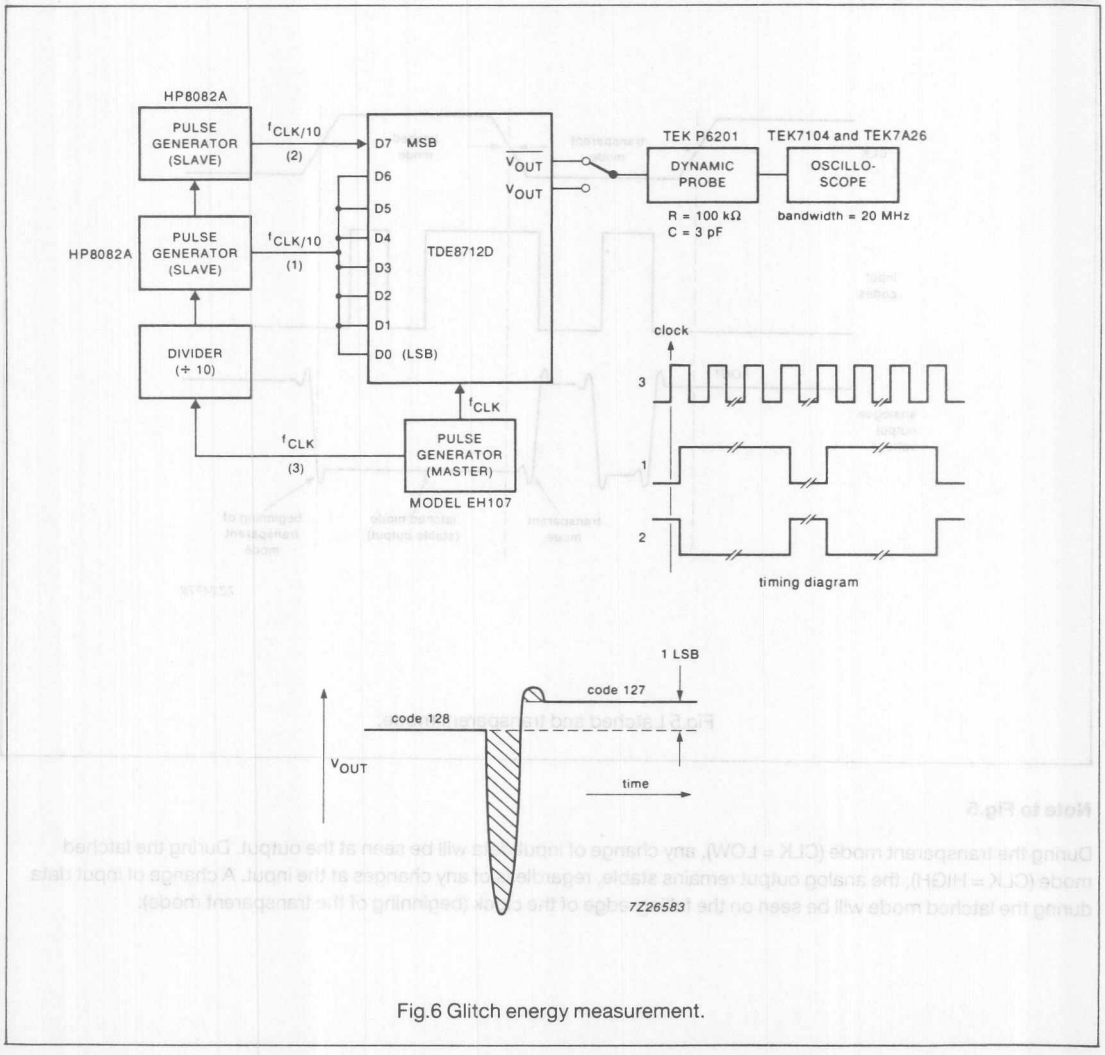


Fig.6 Glitch energy measurement.

Note to Fig.6

The value of the glitch energy is the sum of the shaded area measured in LSB.ns.

INTERNAL PIN CONFIGURATIONS

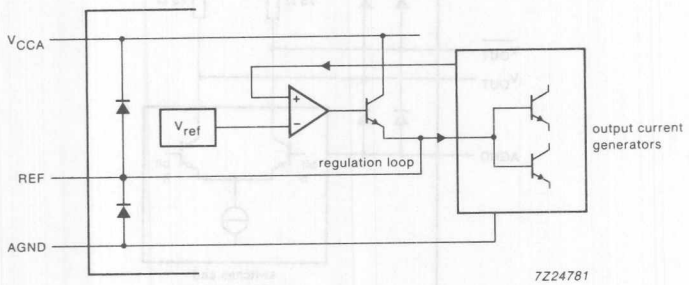


Fig.7 Reference voltage generator decoupling.

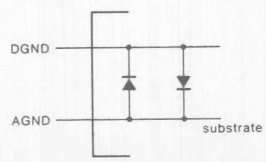


Fig.8 AGND and DGND.

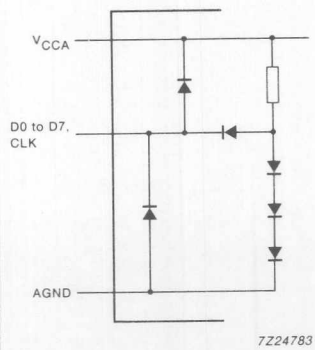


Fig.9 D7 to D0 and CLK.

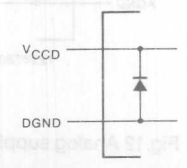


Fig.10 Digital supply.

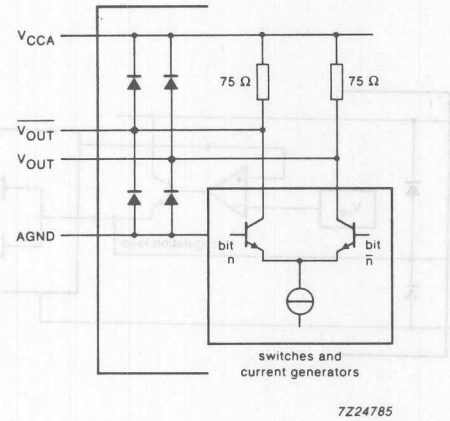


Fig.11 Analog outputs.

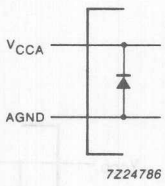


Fig.12 Analog supply.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

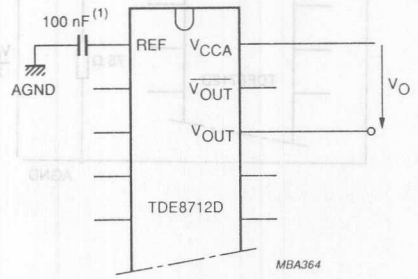


Fig.13 Analog output voltage without external load ($V_O = -\overline{V_{OUT}}$; see Table 1, Z_L = 10 kΩ).

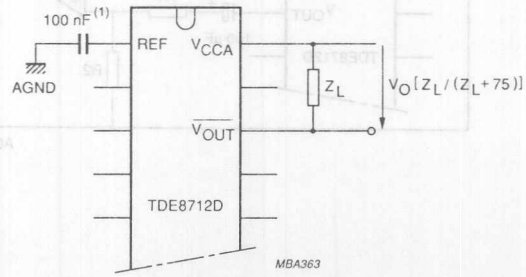


Fig.14 Analog output voltage with external load (external load Z_L = 75 Ω to ∞).

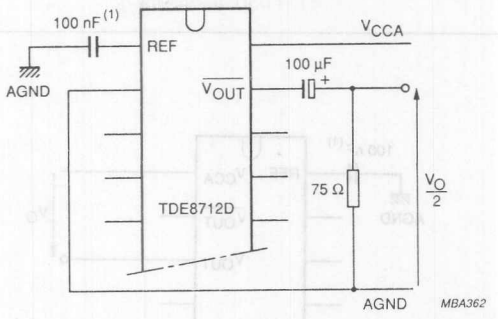


Fig.15 Analog output with AGND as reference.

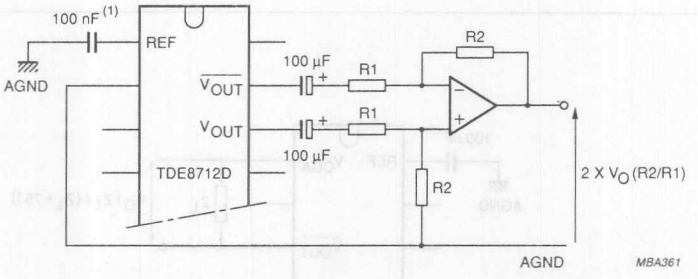


Fig.16 Differential mode (improved supply voltage ripple rejection).

Notes to Figs 13, 14, 15 and 16

1. This is a recommended value for decoupling pin 1.

Section 11
Sample-and-Hold

INDEX

Symbols and definitions for ample-and-hold amplifiers 663

LF198/LF298/ LF398 Sample-and-hold amplifiers 665

NE/SE5537 Sample-and-hold amplifier 670

TDA1535B High-speed single sample-and-hold amplifier 678

Section 11
Sample-and-Hold

INDEX

Symbols and definitions for sample-and-hold amplifiers 663

LF198/LF298/
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NE/SE5537 Sample-and-hold amplifier 679

TDA1535B High-speed single sample-and-hold amplifier 679

Symbols and definitions for sample-and-hold circuits

Acquisition Time (t_{AQ})
The time delay between the 50% (or threshold) point of the hold-to-sample transition of the sample/hold signal and the point at which the output voltage begins to track the input voltage to within a specified error band. By convention the acquisition time is defined for sampling positive (or negative) full-scale input voltage after previously holding a negative (or positive) full-scale output voltage.

Aperture Delay (t_{APD})
The time delay between the 50% (or threshold) point of the hold-to-sample transition of the sample/hold signal and the instant at which the switch is just opening. This latter instant can be defined as the time at which the internal control voltage across the switch element has moved by 10% of its full voltage swing, i.e., the instant at which the switch is 10% open.

Aperture Time (t_{AP})
The time required for the sample-and-hold switch to open. The switch opening time can be defined as the interval between the conditions of 10% open and 90% open and does not include any delays of the sample/hold signal through the switch buffer circuitry.

Aperture Uncertainty (t_{APU})
The range of variation of total aperture delay time (see definition below) due to internal circuit noise of all forms.

Charge Transfer (Q_T)
The amount of charge transferred to the holding capacitor (when switching from the sample-to-hold mode) originating from stray or parasitic capacitance associated with the sample-and-hold switch. Charge transfer is directly related to hold step (see definition below) by the following relationship:

$$V_{HS}(V) = \text{Charge transfer (pC)}/C_H(pF)$$

where V_{HS} is the hold step and C_H is the holding capacitor. It can be seen that increasing C_H will reduce V_{HS}, since the charge transfer is constant for a given circuit.

Input Resistance (R_{IN})
The large-signal input resistance over the specified input voltage range.

Droop Rate (dV_H/dt)
The rate of change of output voltage while the circuit is in the hold mode. It is due to leakage currents to, or from, the holding capacitor and can be positive or negative. It is related to the droop current, I_D (defined below), by the following relationship:

$$dV_H/dt = I_D(pA)/C_H(pF)$$

Droop Current (I_D)
The current flowing *into* the C_H terminal when the circuit is in the hold mode.

Effective Aperture Delay Time (t_{EAPD})
The difference between the propagation time of the analog input voltage to the sample-and-hold switch and the aperture delay (t_{APD}). The value of t_{EAPD} may be positive, negative or zero. For precise timing of the point on the input voltage to be held, the sample-to-hold transition of the sample/hold signal must be advanced by t_{EAPD}.

Feedthrough Attenuation
A measurement of the isolation of the analog switch when the amplifier is in the HOLD mode. A direct function of feedthrough capacitance, it is the ratio of the output signal level to input signal level when in the HOLD mode. Feedthrough Attenuation is specified at a specific frequency and is usually expressed in dB.

Full Power Bandwidth (f_P)
The maximum frequency at which the full-scale output voltage can be achieved without significant distortion. The full power bandwidth is related to the slew rate, SR (defined below) by the following relationship:

$$F_P = SR/2\pi V_{CC}$$

where V_{CC} is the peak value of the input signal; i.e., $V_{IN} = V_{CC}\sin(2\pi Fpt)$.

Gain Error
In a unity gain configuration this is the ratio of the difference between the input and output voltages to the input voltage expressed as a percentage of full scale input range capability.

Hold Mode Feedthrough
A measure of the amount of an input sinusoidal voltage that appears at the output of a sample-and-hold circuit when it is in the hold mode. It is usually expressed as a percentage or as an output RMS voltage for a specified input RMS voltage.

Hold Mode Settling Time (t_{HM})
The time delay between the 50% (or threshold) point of the sample-to-hold transition of the sample/hold signal and the point at which the output settles to within a specified error band of its final value before hold mode droop becomes significant.

Hold Step (V_{HS})
The step in the output voltage caused by charge transfer (defined above).

Input Bias Current (I_{BIAS})
The bias current *into* the input terminal.

Linearity Error (E_L)
The maximum deviation of the output voltage from an ideal straight line drawn between the two output voltages corresponding to the extremes of the input voltage range. It is usually expressed as a percentage of the full-scale input voltage range.

Output Resistance (R_O)
The ratio of the change in output voltage to a change in output load current in either the hold mode or for a fixed input voltage in the sample mode.

Overshoot
The maximum overshoot of the output voltage, in the sample mode, when slewing at its maximum rate over the full-scale output voltage range. It is usually expressed as a percentage of the full-scale output voltage range.

Power Supply Rejection Ratio (PSRR)
The ratio of the change in power supply voltage (over a specified power supply voltage range DPSV) to the corresponding change in zero-scale error, V_{ZS} (defined below); it is expressed in dB where $PSRR(dB) = 20\log(\Delta PSV/\Delta V_{ZS})$.

Slew Rate (SR)
The maximum possible rate of change of the output voltage, in the sample mode, when changing over the full-scale output voltage range.

Total Aperture Delay Time (t_{TAPD})
The sum of the aperture delay and the aperture time.

$$t_{TAPD} = t_{APD} + t_{AP}$$

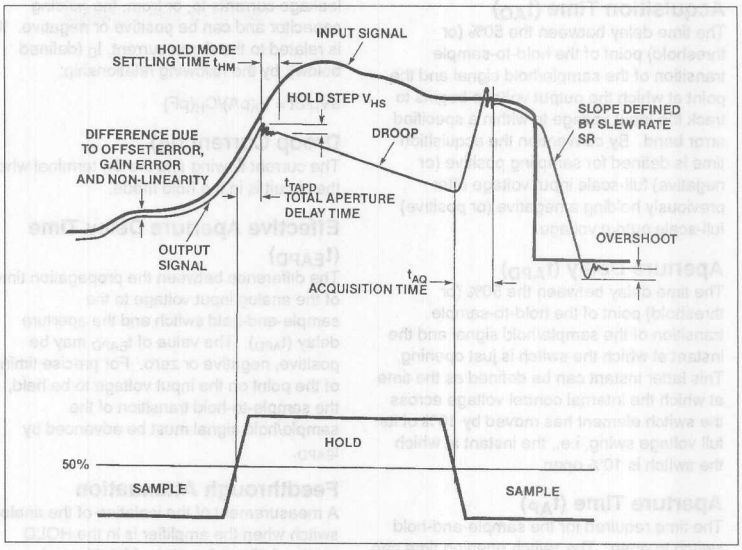
Symbols and definitions for sample-and-hold circuits

Voltage Gain (A_V)

The ratio of the output voltage to the input voltage when operating in the sample mode and over a specified input voltage range.

Zero-Scale Error (V_{ZS}) or Input Offset Voltage (V_{OS})

The difference between the output and input voltages when operating in the sample mode and in a unity gain configuration.



Sample-and-hold amplifiers

LF198/LF298/LF398

DESCRIPTION

The LF198/LF298/LF398 are monolithic sample-and-hold circuits which utilize high-voltage ion-implant JFET technology to obtain ultra-high DC accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, DC gain accuracy is 0.002% typical and acquisition time is as low as 6µs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FETs are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1µF hold capacitor. The JFETs have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feedthrough from input to output in the hold mode even for input signals equal to the supply voltages.

Logic inputs are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS; differential threshold is 1.4V. The LF198/LF298/LF398 will operate from ±5V to ±18V supplies. They are available in 8-pin plastic DIP, 8-pin Cerdip, and 14-pin plastic SO packages.

FEATURES

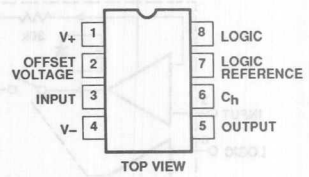
- Operates from ±5V to ±18V supplies
- Less than 10µs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at CH=0.01µF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

APPLICATION

- The LF198/LF298/LF398 are ideally suited for a wide variety of sample-and-hold applications, including data acquisition, analog-to-digital conversion, synchronous demodulation, and automatic test setup

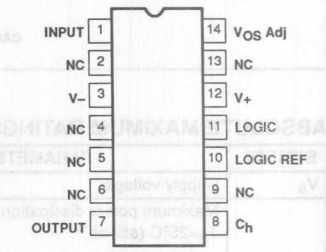
PIN CONFIGURATIONS

FE, N Packages



TOP VIEW

D[1] Package



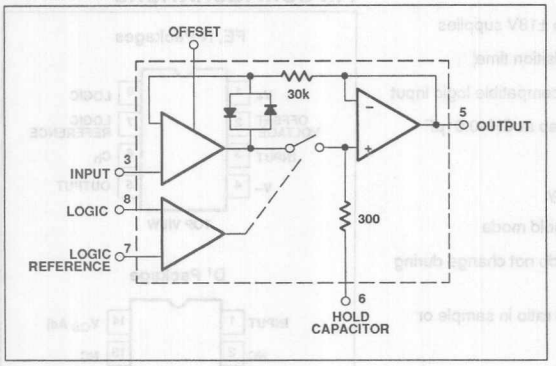
TOP VIEW

NOTE:
1. SO and non-standard pinouts.

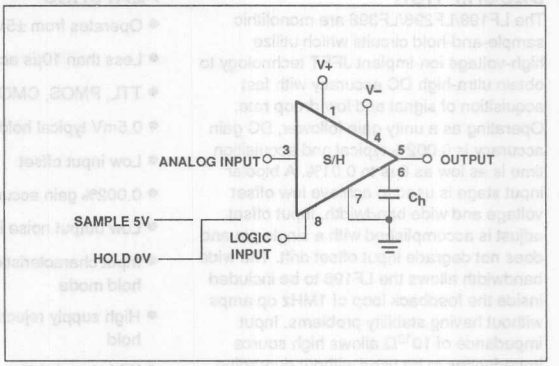
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE
8-Pin Cerdip	-55°C to +125°C	LF198FE
14-Pin Plastic SO Package	0 to +70°C	LF398D
8-Pin Cerdip	0 to +70°C	LF398FE
8-Pin Plastic DIP	0 to +70°C	LF398N
8-Pin Cerdip	-25°C to +85°C	LF298FE

FUNCTIONAL DIAGRAM



TYPICAL APPLICATIONS



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Supply voltage	±18	V
	Maximum power dissipation T_A=25°C (still-air)[3]		
	F package	780	mW
	N package	1160	mW
	D package	1040	mW
T_A	Operating ambient temperature range		
	LF198	-55 to +125	°C
	LF298	-25 to +85	°C
	LF398	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
V_{IN}	Input voltage	Equal to supply voltage	
	Logic-to-logic reference differential voltage[2]	+7, -30	V
	Output short-circuit duration	Indefinite	
	Hold capacitor short-circuit duration	10	sec
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. The maximum junction temperature of the LF398 is 150°C. When operating at elevated ambient temperature, the packages must be derated based on the thermal resistance specified.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
3. Derate above 25°C, at the following rates:
   F package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 8.3mW/°C

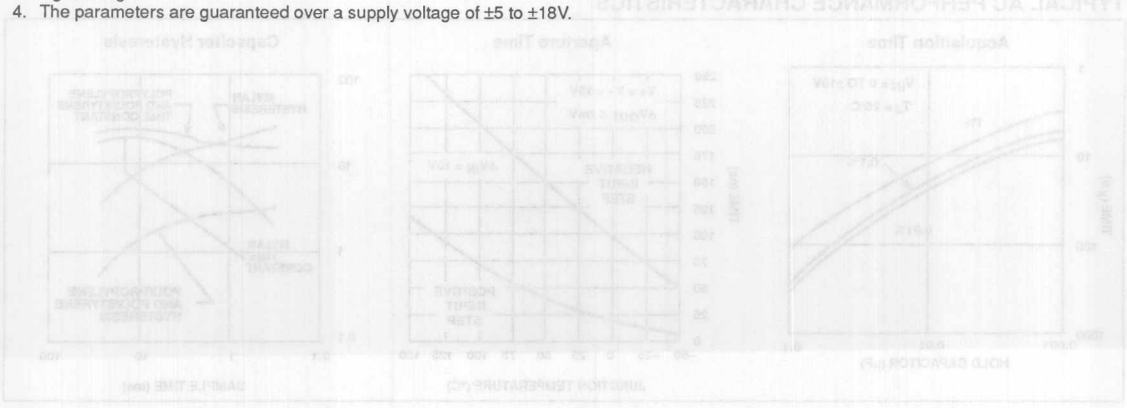
DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following conditions apply: unit is in "sample" mode; $V_S = \pm 15V$; $T_J = 25°C$; -11.5V3 $V_{IN} \leq +11.5V$; $C_H = 0.01\mu F$; and $R_L = 10k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

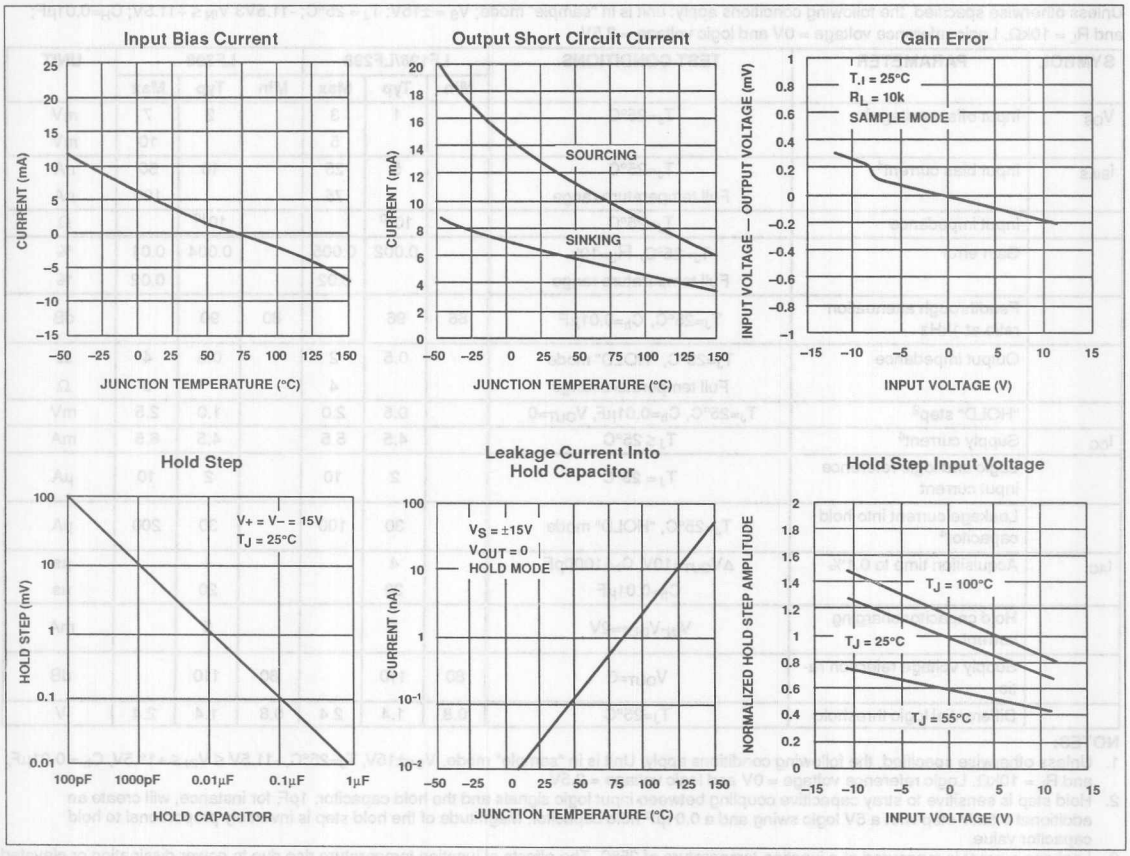
SYMBOL	PARAMETER	TEST CONDITIONS	LF198/LF298			LF398			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[4]	T_J=25°C		1	3		2	7	mV
					5			10	mV
I_{BIAS}	Input bias current[4]	T_J=25°C		5	25		10	50	nA
		Full temperature range			75			100	nA
	Input impedance	T_J=25°C		10^{10}			10^{10}		Ω
	Gain error	T_J=25°C, R_L=10k		0.002	0.005		0.004	0.01	%
		Full temperature range			0.02			0.02	%
	Feedthrough attenuation ratio at 1kHz	T_J=25°C, C_h=0.01μF	86	96		80	90		dB
	Output impedance	T_J=25°C, "HOLD" mode		0.5	2		0.5	4	Ω
		Full temperature range			4			6	Ω
	"HOLD" step[2]	T_J=25°C, C_h=0.01μF, V_{OUT}=0		0.5	2.0		1.0	2.5	mV
I_{CC}	Supply current[4]	$T_J \leq 25°C$		4.5	5.5		4.5	6.5	mA
	Logic and logic reference input current	T_J = 25°C		2	10		2	10	μA
	Leakage current into hold capacitor[4]	T_J=25°C, "HOLD" mode		30	100		30	200	pA
t_{AC}	Acquisition time to 0.1%	ΔV_{OUT}=10V, C_h=1000pF		4			4		μs
		C_h=0.01μF		20			20		μs
	Hold capacitor charging current	V_{IN}-V_{OUT}=2V		5			5		mA
	Supply voltage rejection ratio	V_{OUT}=0	80	110		80	110		dB
	Differential logic threshold	T_J=25°C	0.8	1.4	2.4	0.8	1.4	2.4	V

NOTES:

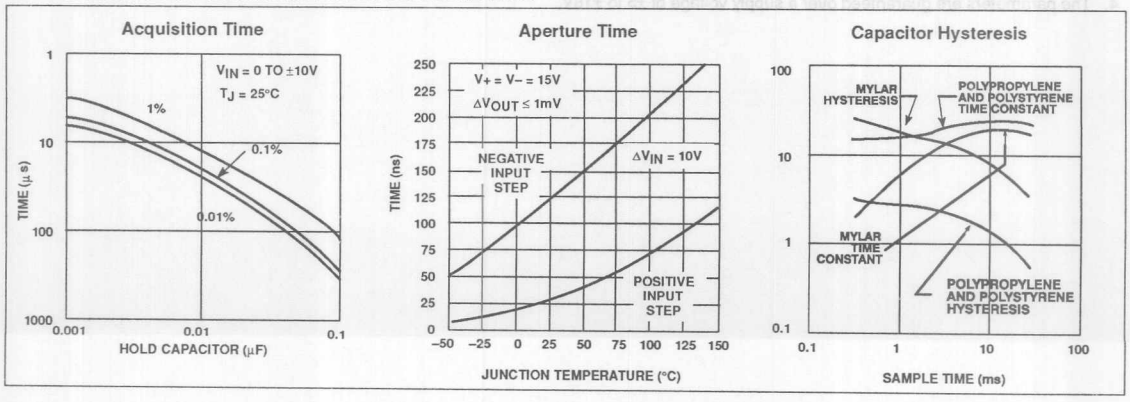
1. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_J = 25°C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.
2. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
3. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
4. The parameters are guaranteed over a supply voltage of ±5 to ±18V.



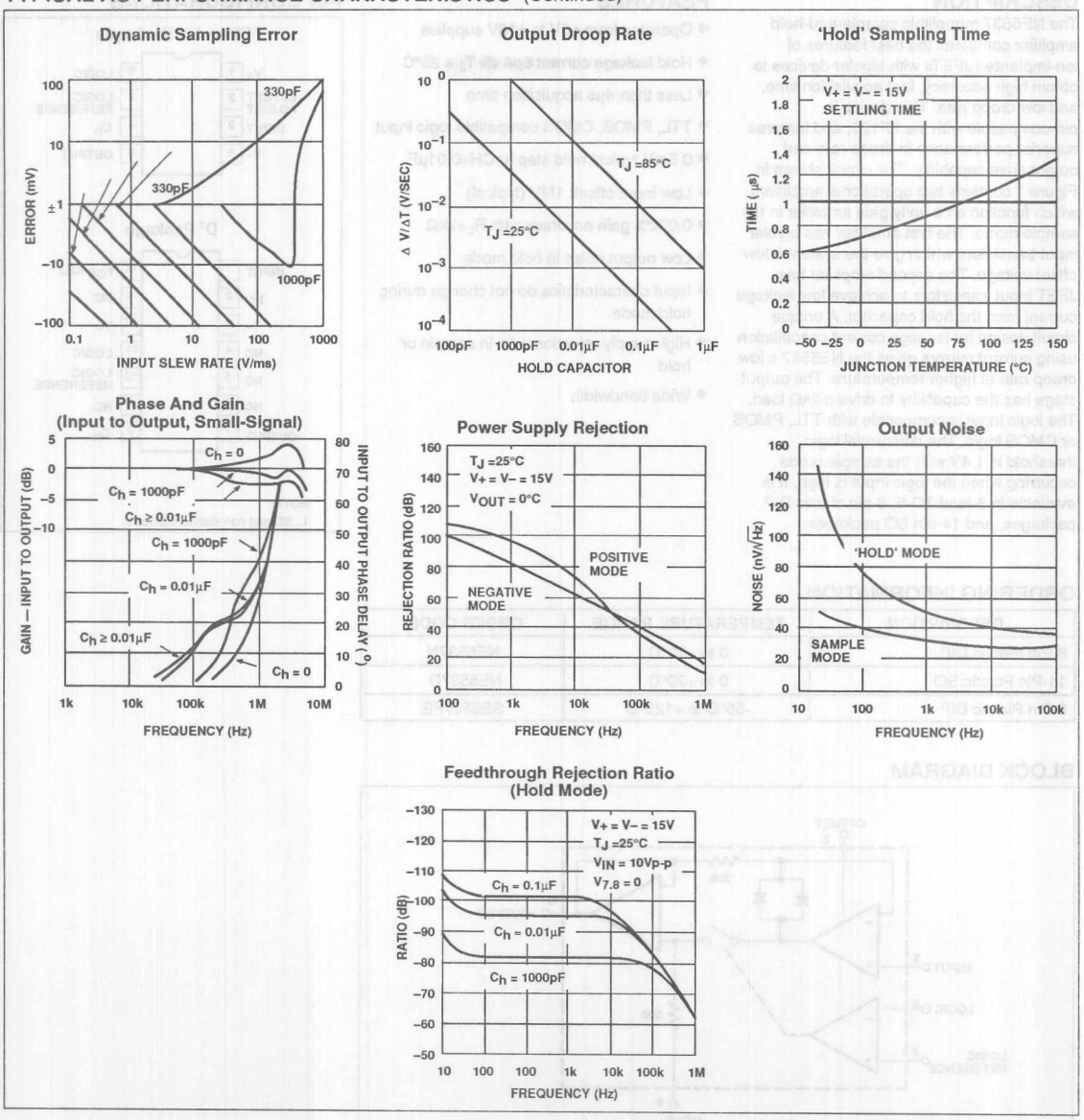
TYPICAL DC PERFORMANCE CHARACTERISTICS



TYPICAL AC PERFORMANCE CHARACTERISTICS



TYPICAL AC PERFORMANCE CHARACTERISTICS (Continued)



Sample-and-hold amplifier — NE/SE5537

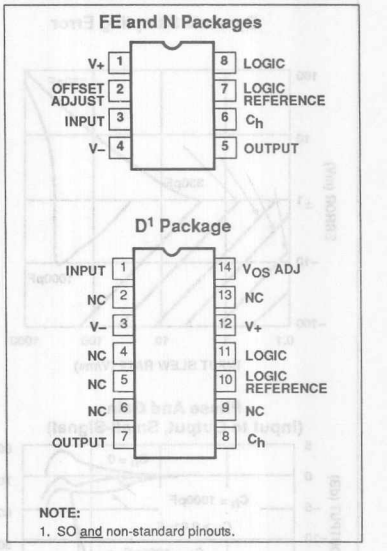
DESCRIPTION

The NE5537 monolithic sample-and-hold amplifier combines the best features of ion-implanted JFETs with bipolar devices to obtain high accuracy, fast acquisition time, and low droop rate. This device is pin-compatible with the LF198, and features superior performance in droop rate and output drive capability. The circuit shown in Figure 1 contains two operational amplifiers which function as a unity gain amplifier in the sample mode. The first amplifier has bipolar input transistors which give the system a low offset voltage. The second amplifier has JFET input transistors to achieve low leakage current from the hold capacitor. A unique circuit design for leakage current cancellation using current mirrors gives the NE5537 a low droop rate at higher temperature. The output stage has the capability to drive a 2kΩ load. The logic input is compatible with TTL, PMOS or CMOS logic. The differential logic threshold is 1.4V with the sample mode occurring when the logic input is high. It is available in 8-lead TO-5, 8-pin plastic DIP packages, and 14-pin SO packages.

FEATURES

- Operates from ±5V to ±18V supplies
- Hold leakage current 6pA @ T_J = 25°C
- Less than 4μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at CH=0.01μF
- Low input offset: 1MV (typical)
- 0.002% gain accuracy with R_L=2kΩ
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

PIN CONFIGURATIONS

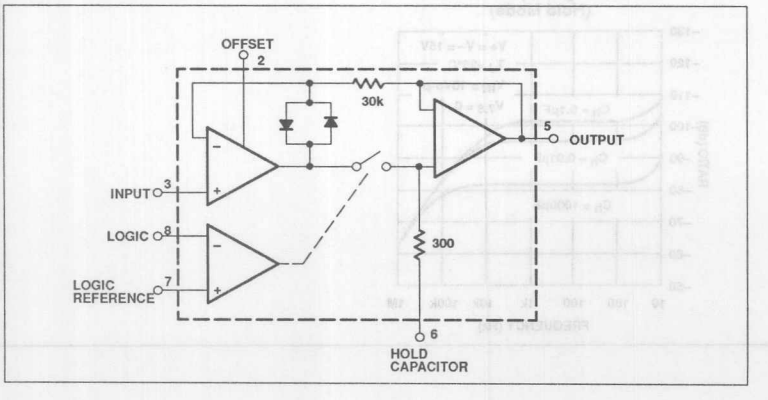


NOTE:
1. SO and non-standard pinouts.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5537N
14-Pin Plastic SO	0 to +70°C	NE5537D
8-Pin Plastic DIP	-55°C to +125°C	SE5537FE

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_S	Voltage supply	±18	V
P_D	Maximum power dissipation T_A=25°C (still-air)[1]		
	N package	1160	mW
	D package	1090	mW
	FE package	780	mW
T_A	Operating ambient temperature range		
	SE5537	-55 to +125	°C
	NE5537	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
V_{IN}	Input voltage	Equal to supply voltage	
	Logic to logic reference differential voltage[2]	+7, -30	V
	Output short circuit duration	Indefinite	
	Hold capacitor short circuit duration	10	s
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 8.3mW/°C
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

DC ELECTRICAL CHARACTERISTICS[1]

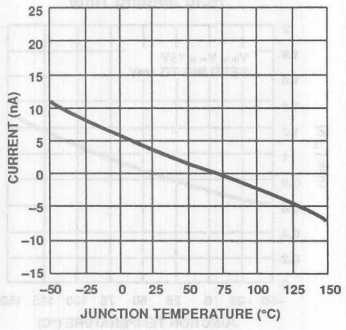
SYMBOL	PARAMETER	TEST CONDITIONS	SE5537			NE5537			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[4]	T_J=25°C		1	3		2	7	mV
		Full temperature range			5			10	mV
I_{BIAS}	Input bias current[4]	T_J=25°C		5	25		10	50	nA
		Full temperature range			75			100	nA
	Input impedance	T_J=25°C		10^{10}			10^{10}		Ω
	Gain error	T_J=25°C		0.002	0.007		0.004	0.01	%
		-10V≤V_{IN}≤10V, R_L=2kΩ -11.5V≤V_{IN}≤11.5V, R_L=10kΩ							
		Full temperature range			0.02			0.02	%
	Feedthrough attenuation ratio at 1kHz	T_J=25°C, C_H=0.01µF	86	96		80	90		dB
	Output impedance	T_J=25°C, "HOLD" mode		0.5	2		0.5	4	Ω
		Full temperature range			4			6	
	"HOLD" Step[2]	T_J=25°C, C_H=0.01µF, V_{OUT}=0		0.5	2.0		1.0	2.5	mV
I_{CC}	Supply current[4]	T_J=25°C		4.5	6.5		4.5	7.5	mA
	Logic and logic reference input current	T_J=25°C		2	10		2	10	µA
	Leakage current into hold capacitor[4]	T_J=25°C "hold" mode[3]		6	50		6	100	pA
	Acquisition time to 0.1%	V_{OUT}=10V, C_H=1000pF		4			4		µs
		C_H=0.01µF		20			20		µs
	Hold capacitor charging current	V_{IN}-V_{OUT}=2V		5			5		mA
SVRR	Supply voltage rejection ratio	V_{OUT}=0V	80	110		80	110		dB
	Differential logic threshold	T_J=25°C	0.8	1.4	2.4	0.8	1.4	2.4	V

NOTES:

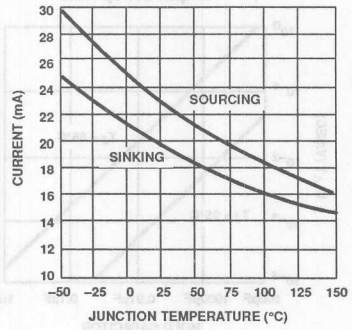
1. Unless otherwise specified, the following conditions apply: Unit is in "sample" mode. V_S=±15V, T_J=25°C, -11.5V≤V_{IN}≤11.5V, C_H=0.01µF, and R_L=2kΩ. Logic reference voltage=0V and logic voltage=2.5V.
2. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01F hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
3. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
4. These parameters guaranteed over a supply voltage range of ±5 to ±18V.

TYPICAL PERFORMANCE CHARACTERISTICS

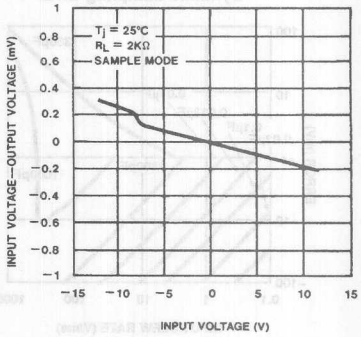
Input Bias Current



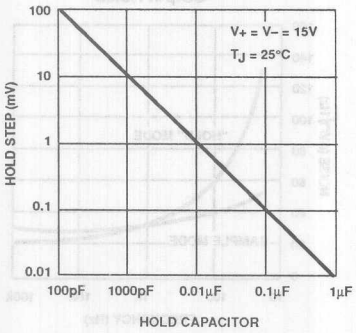
Output Short-Circuit Current



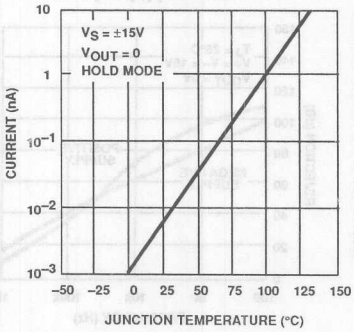
Gain Error



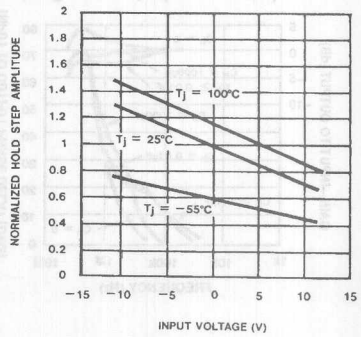
Hold Step



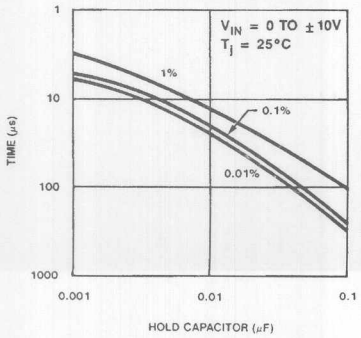
Leakage Current Into Hold Capacitor



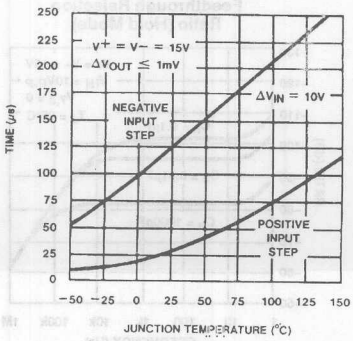
Hold Step vs Input Voltage



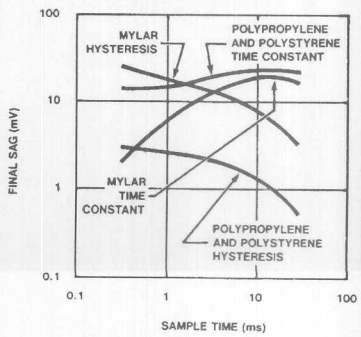
Acquisition Time



Aperture Time

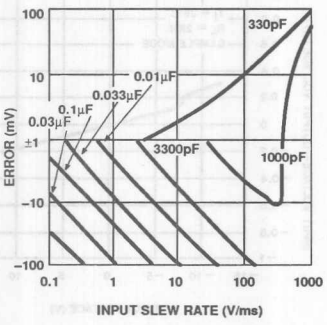


Capacitor Hystersis

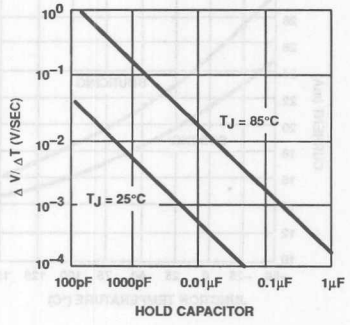


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

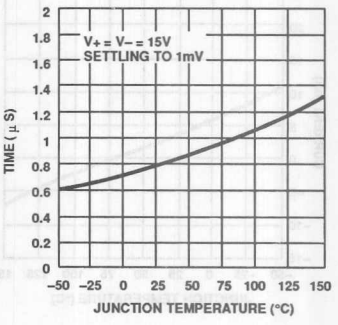
Dynamic Sampling Error



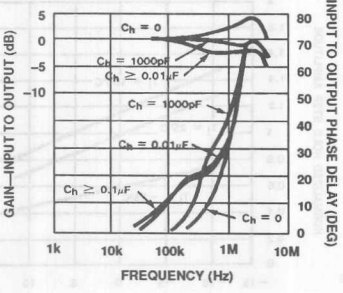
Output Droop Rate



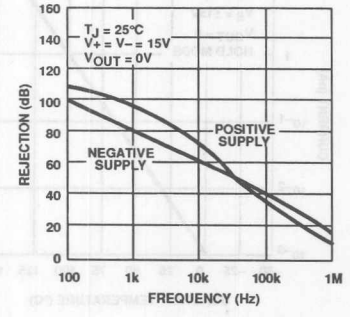
Hold Settling Time



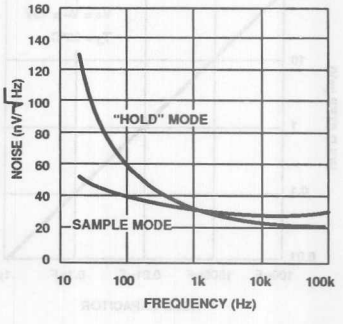
Phase and Gain
(Input-to-Output, Small-Signal)



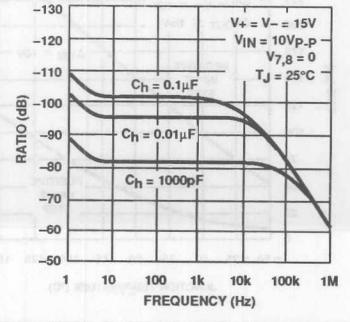
Power Supply Rejection



Output Noise



Feedthrough Rejection
Ratio (Hold Mode)



Sample-and-hold amplifier NE/SE5537

SAMPLE-AND-HOLD

For many years designers have used the sample-and-hold (or track-and-hold) to operate on analog information in a time frame which is expedient.

By sampling a segment of the information and holding it until the proper timing for converting to some form of control signal or readout, the designer maintains certain freedom in performing predetermined manipulative functions. Therefore, the sample-and-hold can be defined as a "selective analog memory cell".

The memory is volatile and will also decay with time.

When using the sample-and-hold method for evaluating signal information, the designer is given the added feature of eliminating outside noise elements. With the analog-to-digital converter products available today, the "DC memory" of the sample-and-hold can be easily converted to digital format and further incorporated into microprocessor-based systems.

Parametric evaluation of the sample-and-hold will be discussed in the following paragraphs.

DEFINITION OF TERMS

Acquisition Time —
The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Delay Time —
The time elapsed from the hold command to the opening of the switch. *H4Aperture Jitter| Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

Aperture Time —
The delay required between "HOLD" command and an input analog transition, so that the transition does not affect the held output.

Bandwidth —
The frequency at which the gain is down 3dB from its DC value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

Dynamic Sampling Error —
The error introduced into the hold output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Effective Aperture Delay —
The time difference between the hold command and the time at which the input signal is at the held voltage.

Figure of Merit —
The ratio of the available charging current during sample mode to the leakage current during hold mode.

Gain Error —
The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Mode Droop —
The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

Hold Mode Feedthrough —
The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

Hold Settling Time —
The time required for the output to settle within 1mV of final value after the "HOLD" logic command.

Hold Step —
The voltage step at the output of the sample-and-hold when switching from sample mode to hold mode with a steady (DC) analog input voltage. Logic swing is 5V.

Sample-to-Hold Offset Error —
The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

Slew Rate —
The fastest rate at which the sample-and-hold output can change (specified in V/μs).

Threshold Level —
That level which causes the switch control to change state.

BASIC BLOCK DIAGRAM

The basic circuit concept of the sample-and-hold circuit incorporates the use of two (2) operational amplifiers and a switch control mechanism (which determines sample, hold or track conditions).

The block diagram of the NE5537 is a closed loop, non-inverting unity gain sample-and-hold system. The input buffer amplifier supplies the current necessary to charge the hold capacitor, while the output buffer amplifier closes the loop so that the output voltage is identical to the input voltage (with consideration for input offset voltage, offset current, and temperature variations which are common to all sample-and-hold circuits, be they monolithic, hybrid or modular).

When the sampling switch is open (in the hold mode), the clamping diodes close the loop around the input amplifier to keep it from being overdriven into saturation.

The switch control is driven by external logic levels via a timing sequence remote from the sample-and-hold device (See Figure 1). The switch control has a floating reference (Pin 7), referred to as the logic reference which makes the sample-and-hold device compatible to several types of external logic signals (TTL, PMOS, and CMOS). The switching device operates at a threshold level of 1.4V.

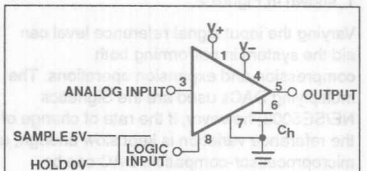


Figure 1. Typical Connection

The switch mechanism is on (sampling an information stream) when the logic level is high (Pin 8 is 1.4V higher than Pin 7) and presents a load of 5μA to the input logic signal. The analog sampled signal is amplified, stored (in the external holding capacitor), and buffered. At the end of the sampling period, the internal switch mechanism turns off (switch opens) and the "stored analog memory" information on the external capacitor (Pin 6) is loaded down by an operational amplifier connected in the unity gain non-inverting configuration. This input impedance of this amplifier is effectively:

$$R = R_{IN}(A_{OL}) / (1 + 1/A)$$

where R = Effective input impedance
R_{IN} = Open-loop input impedance
A_{OL} = Open-loop gain
A = AC loop gain

Therefore, the higher the open-loop gain of the second operational amplifier, the larger the effective loading on the capacitor. The larger the load, the lower the "leakage" current and the better the droop characteristics.

In actuality, the amplifiers are designed with special leakage current cancellation circuits along with FET input devices. The leakage current cancellation circuits give better high temperature operation. (Remember that the FET amplifiers double in required bias current for every 10 degree increase in junction temperature.)

Sampling time for the NE5537 is less than 10µs (measured to 0.1% of input signal). Leakage current is 6pA at a rate output load of 2kΩ.

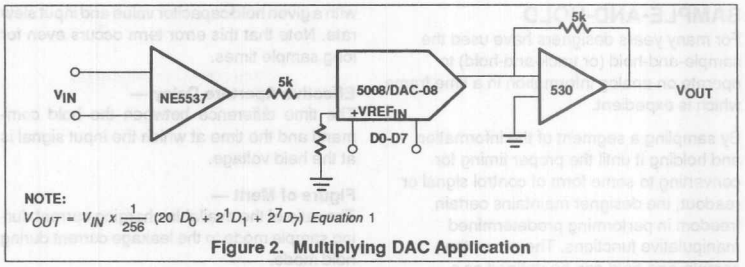


Figure 2. Multiplying DAC Application

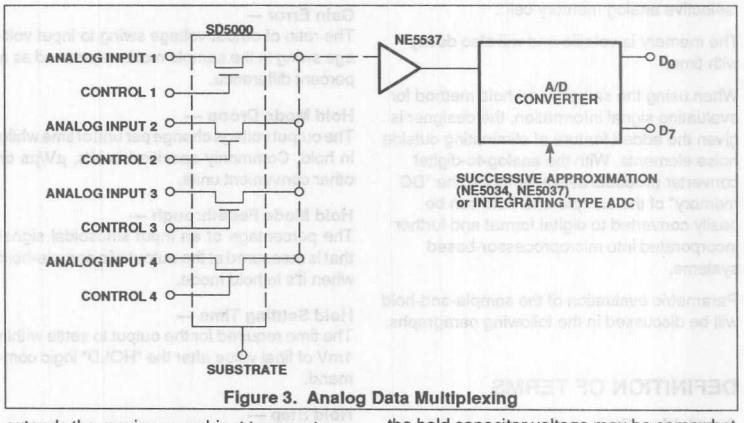


Figure 3. Analog Data Multiplexing

BASIC APPLICATIONS

Multiplying DAC

As depicted in the block diagram of Figure 2, the sample-and-hold circuit is used to supply a "variable" reference to the digital-to-analog converter. As the input reference varies, the output will change in accordance with Equation 1, shown in Figure 2.

Varying the input signal reference level can aid the system in performing both compression and expansion operations. The multiplying DACs used are the Signetics NE/SE5008; however, if the rate of change of the reference variation is kept slow enough, a microprocessor-compatible DAC can be incorporated, such as the NE5018 or the NE5020.

DATA ACQUISITION SYSTEMS

As mentioned earlier, the designer may wish to operate on several different segments of an "analog" signal; however, he is limited by the fact that only one analog-to-digital converter channel is available to him. Figure 3 shows the means by which a multiplexing system may be accomplished.

APPLICATION HINTS

Hold Capacitor

A significant source of error in an accurate sample-and-hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back in the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with >1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. The hysteresis relaxation time constant in polystyrene, for instance, is 10-50ms. If A-to-D conversion can be made within 1ms, hysteresis error will be reduced by a factor of ten.

DC ZEROING

zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1kw potentiometer which has one end tied to V+ and the other end tied through a resistor to ground. The resistor should be selected to give κ0.6mA through the 1kw potentiometer.

Sampling Dynamic Signals

Sampling errors due to moving (changing) input signals are of significant concern to designers employing sample-and-hold circuits. There exist finite phase delays through the sample-and-hold circuit causing an input-output phase of differential for moving signals. In addition, the series protection resistor (300Ω to Pin 6 of the NE5537) will add an RC time constant, over and above the slew rate limitation of the input buffer/current drive amplifier. This means that at the moment the "HOLD" command arrives, the hold capacitor voltage may be somewhat different from the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 V_{P-P} at 10kHz. Maximum dV/dt is 0.6V/µs. With no analog phase delay and 100ns logic delay, one could expect up to (0.1µs) (0.6V/µs) =60mV error if the "HOLD" signal arrived near maximum dV/dt of the input. A positive-going input would give a ±60mV error. Now assume a 1MHz (3dB) bandwidth for the overall analog loop. This generates a phase delay of 160ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16µs) (0.6V/µs)=-96mV (analog) for a total of -36mV. To add to the confusion, analog delay is proportional to hold capacitor value, while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labeled "Aperture Time" has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "HOLD" command. This

curve is based on a 1mV error fed into the output.

A second curve, "Hold Settling Time," indicates the time required for the output to settle to 1mV after the "HOLD" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

Logic signals also couple to the hold capacitor. This hold capacitor should be guarded by a PC card trace connected to the sample-and-hold output. This will also minimize board leakage.

SPECIAL NOTES

1. Not all definitions herein defined are measured parametrically for the NE5537, but are legitimate terms used in sample-and-hold systems.
2. Reference should be made to Design Engineering, Volumes 23 (Nov. 8, 1978), 25 (Dec. 6, 1978) and 26 (Dec. 20, 1978) for articles written by Eugene Zuch of Datel Systems, Inc., for a further discussion of sample-and-hold circuits.
3. Reference also made to National Semiconductor Corporation's Special Functions Data Book (1976).

High-speed single sample-and-hold amplifier

TDA1535B

GENERAL DESCRIPTION

The TDA1535B is a high-speed sample-and-hold amplifier with a total harmonic distortion of 0.001%, and a very high signal-to-noise ratio.

The excellent performance of the circuit makes it suitable for data acquisition systems with resolution up to 16 bits. The control input is TTL compatible.

FEATURES

- High-speed: fast acquisition, hold-mode settling and aperture time
- Small sample-to-hold offset step, low droop rate
- Low noise: low total harmonic distortion and high signal-to-noise ratio
- Control circuit with TTL input.

FUNCTIONAL DESCRIPTION

The operation of the circuit will be explained using the application diagram (Fig.3). The circuit is a single Sample-and-Hold circuit. The several parts of the diagram will be described in the next sections.

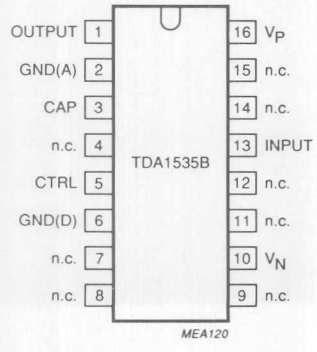


Fig.1 Pinning diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage	4.5	5.0	5.5	V
V_N	negative supply voltage	−5.5	−5.0	−4.5	V
THD	total harmonic distortion	–	−100	–	dB
		–	0.001	–	%
S/N	signal-to-noise ratio	–	110	–	dB
t_{ac}	acquisition time to 0.001% (8 V step)	–	2	–	µs
t_{av}	aperture uncertainty	–	0.1	–	ns
B	small signal bandwidth	–	2	–	MHz
V_{SHO}	sample-to-hold offset step	–	2	–	mV
dV/dt	droop rate	–	40	–	mV/s
t_{se}	hold-mode settling time	–	1	–	µs
P_{tot}	total power dissipation	–	225	–	mW
T_{amb}	operating ambient temperature range	−30	–	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1535B	16	DIL	plastic	SOT38

PINNING

SYMBOL	PIN	DESCRIPTION
OUTPUT	1	output
GND(A)	2	analog ground
CAP	3	S/H capacitor
n.c.	4	not connected
CTRL	5	S/H control
GND(D)	6	digital ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
V_N	10	negative supply voltage
n.c.	11	not connected
n.c.	12	not connected
INPUT	13	input
n.c.	14	not connected
n.c.	15	not connected
V_p	16	positive supply voltage

High-speed single sample-and-hold amplifier

TDA1535B

Supply block

The circuit must be supplied by a dual supply voltage. Nominally the supply voltages are plus and minus 5 V. This supply voltage is needed for a rated output voltage of 8 Vtt, but the circuit will also operate at lower supply voltages. Furthermore separate 'grounds' for analog and digital signals are used. The supply circuit consists of a current source circuit which contains separate sources for the voltage follower, and the hold amplifier to prevent feedthrough in the hold condition. The supply acts as a current source, so the current consumption is almost independent of the supply voltage resulting in a good supply ripple rejection.

Voltage follower amplifier

The voltage follower amplifier is an operational amplifier in voltage follower configuration. It contains two PMOS input stages controlled by the S/H switch, one input stage for the track mode, the other for the hold mode. The input stage that is used in the hold mode has it's + input connected to the analog ground forcing the output to analog ground too. In this way, feedthrough of the input signal is prevented in the hold mode.

Hold switch

The hold switch is a large NMOS transistor with an on-resistance of 50 Ω. In order to reduce the charge transfer of the digital signal into the analog path, two short-circuited NMOS transistors, with the inverse, digital signal on their gate, are added on both sides of the switching transistor.

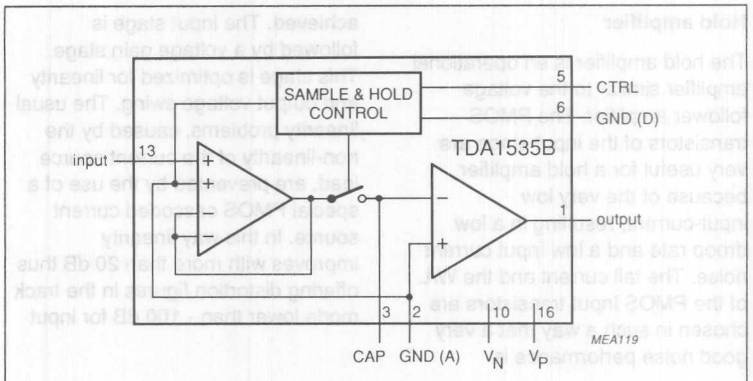


Fig.2 Block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage		–	6	V
V_N	negative supply voltage		–6	–	V
T_{stg}	storage temperature range		–55	+150	°C
T_{amb}	operating ambient temperature range		–30	+85	°C
V_{es}	electrostatic handling	see note 1	–2000	+2000	V

Note

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient	75	K/W

High-speed single sample-and-hold amplifier

TDA1535B

Hold amplifier

The hold amplifier is an operational amplifier similar to the voltage follower amplifier. The PMOS transistors of the input stage are very useful for a hold amplifier because of the very low input-current, resulting in a low droop rate and a low input current noise. The tail current and the W/L of the PMOS input transistors are chosen in such a way that a very good noise performance is achieved. The input stage is followed by a voltage gain stage. This stage is optimized for linearity and output voltage swing. The usual linearity problems, caused by the non-linearity of the current source load, are prevented by the use of a special PMOS cascoded current source. In this way linearity improves with more than 20 dB thus offering distortion figures in the track mode lower than - 100 dB for input frequencies up to 20 kHz and output voltages up to 8 Vtt.

Sample-and-hold control

The sample-and-hold control input is a TTL compatible input. The signal on this input controls the switches mentioned in the above sections in the correct timing order. The supply is taken from the 'V_p' pin via an on-chip separate supply line.

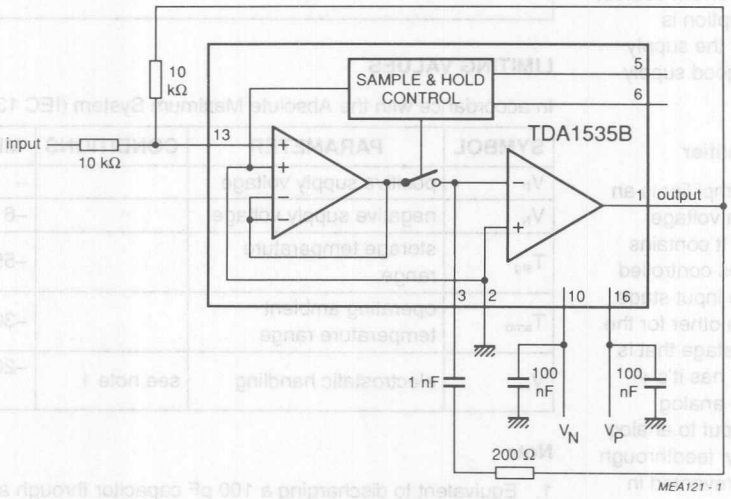


Fig.3 Test and application diagram.

CHARACTERISTICS

V_P = +5 V; T_{amb} = +25 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage		4.5	5.0	5.5	V
V_N	negative supply voltage		−5.5	−5.0	−4.5	V
I_P	positive supply current		–	22	–	mA
I_N	negative supply current		–	−23	–	mA
P_{tot}	total power dissipation		–	225	–	mW
Input/Output						
A_v	gain	note 2	–	−1	–	V/V
V_i	input voltage (RMS value)		–	–	2.82	V
Sample mode						
THD	total harmonic distortion	notes 1,2,3	–	−100	–	dB
SNR	S/N ratio	notes 1,2,3	–	110	–	dB
B	small signal band width		–	2	–	MHz
Sample/hold mode						
t_{ad}	aperture delay time	see Fig.4	–	100	–	ns
t_{av}	aperture uncertainly (RMS)	see Fig.4	0	0.1	0.2	ns
V_{SHO}	sample-to-hold (pedestal)	see Fig.4	–	2	–	mV
dV/dt	offset step droop rate	see Fig.4	–	40	–	mV/s
t_{ac}	acquisition time to 0.001%	see Fig.4	–	2	–	µs
t_{se}	hold-mode settling time	see Fig.4	–	1	–	µs
THDF	total harmonic distortion functional	notes 1,4	–	−100	−96	dB
Supply voltage ripple rejection						
SVRR		note 5	–	80	–	dB
SVRR		note 5	55	80	–	dB
Digital inputs						
V_{IH}	digital input voltage, hold mode (logic 1)		2	–	V_p	V
I_{IH}	digital input current, sample mode	V_{IH} = 2.4 V	–	–	20	µA
V_{IL}	digital input voltage, sample mode (logic 0)		0	–	0.8	V
I_{IL}	digital input current, hold mode	V_{IL} = 0.4 V	−400	–	–	µA

Notes

1. Over audio band (20 Hz to 20 kHz).
2. In sampling mode.
3. At maximum input signal.
4. Distortion of sampled signal at a sample frequency of 50 kHz.
5. The ripple rejection is measured at the output of the hold amplifier; amplitude = 0.5 Vtt. f = 100 Hz to 10 kHz.

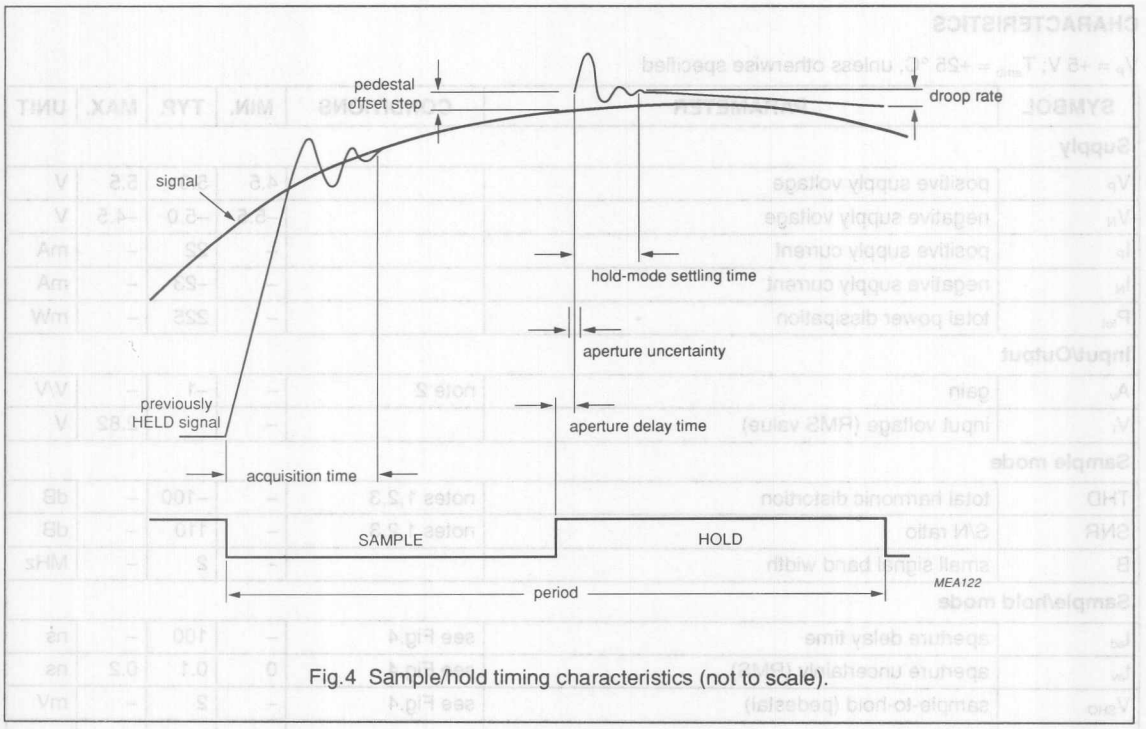


Fig.4 Sample/hold timing characteristics (not to scale).

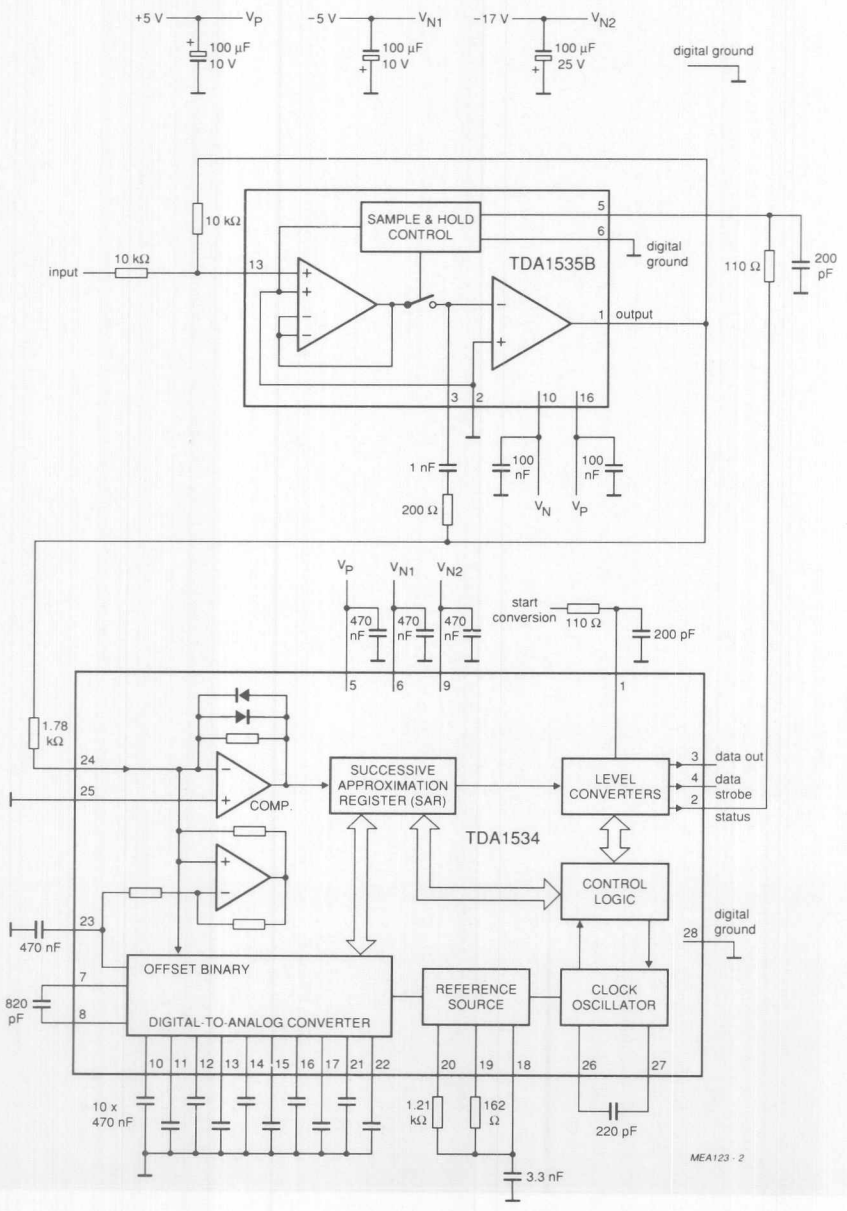


Fig.5 Application diagram of TDA1535B in combination with TDA1534.

Fig.5 Application diagram of TDA1535B in combination with TDA1534.

Section 12
Position Measurement

INDEX

NE/SA/SE5521 LVDT signal conditioner 687

Section 12
Position Measurement

INDEX

NE/SA/SE5521 LVDT signal conditioner 687

LVDT signal conditioner

NE/SA/SE5521

DESCRIPTION

The NE/SA/SE5521 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LVDTs) and Rotary Variable Differential Transformers (RVDTs). The chip includes a low distortion, amplitude-stable sine wave oscillator with programmable frequency to drive the primary of the LVDT/RVDT, a synchronous demodulator to convert the LVDT/RVDT output amplitude and phase to position information, and an output ampliifier to provide amplification and filtering of the demodulated signal.

FEATURES

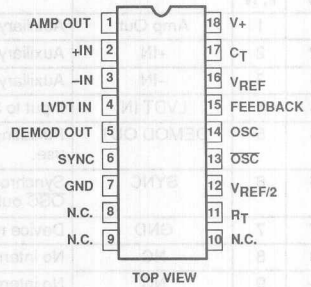
- Low distortion
- Single supply 5V to 20V, or dual supply ±2.5V to ±10V
- Oscillator frequency 1kHz to 20kHz
- Capable of ratiometric operation
- Low power consumption (182mV typ)

APPLICATIONS

- LVDT signal conditioning
- RVDT signal conditioning
- LPDT signal conditioning
- Bridge circuits

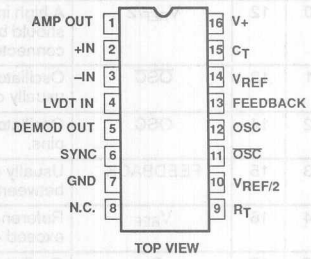
PIN CONFIGURATIONS

F, N Packages



TOP VIEW

D[1] Package



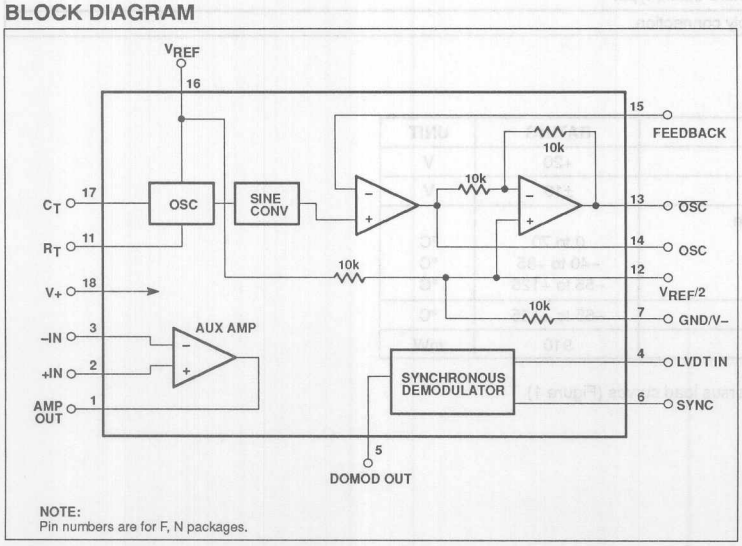
TOP VIEW

NOTE:
1. SOL — released in large SO package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Plastic DIP	0 to +70°C	NE5521N
16-Pin SOL Package	0 to +70°C	NE5521D
18-Pin Plastic DIP	–40 to +85°C	SA5521N
18-Pin Cerdip	–55 to +125°C	SE5521F
16-Pin Cerdip	–40 to +85°C	SA5521D

BLOCK DIAGRAM



NOTE:
Pin numbers are for F, N packages.

PIN DEFINITIONS FOR D, F AND N PACKAGES

PIN NO.		SYMBOL	DEFINITION
D	F, N		
1	1	Amp Out	Auxiliary Amplifier Out.
2	2	+IN	Auxiliary Amplifier non-inverting input.
3	3	–IN	Auxiliary Amplifier inverting input.
4	4	LVDT IN	Input to Synchronous Demodulator from the LVDT/RVDT secondary.
5	5	DEMOD OUT	Pulsating DC output from the Synchronous Demodulator output. This voltage should be filtered before use.
6	6	SYNC	Synchronizing input for the Synchronizing Demodulator. This input should be connected to the OSC or $\overline{OSC}$ output. Sync is referenced to $V_{REF}/2$.
7	7	GND	Device return. Should be connected to system ground or to the negative supply.
8	8	NC	No internal connection.
--	9	NC	No internal connection.
--	10	NC	No internal connection.
9	11	R_T	A temperature stable 18kΩ resistor should be connected between this pin and Pin 7.
10	12	$V_{REF}/2$	A high impedance source of one half the potential applied to V_{REF}. The LVDT/RVDT secondary return should be to this point. A bypass capacitor with low impedance at the oscillator frequency should also be connected between this pin and ground.
11	13	$\overline{OSC}$	Oscillator sine wave output that is 180° out of phase with the OSC signal. The LVDT/RVDT primary is usually connected between OSC and $\overline{OSC}$ pins.
12	14	OSC	Oscillator sine wave output. The LVDT/RVDT primaries are usually connected between OSC and $\overline{OSC}$ pins.
13	15	FEEDBACK	Usually connected to the OSC output for unity gain, a resistor between this pin and OSC, and one between this pin and ground can provide for a change in the oscillator output pin amplitudes.
14	16	V_{REF}	Reference voltage input for the oscillator and sine converter. This voltage MUST be stable and must not exceed +V supply voltage.
15	17	C_T	Oscillator frequency-determining capacitor. The capacitor connected between this pin and ground should be a temperature-stable type.
16	18	+V	Positive supply connection.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+20	V
	Split supply voltage	±10	V
T_A	Operating temperature range NE5521 SA5521 SE5521	 0 to 70 –40 to +85 –55 to +125	 °C °C °C
T_{STG}	Storage temperature range	–65 to +125	°C
P_D	Power dissipation[1]	910	mW

NOTES:
1. For derating, see typical power dissipation versus load curves (Figure 1).

DC ELECTRICAL CHARACTERISTICS

$V+ = V_{REF} = 10V$, $T_A = 0$ to 70°C for NE5521, $T_A = -55$ to +125°C for SE5521, $T_A = -40$ to 85°C for SA5521, Frequency = 1kHz, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5521			SA/SE5521			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply current			12.9	20		12.9	18	mA
I_{REF}	Reference current			5.3	8		5.3	8	mA
V_{REF}	Reference voltage range		5		V+	5		V+	V
P_D	Power dissipation			182	280		182	260	mW
Oscillator Section									
	Oscillator output	$R_L = 10k\Omega$	$\frac{V_{REF}}{8.8}$				$\frac{V_{REF}}{8.8}$		V_{RMS}
THD	Sine wave distortion	No load		1.5			1.5		%
	Initial amplitude error	$T_A = 25°C$		0.4	±3		0.4	±3	%
	Tempco of amplitude			0.005	0.01		0.005	0.01	%/°C
	Init. accuracy of oscillator freq.	$T_A = 25°C$		±0.9	±5		±0.9	±5	%
	Temperature coeff. of frequency[1]			0.05			0.05		%/°C
	Voltage coeff. of frequency			2.5			3.3		%/V(V_{REF})
	Min OSC ($\overline{OSC}$) Load[2]		300	170		300	170		Ω
Demodulator Section									
ϵ_r	Linearity error	$5V_{P-P}$ input		±0.05	±0.1		±0.05	±0.1	%FS
	Maximum demodulator input			$\frac{V_{REF}}{2}$			$\frac{V_{REF}}{2}$		V_{P-P}
V_{OS}	Demodulator offset voltage			±1.4	±5		±1.4	±5	mV
TCV_{OS}	Demodulator offset voltage drift			5	25		5	25	µV/°C
I_{BIAS}	Demodulator input current		–600	–234		–500	–234		nA
	$V_{R/2}$ accuracy			±0.1	±1		±0.1	±1	%
Auxiliary Output Amplifier									
V_{OS}	Input offset voltage			±0.5	±5		±0.5	±5	mV
I_{BIAS}	Input bias current		–600	–210		–500	–210		nA
I_{OS}	Input offset current			10	50		10	50	nA
A_V	Gain		100	385		100	385		V/mV
SR	Slew rate			1.3			1.3		V/µs
GBW	Unity gain bandwidth product	$A_V = 1$		1.6			1.6		MHz
	Output voltage swing	$R_L = 10k\Omega$	7	8.2		7	8.2		V
	Output short circuit current to ground or to V_{CC}	$T_A = 25°C$		42	100		42	100	mA

NOTES:

1. This is temperature coefficient of frequency for the device only. It is assumed that C_T and R_T are fixed in value and C_T leakage is fixed over the operating temperature range.
2. Minimum load impedance for which distortion is guaranteed to be less than 5%.

DEFINITION OF TERMS

Oscillator Output	RMS value of the AC voltage at the oscillator output pin. This output is referenced to $V_{REF/2}$ and is a function of V_{REF}.
Sine Wave Distortion	The Total Harmonic Distortion (THD) of the oscillator output with no load. This is not a critical specification in LVDT/RVDT systems. This figure could be 15% or more iwthout affecting system performance.
Initial Amplitude Error	A measure of the interchangeability of NE/SA/SE5521 parts, not a characteristic of any one part. It is the degree to which the oscillator output of a number of NE/SA/SE5521 samples will vary from the median of that sample.
Initial Accuracy of Oscillator Frequency	Another measure of the interchangeability of individual NE/SA/SE5521 parts. This is the degree to which the oscillator frequency of anumber of NE/SA/SE5521 samples will vary from the median of that sample with a given timing capaictor.
Tempco of Oscillator Amplitude	A measure of how the oscillator amplitude varies with ambient temperature as that temperature deviates from a 25°C ambient.
Tempco of Oscillator Frequency	A measure of how the oscillator frequency varies with ambient temperature as that temperature deviates from a 25°C ambient.
Voltage Coefficient of Oscillator Frequency	The degree to which the oscillator frequency will vary as the reference voltage (V_{REF}) deviates from +10V.
Min OSC ($\overline{OSC}$) Load	Minimum load impedance for which distortion is guaranteed to be less than 5%.
Linearity Error	The degree to which the DC output of the demodulator/amplifier combination matches a change in the AC signal at the demodulator input. It is measured as the worst case nonlinearity from a straight line drawn between positive and negative fullscale end points.
Maximum Demodulator Input	The maximum signal that can be applied to the demodulator iput without exceeding the specified linearity error.

APPLICATION INFORMATION

$$OSC\ frequency = \frac{V_{REF} - 1.3V}{V_{REF}\ (R_T + 1.5k)\ C_T}$$

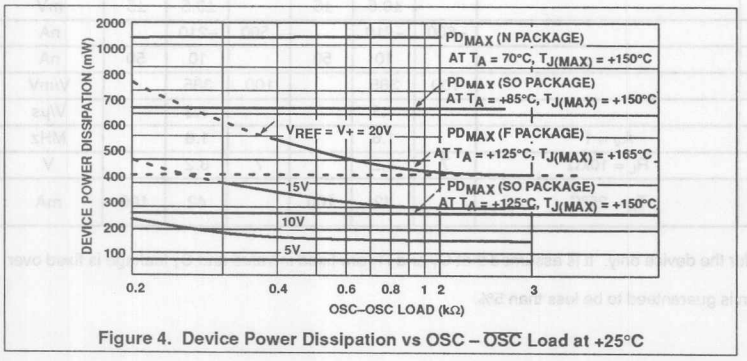


Figure 4. Device Power Dissipation vs OSC – $\overline{OSC}$ Load at +25°C

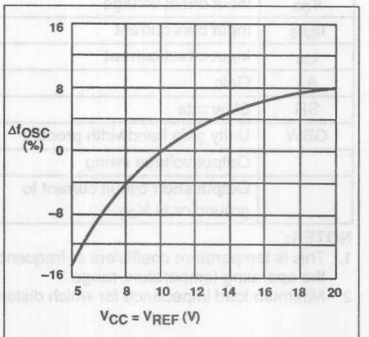


Figure 5. Oscillator Frequency Variation With Voltage (Normalized to $V_{REF} = V_{CC} = 10V$) $T_A = +25°C$

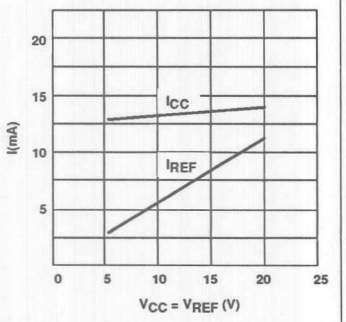


Figure 6. I_{REF} and I_{CC} vs Voltage (T_A = +25°C)

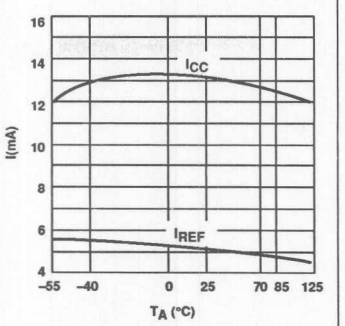


Figure 7. I_{REF} and I_{CC} vs Temperature (V_{REF} = V_{CC} = 10V)

Figure 6. I_{REF} and I_{CC} vs Voltage
(T_A = +25°C)

Figure 7. I_{REF} and I_{CC} vs Temperature
(V_{REF} = V_{CC} = 10V)

Section 13
Motor Control and Remote Control Circuits

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PCF1252X Family	Power failure detector and reset generator	695
TDA1023/T	Proportional-control triac triggering circuit	705
TEA1041T	Battery low-level indicator	720
TEA1088T	Switched-mode power supply battery charger control circuit	728
UAA1300	Voltage regulator with watchdog for microprocessor/controller systems	744

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Motor Control and Remote Control Circuits

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PCF1262X Family	Power failure detector and reset generator	695
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TEA1044T	Battery low level indicator	720
TEA1088T	Switched mode power supply battery charger control circuit	728
UAA1200	Voltage regulator with watchdog for microprocessor/controller systems	744

Power failure detector and reset generator PCF1252X Family

GENERAL DESCRIPTION

The PCF1252-X family are CMOS voltage detectors designed especially for power-ON/OFF detection in microcontroller/microprocessor systems (for initialization and data storage purposes). The output $\overline{POWF}$ is activated at a precise, temperature stable, trip-point. The RESET output has a built-in delay with duration determined by an external capacitor (C_{CT}). A second comparator (comparator 2) has been included to allow for the possibility of a second monitoring point in the system.

Features

- Low current consumption, typically 6 μA
- 10 versions available, trip-points vary from 2.55 V to 4.75 V
- Temperature stable trip-point
- Variable RESET delay
- Reset polarity selection
- Comparator for second level detection (e.g. overvoltage detection)
- Advance warning of power failure

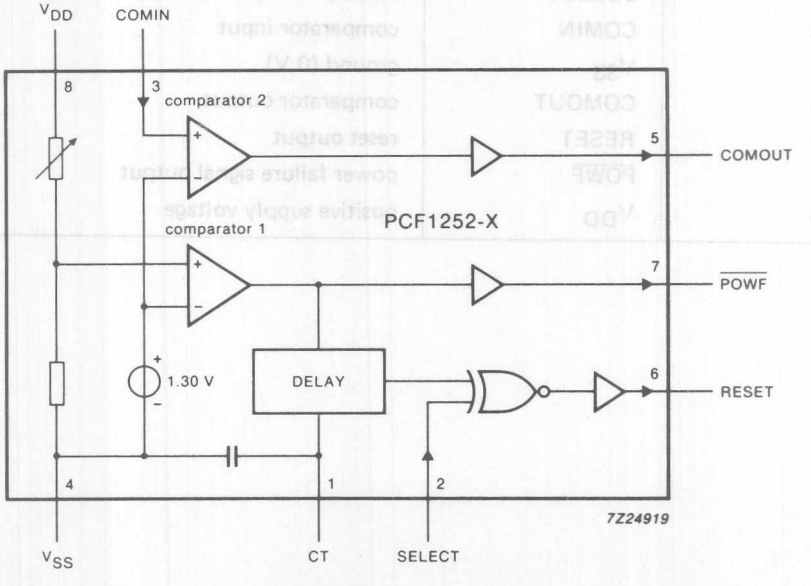


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF1252-XP: 8-lead DIL; plastic (SOT97).
PCF1252-XT: 8-lead mini-pack; plastic (SO8; SOT96A).

PINNING

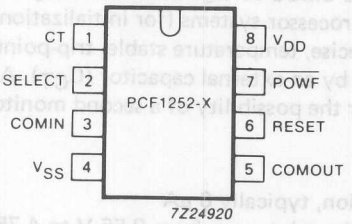


Fig.2 Pinning diagram.

pin no.	mnemonic	description
1	CT	connection for the external capacitor
2	SELECT	select polarity or external reset input
3	COMIN	comparator input
4	V_{SS}	ground (0 V)
5	COMOUT	comparator output
6	RESET	reset output
7	$\overline{POWF}$	power failure signal output
8	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION (see Fig.1)

The PCF1252-X contains a precise factory-programmed voltage reference, two comparators and a delay circuit. The PCF1252-X family is comprised of 10 versions with varying voltage trip-points (V_{TRIP}), see section "Characteristics".

Supply

The supply voltage (V_{DD}) is internally divided before being compared, via comparator 1, with the internal reference voltage.

$\overline{POWF}$ (see Fig.3)

The $\overline{POWF}$ output is:

- LOW, if V_{DD} is below V_{TRIP}.
- HIGH, if V_{DD} is above V_{TRIP}.

Power-ON reset (SELECT = LOW)

As V_{DD} rises past V_{TRIP}, a positive reset pulse is generated at RESET. The duration of the reset pulse (t_R) is determined by the value of the external capacitor (C_{CT}; maximum 1 μF, see Fig.8) connected to CT. With no external capacitor connected, C_{CT} assumes a minimum value of 100 pF. If SELECT is HIGH, the reset pulse is inverted.

Power failure

During a power-OFF condition ($V_{DD} < V_{TRIP}$), $\overline{POWF}$ goes LOW. After a time delay (t_S), also determined by C_{CT}, RESET goes HIGH. Any $\overline{POWF}$ output ($V_{DD} < V_{TRIP}$) will result in a subsequent RESET pulse.

Voltage trip-point

By selecting the voltage trip-point slightly higher than the minimum operating voltage of the microcontroller/microprocessor, there is sufficient time for data storage before the power actually fails.

In order to prevent oscillations around the voltage trip-point, a small hysteresis has been included, resulting in a power-ON switching point that is higher than the voltage trip-point (minimum of 15 mV). The voltage trip-point refers to the value at which power-OFF is signalled.

COMIN

Input to the second comparator (comparator 2). When used in conjunction with an external voltage divider, this allows a second point in the system to be monitored. This input has no built-in hysteresis. When not in use connect to V_{DD}. COMOUT will be LOW or HIGH depending on the voltage at COMIN:

- COMOUT = HIGH, if voltage at COMIN is above the switch point V_{SP} (typically 1.30 V).
- COMOUT = LOW, if voltage at COMIN is below the switch point V_{SP} (typically 1.30 V).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0.5	+ 7	V
Input voltage range		V_I	−0.5	V_{DD} + 0.5	V
DC clamp-diode current	all pins; $V_I < -0.5$ V or $> V_{DD}$ + + 0.5 V	I_I	–	20	mA
Output current		I_O	–	20	mA
Total power dissipation		P_{tot}	–	150	mW
Storage temperature range		T_{stg}	−65	+ 100	°C
Operating ambient tempetature range		T_{amb}	−40	+ 85	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal handling precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS (see Fig.3)

V_{DD} = 2.4 V to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 °C to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	2.4	–	6.0	V
Voltage trip-point:	T_{amb} = + 25 °C					
PCF1252-0		V_{TRIP}	4.70	4.75	4.80	V
PCF1252-1		V_{TRIP}	4.50	4.55	4.60	V
PCF1252-2		V_{TRIP}	4.20	4.25	4.30	V
PCF1252-3		V_{TRIP}	4.00	4.05	4.10	V
PCF1252-4		V_{TRIP}	3.70	3.75	3.80	V
PCF1252-5		V_{TRIP}	3.50	3.55	3.60	V
PCF1252-6		V_{TRIP}	3.20	3.25	3.30	V
PCF1252-7		V_{TRIP}	3.00	3.05	3.10	V
PCF1252-8		V_{TRIP}	2.70	2.75	2.80	V
PCF1252-9		V_{TRIP}	2.50	2.55	2.60	V
Supply current	T_{amb} = + 25 °C; see Figs 4 and 5					
	V_{DD} = V_{TRIP} + 0.5 V; COMIN = V_{DD}	I_{DD}	–	6	10	μA
Voltage trip-point temperature coefficient	note 1	ΔV_{TRIP}	–	$\pm 100 \times 10^{-6}$	$\pm 400 \times 10^{-6}$	/K
Voltage trip-point hysteresis		V_H	15	30	50	mV
COMIN switch point	T_{amb} = + 25 °C	V_{SP}	1.28	1.30	1.32	V
COMIN switch point temperature coefficient	note 1	ΔV_{SP}	–	±0.1	±0.5	mV/K
SELECT input voltage:						
LOW		V_{IL}	–	–	$0.3V_{DD}$	V
HIGH		V_{IH}	$0.7V_{DD}$	–	–	V
SELECT and COMIN leakage current:						
LOW		$-I_{IL}$	–	–	1.0	μA
HIGH		I_{IL}	–	–	1.0	μA
$\overline{POWF}$, RESET and COMOUT						
Output sink current	see Fig.6; V_O = 0.4 V; V_{DD} = 2.4 V	I_O	1	3	–	mA
Output source current	see Fig.7; V_O = 2.0 V; V_{DD} = 2.4 V	$-I_O$	0.75	2	–	mA
Reset time	note 2; C_{CT} = 1 nF	t_R	400	1000	2000	μs
Save time	note 2; C_{CT} = 1 nF	t_S	40	100	200	μs
Reset to save time ratio		t_R/t_S	–	10	–	

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
CT internal capacitance		C_{INT}	–	100	–	pF

Notes to the characteristics

1. Value given per degree Kelvin. Tested on a sample basis.
2. Conformance to these specifications is only guaranteed when the slew rate of V_{DD} is less than 25 V/ms.

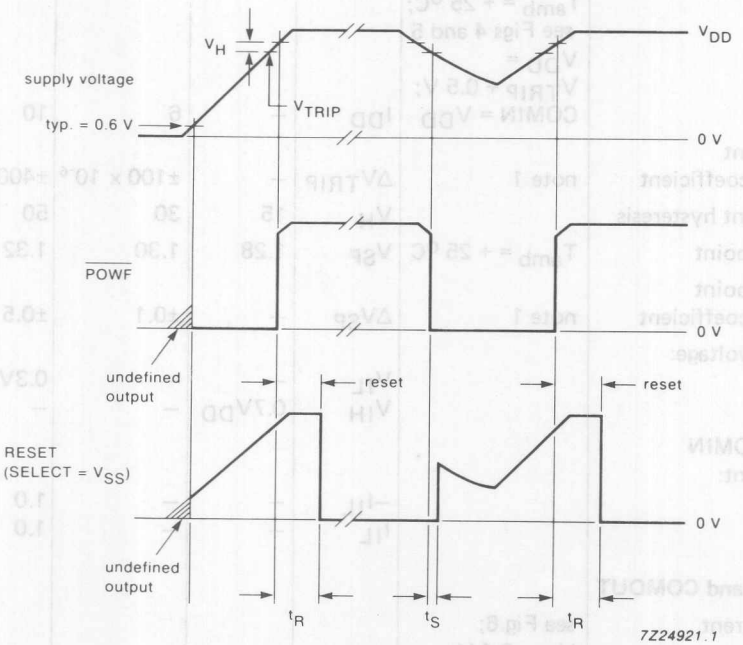


Fig.3 Timing diagram.

Typical performance characteristics

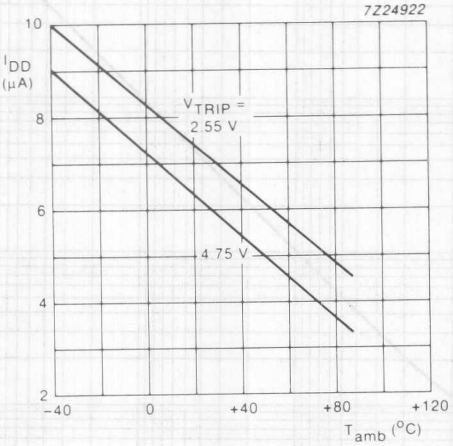


Fig.4 Supply current as a function of temperature; V_{DD} = 5 V; COMIN = V_{DD}.

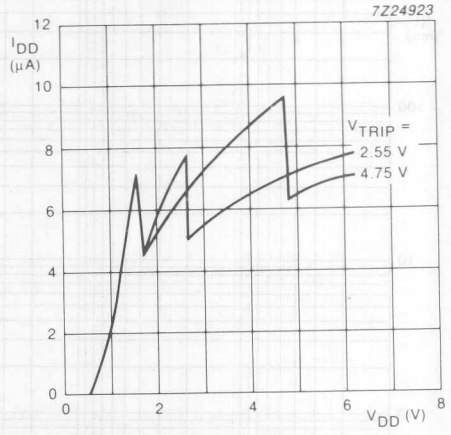


Fig.5 Supply current as a function of the supply voltage; T_{amb} = + 25 °C.

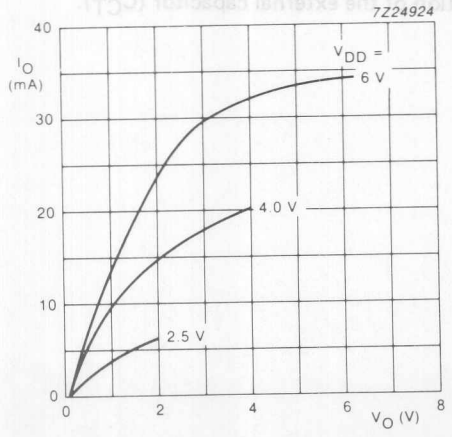


Fig.6 Output sink current as a function of the output voltage.

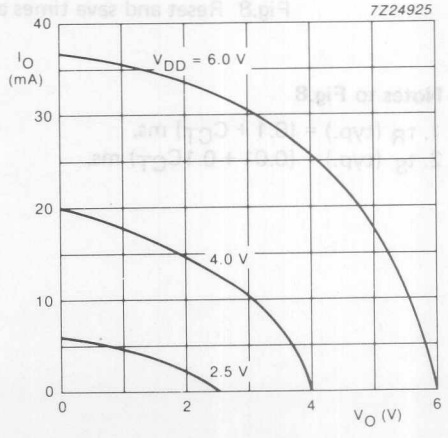


Fig.7 Output source current as a function of the output voltage.

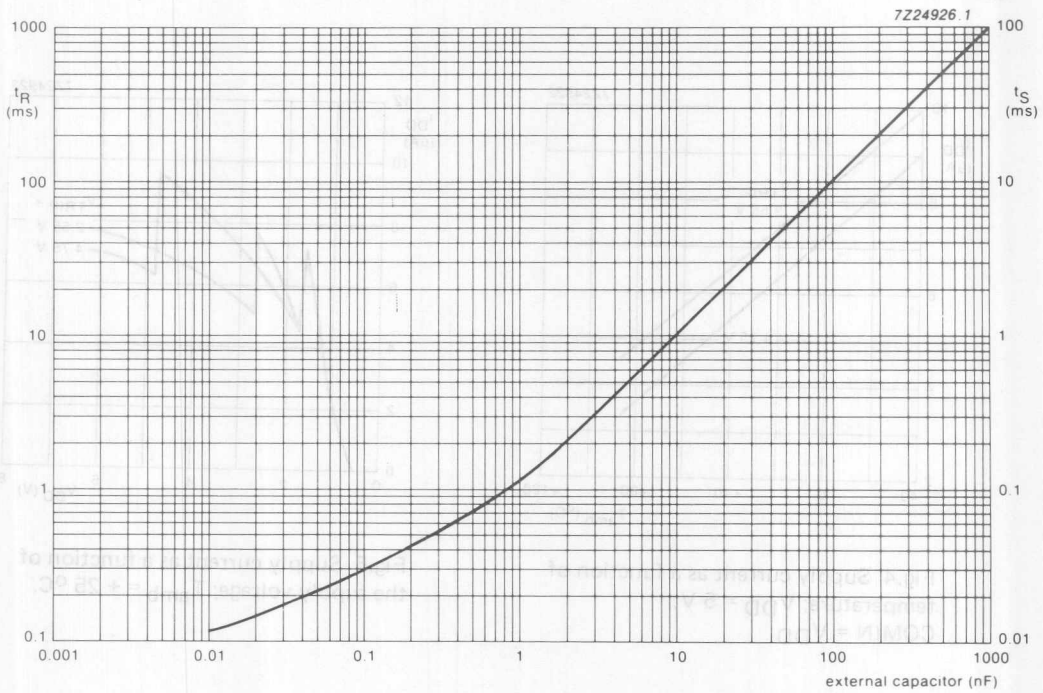


Fig.8 Reset and save times as a function of the external capacitor (C_{CT}).

Notes to Fig.8

1. t_R (typ.) = (0.1 + C_{CT}) ms.
2. t_S (typ.) = (0.01 + 0.1C_{CT}) ms.

APPLICATION INFORMATION

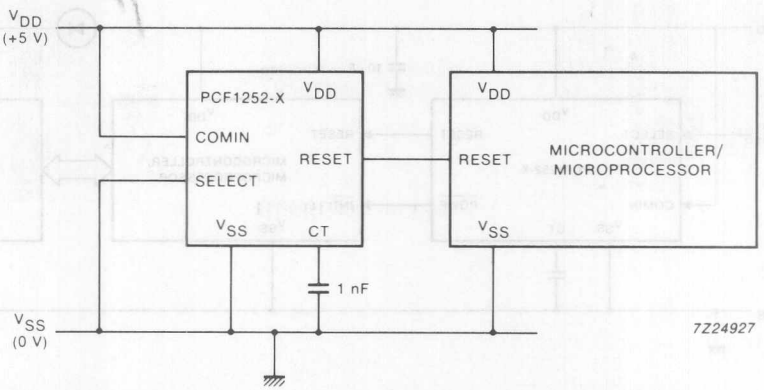


Fig.9 Typical power-ON reset circuit for a microcontroller/microprocessor system; (when not used, COMIN must be connected to V_{DD}).

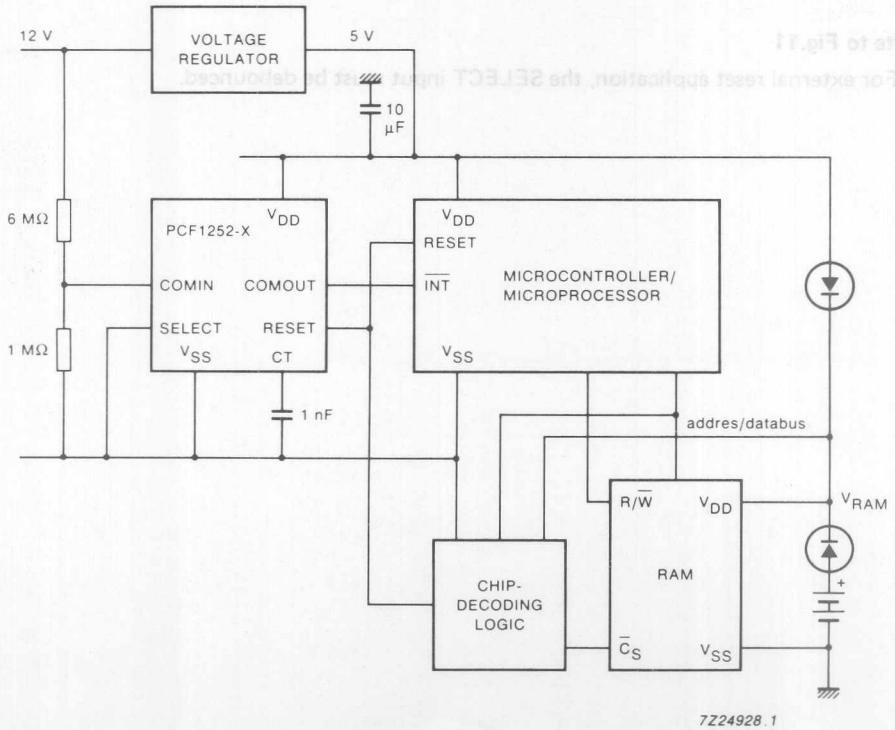


Fig.10 Data retention circuit for memory back-up systems.

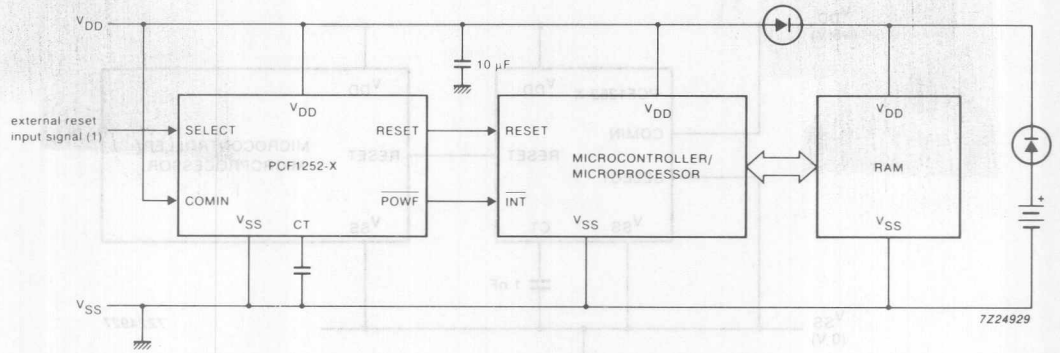


Fig.11 Data retention circuit with external switchable reset for systems with a single voltage supply.

Note to Fig.11

1. For external reset application, the SELECT input must be debounced.

Proportional-control triac triggering circuit

TDA1023/T

FEATURES

- Adjustable width of proportional range
- Adjustable hysteresis
- Adjustable width of trigger pulse
- Adjustable repetition timing of firing burst
- Control range translation facility
- Fail safe operation
- Supplied from the mains
- Provides supply for external temperature bridge

APPLICATIONS

- Panel heaters
- Temperature control

GENERAL DESCRIPTION

The TDA1023 is a bipolar integrated circuit for controlling triacs in a proportional time or burst firing mode. Permitting precise temperature control of heating equipment it is especially suited to the control of panel heaters. It generates positive-going trigger pulses but complies with regulations regarding mains waveform distortion and RF interference.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage (derived from mains voltage)	-	13.7	-	V
V_Z	stabilized supply voltage for temperature bridge	-	8	-	V
$I_{16(AV)}$	supply current (average value)	-	10	-	mA
t_w	trigger pulse width	-	200	-	µs
T_b	firing burst repetition time at C_T = 68 µF	-	41	-	s
$-I_{OH}$*	output current	-	-	150	mA
T_{amb}	operating ambient temperature range	−20	-	+75	°C

Note

*Negative current is defined as conventional current flow out of a device. A negative output current is suited for positive triac triggering.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1023	16	DIL	plastic	SOT38
TDA1023T	16	mini-pack	plastic	SO16; SOT109A

Proportional-control triac triggering circuit

TDA1023/T

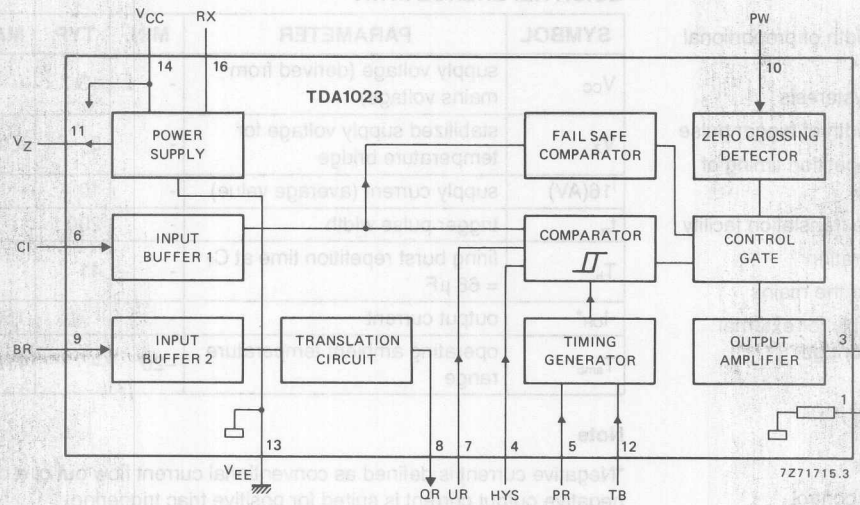


Fig.1 Block diagram.

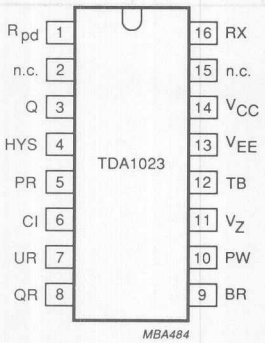


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
R_{pd}	1	internal pull-down resistor
n.c.	2	not connected
Q	3	output
HYS	4	hysteresis control input
PR	5	proportional range control input
CI	6	control input
UR	7	unbuffered reference input
QR	8	output of reference buffer
BR	9	buffered reference input
PW	10	pulse width control input
V_Z	11	reference supply output
TB	12	firing burst repetition time control input
V_{EE}	13	ground
V_{CC}	14	positive supply
n.c.	15	not connected
RX	16	external resistor connection

FUNCTIONAL DESCRIPTION

The TDA1023 generates pulses to trigger a triac. These pulses coincide with the zero excursions of the mains voltage, thus minimizing RF interference and mains supply transients. In order to gate the load on and off, the trigger pulses occur in bursts thus further reducing mains supply pollution. The average power in the load is varied by modifying the duration of the trigger pulse burst in accordance with the voltage difference between the control input CI and the reference input, either UR or BR.

Power supply: V_{CC}, RX and V_z (pins 14, 16 and 11)

The TDA1023 is supplied from the AC mains via a resistor R_D to the RX connection (pin 16); the V_{EE} connection (pin 13) is linked to the neutral line (see Fig.4a). A smoothing capacitor C_S should be coupled between the V_{CC} and V_{EE} connections.

A rectifier diode is included between the RX and V_{CC} connections whilst the DC supply voltage is limited by a chain of stabilizer diodes between the RX and V_{EE} connections (see Fig.3).

A stabilized reference voltage (V_Z) is available at pin 11 to power an external temperature sensing bridge.

Supply operation

During the positive mains half-cycles the current through the external voltage dropping resistor R_D charges the external smoothing capacitor C_S until RX attains the stabilizing potential of the internal stabilizing diodes. R_D should be selected to be capable of supplying the current I_{CC} for the TDA1023, the average output current $I_{3(AV)}$, recharge the smoothing capacitor C_S and provide the supply for an external temperature bridge. (see Figs 9 to 12). Any excess current is by-passed by the internal stabilizer diodes. The maximum rated supply current, however, must not be exceeded.

During the negative mains half-cycles external smoothing capacitor C_S supplies the sum of the current demand described above. Its capacitance must be sufficiently high to maintain the supply voltage above the specified minimum.

Dissipation in resistor R_D is halved by connecting a diode in series (see Fig.4b and 9 to 12). A further reduction in dissipation is possible by using a high quality dropping capacitor C_D in series with a resistor R_{SD} (see Figs 4c and 14). Protection of the TDA1023 and the triac against mains-borne transients can be provided by connecting a suitable VDR across the mains input.

Control and reference inputs CI, BR and UR (pins 6, 9 and 7)

For the control of room temperature (5 °C to 30 °C) optimum performance is obtained by using the translation circuit. The buffered reference input BR (pin 9) is used as a reference input whilst the output reference buffer QR (pin 8) is connected to the unbuffered reference input UR (pin 7). This ensures that the range of room temperature is encompassed in most of the rotation of the potentiometer to give a linear temperature scale with accurate setting.

Should the translation circuit not be required, the unbuffered reference input UR (pin 7) is used as a reference input. The buffered reference input BR (pin 9) must then be connected to the reference supply output V_Z (pin 11).

For proportional power control the unbuffered reference input UR (pin 7) must be connected to the firing burst repetition time control input TB (pin 12).The buffered reference input BR (pin 9), which is in this instance inactive, must then be connected to the reference supply output V_Z (pin 11).

Proportional range control input PR (pin 5)

The output duty factor changes from 0% to 100% by a variation of 80 mV at the control input CI (pin 6) with the proportional range control input PR open. For temperature control this corresponds to a temperature difference of 1 K.

By connecting the proportional range control input PR (pin 5) to ground the range may be increased to 400 mV, i.e. 5 K. Intermediate values may be obtained by connecting the PR input to ground via a resistor R5 (see Table 1).

Hysteresis control input HYS (pin 4)

With the hysteresis control input HYS (pin 4) open, the device has a built-in hysteresis of 20 mV. For temperature control this corresponds with 0.25 K.

Hysteresis is increased to 320 mV, corresponding to 4 K, by grounding HYS (pin 4). Intermediate values are obtained by connecting pin 4 via resistor R4 to ground. Table 1 provides a set of values for R4 and R5 giving a fixed ratio between hysteresis and proportional range.

Trigger pulse width control input PW (pin 10)

The width of the trigger pulse may be adjusted to the value required for the triac by choosing the value of the external synchronization resistor

R_S between the trigger pulse width control input PW (pin 10) and the AC mains. The pulse width is inversely proportional to the input current (see Fig.13).

Output Q (pin 3)

Since the circuit has an open-emitter output it is capable of sourcing current. It is thus suited for generating positive-going trigger pulses. The output is current-limited and short-circuit protected. The maximum output current is 150 mA and the output pulses are stabilized at 10 V for output currents up to that value.

To minimize the total supply current and power dissipation, a gate resistor R_G must be connected between the output Q and the triac gate to limit the output current to the minimum required by the triac (see Figs 5 to 8).

Pull-down resistor R_{pd} (pin 1)

The TDA1023 includes a 1.75 kΩ pull-down resistor R_{pd} between pins 1 and 13 (V_{EE}, ground connection) intended for use with sensitive triacs.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage	-	16	V
Supply current				
$I_{16(AV)}$	average	-	30	mA
$I_{16(RM)}$	repetitive peak	-	100	mA
$I_{16(SM)}$	non-repetitive peak (tp < 50 µs)	-	2	A
V_I	input voltage, all inputs	-	16	V
$I_{6, 7, 9, 10}$	input current	-	10	mA
V_1	voltage on R_{pd} connection	-	16	V
$V_{3, 8, 11}$	output voltage, Q, QR, V_Z	-	16	V
Output current				
$-I_{OH(AV)}$	average	-	30	mA
$-I_{OH(M)}$	peak max. 300 µs	-	700	mA
P_{tot}	total power dissipation	-	500	mW
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−20	+75	°C

CHARACTERISTICS

V_{CC} = 11 to 16 V; T_{amb} = –20 to +75 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	internally stabilized supply voltage at I_{16} = 10mA		12	13.7	15	V
$\Delta V_{CC}/\Delta I_{16}$	variation with I_{16}		-	30	-	mV/mA
I_{16}	supply current at V_{16-13} = 11 to 16 V I_{10} = 1mA; f = 50 Hz; pin 11 open; $V_{6-13} > V_{7-13}$	pins 4 and 5 open	-	-	6	mA
		pins 4 and 5 grounded	-	-	7.1	mA
Reference supply output V_Z (pin 11) for external temperature bridge						
V_{11-13}	output voltage		-	8	-	V
$-I_{11}$	output current		-	-	1	mA
Control and reference inputs CI, BR and UR (pins 6, 9 and 7)						
V_{6-13}	input voltage to inhibit the output		-	7.6	-	V
$I_{6, 7, 9}$	input current	V_1 = 4 V	-	-	2	µA
Hysteresis control input HYS (pin 4)						
ΔV_6	hysteresis	pin 4 open	9	20	40	mV
ΔV_6	hysteresis	pin 4 grounded	-	320	-	mV
Proportional control range input PR (pin 5)						
ΔV_6	proportional range	pin 5 open	50	80	130	mV
ΔV_6	proportional range	pin 5 grounded	-	400	-	mV
Pulse width control input PW (pin 10)						
t_w	pulse width	$I_{10(RMS)}$ = 1mA; f = 50 Hz	100	200	300	µs
Firing burst repetition time control input TB (pin 12)						
T_bC_T	firing burst repetition time, ratio to capacitor C_T		320	600	960	ms/µF
Output of reference buffer QR (pin 8)						
	output voltage at input voltage:					
V_{8-13}		V_{9-13} = 1.6 V	-	3.2	-	V
V_{8-13}		V_{9-13} = 4.8 V	-	4.8	-	V
V_{8-13}		V_{9-13} = 8 V	-	6.4	-	V
Output Q (pin 3)						
V_{OH}	output voltage HIGH	$-I_{OH}$ = 150 mA	10	-	-	V
$-I_{OH}$	output current HIGH		-	-	150	mA
Internal pull-down resistor R_{pd} (pin 1)						
R_{pd}	resistance to V_{EE}		1	1.75	3	kΩ

Table 1 Adjustment of proportional range and hysteresis. Combinations of resistor values giving hysteresis > $^1/_4$ proportional range.

Proportional range	Proportional range resistor	Minimum hysteresis	Maximum hysteresis resistor
	R5		R4
mV	kΩ	mV	kΩ
80	open	20	open
160	3.3	40	9.1
240	1.1	60	4.3
320	0.43	80	2.7
400	0	100	1.8

Table 2 Timing capacitor values C_T

Effective DC value	Marked AC specification		Catalogue number*
µF	µF	V	
68	47	25	2222 016 90129
47	33	40	- - 90131
33	22	25	- 015 90102
22	15	40	- - 90101
15	10	25	- - 90099
10	6.8	40	- - 90098

Note

*Special electrolytic capacitors recommended for use with the TDA1023.

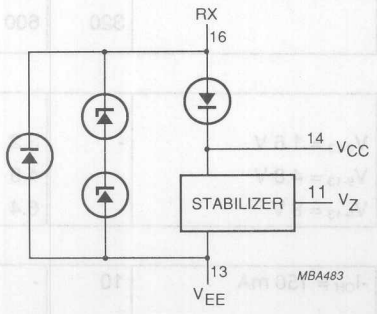


Fig.3 Internal supply connections.

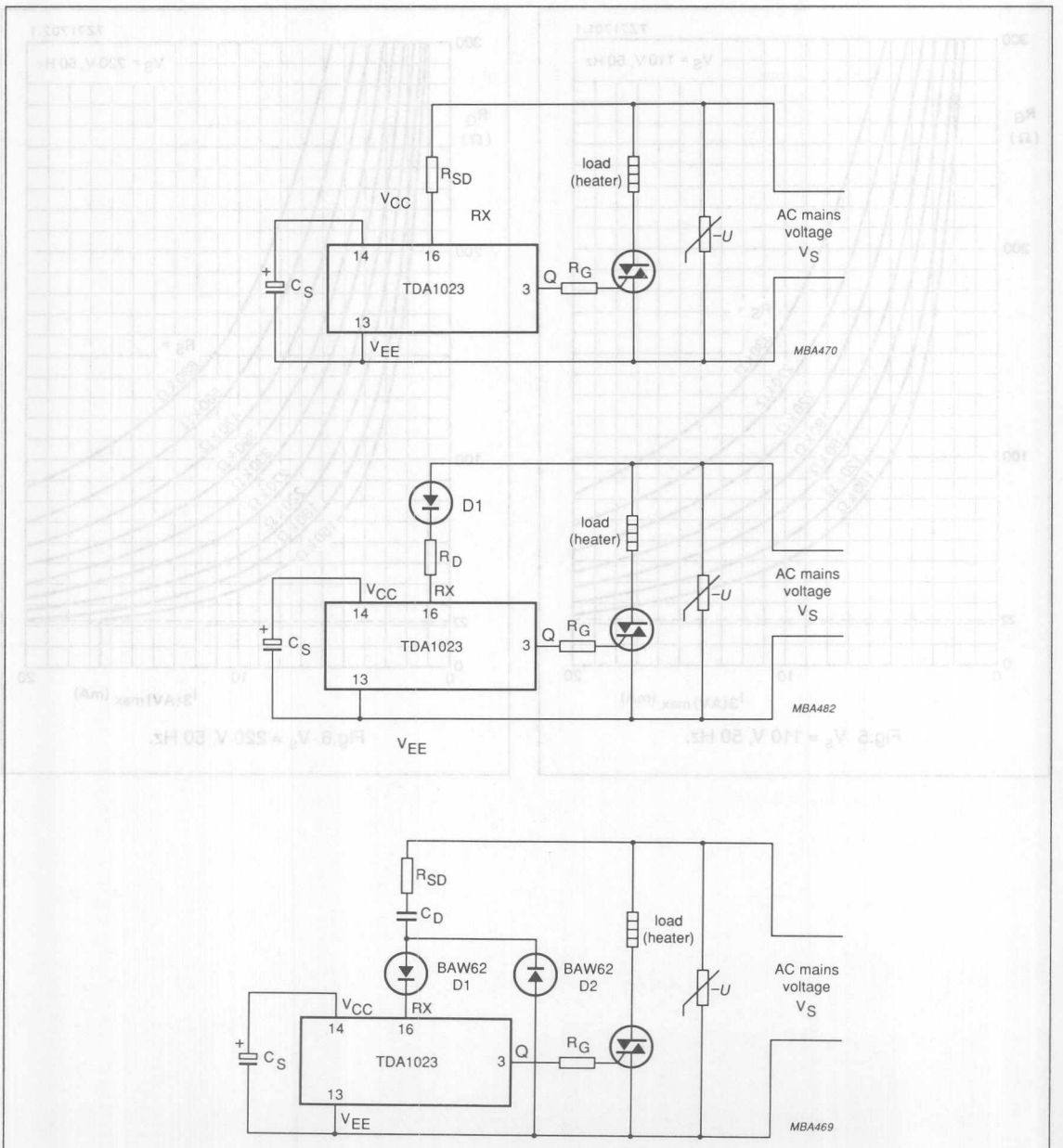


Fig.4 Alternative supply arrangements.

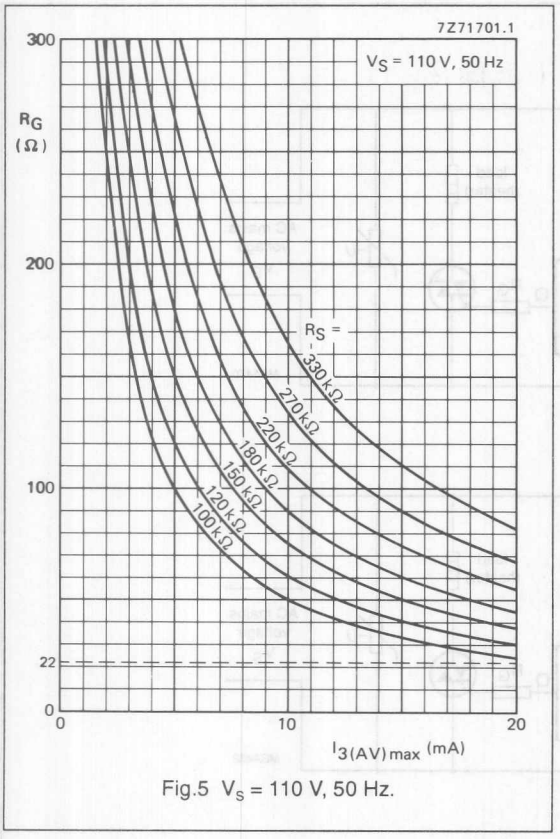


Fig.5 V_S = 110 V, 50 Hz.

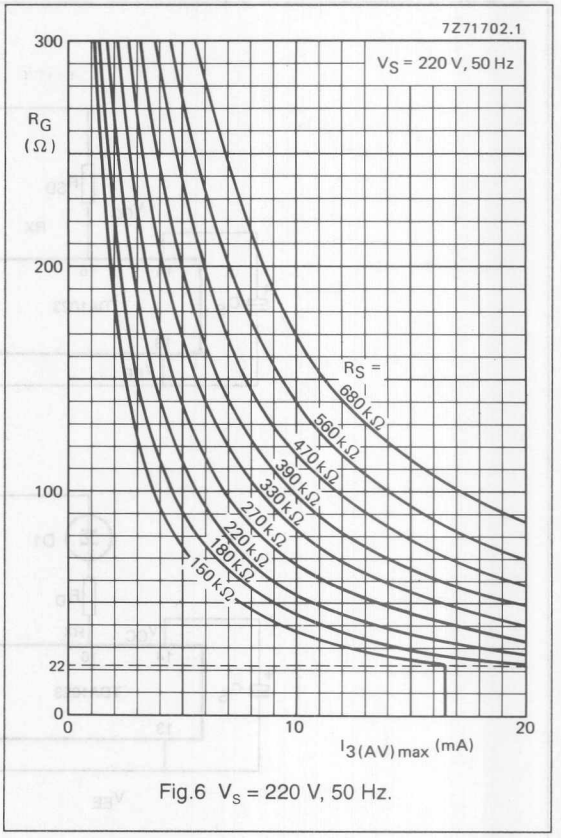


Fig.6 V_S = 220 V, 50 Hz.

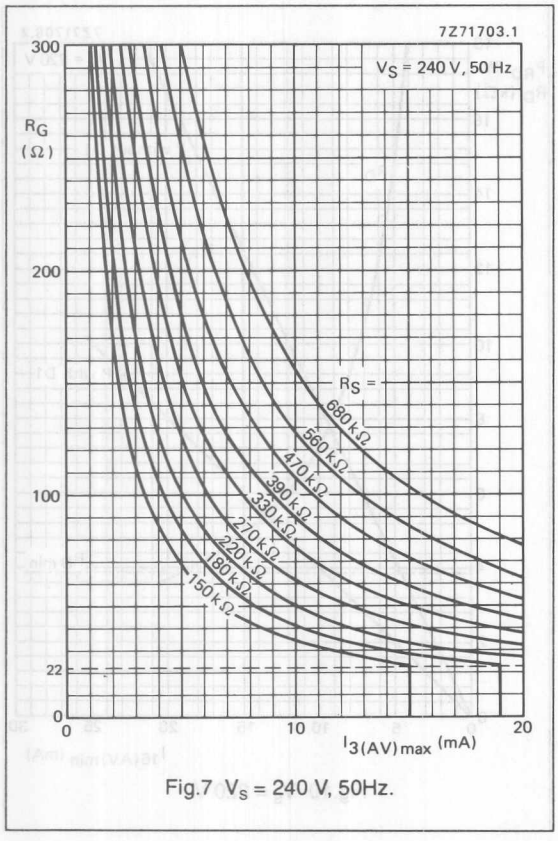


Fig.7 V_S = 240 V, 50Hz.

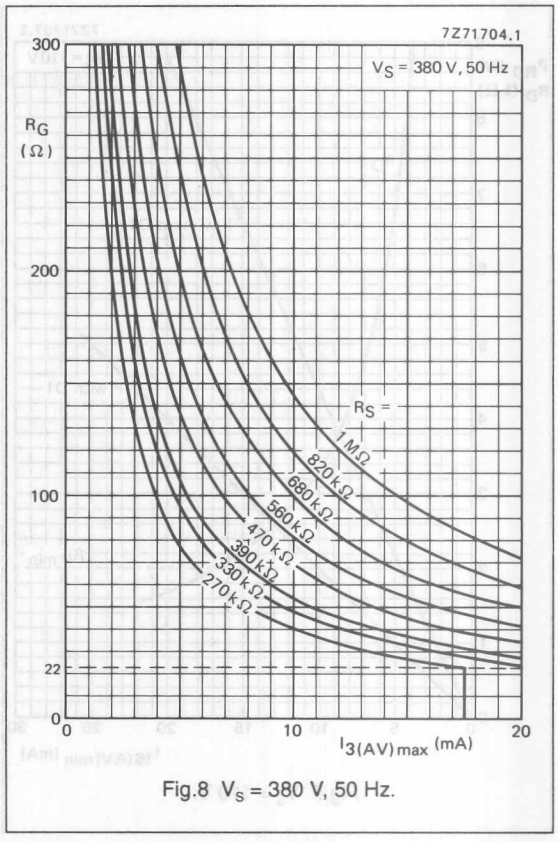


Fig.8 V_S = 380 V, 50 Hz.

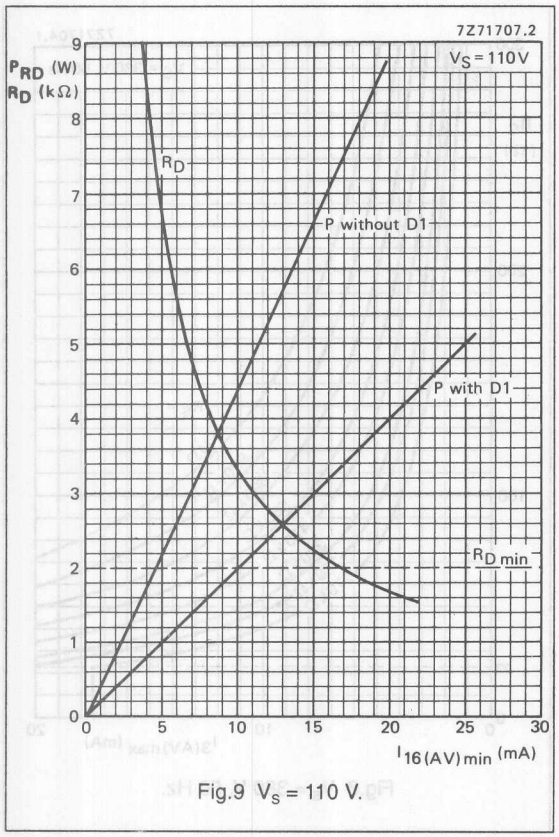


Fig.9 V_S = 110 V.

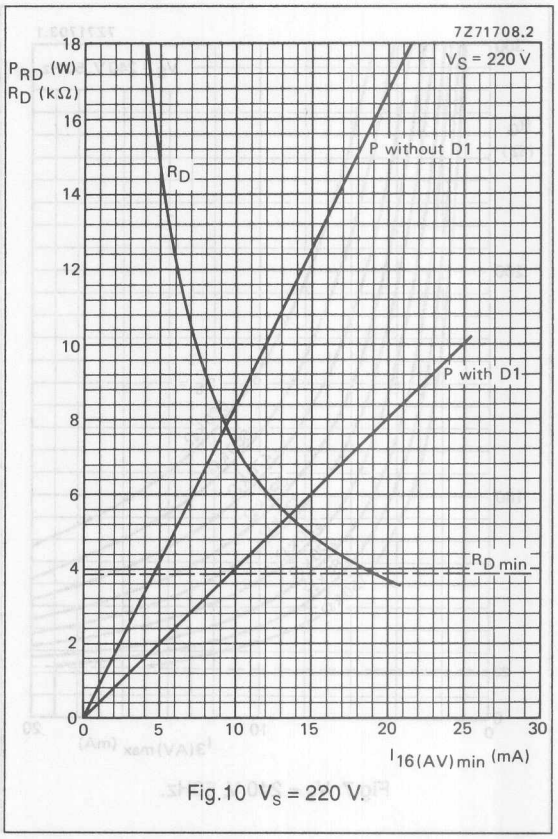


Fig.10 V_S = 220 V.

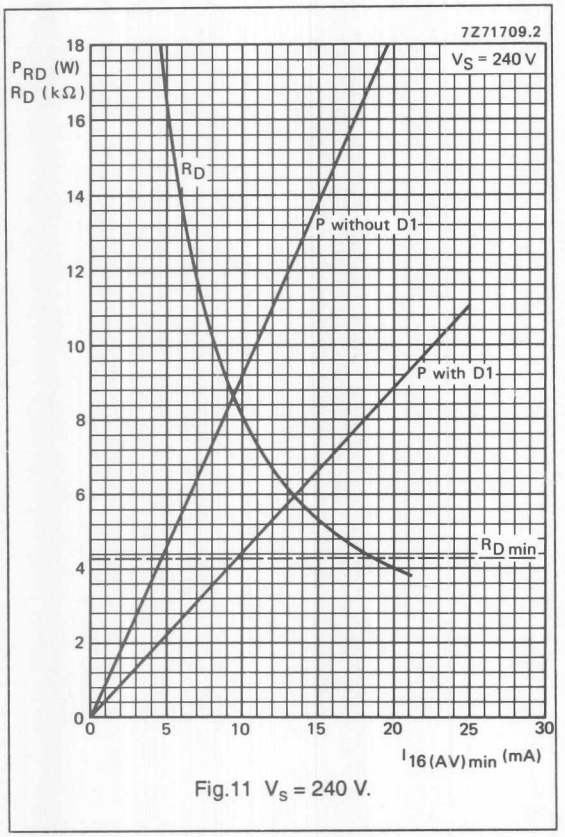


Fig.11 V_S = 240 V.

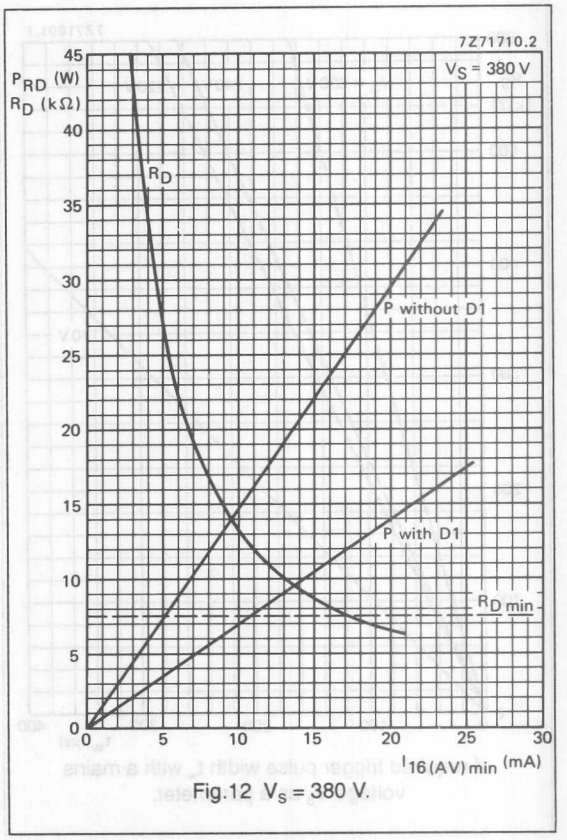
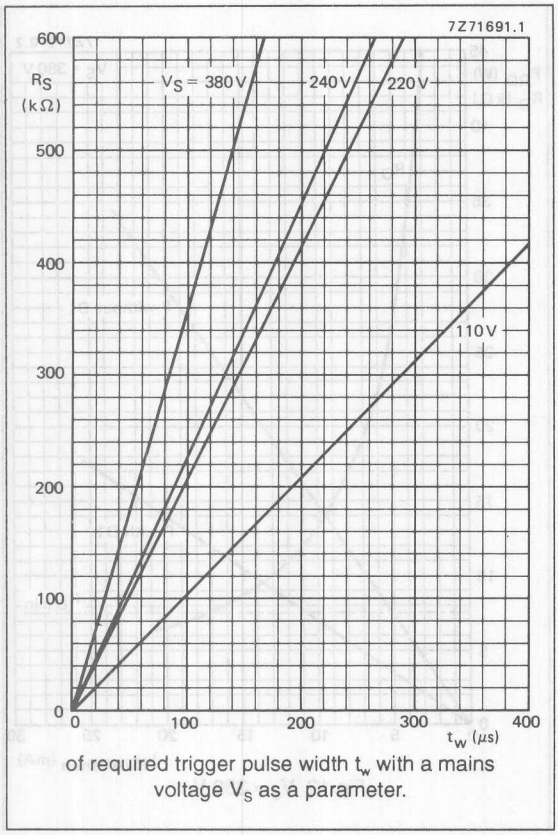


Fig.12 V_S = 380 V.



of required trigger pulse width t_w with a mains voltage V_S as a parameter.

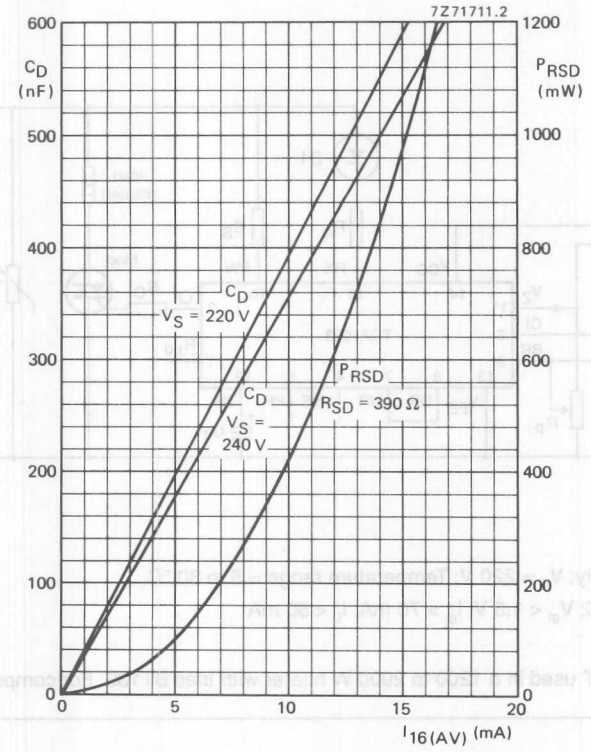
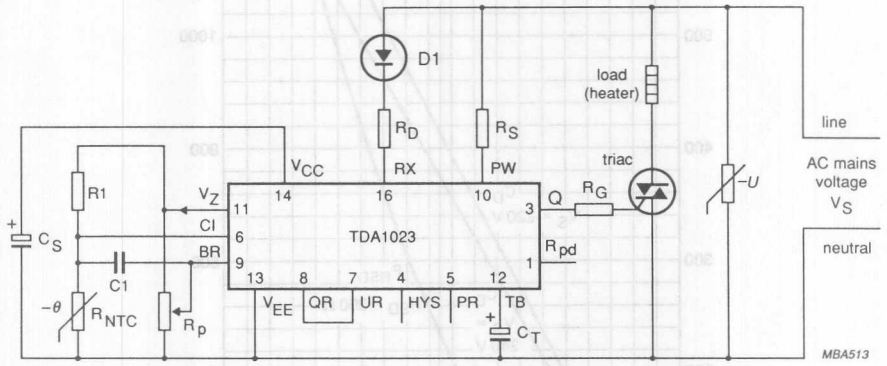


Fig.14 Nominal value of voltage dropping capacitor C_D and power P_{RSD} dissipated in a voltage dropping resistor R_{SD} as a function of average supply current $I_{16\ (AV)}$ with the mains supply voltage V_S as a parameter.



Conditions:- Mains supply; V_S = 220 V; Temperature range = 5 to 30 °C.
BT139 data at T_j = 25 °C; V_{gt} < 1.5 V; I_{gt} > 70 mA; I_L < 60 mA

Fig.15 The TDA1023/T used in a 1200 to 2000 W heater with triac BT139. For component values see Table 3.

Table 3 Temperature controller component values (see Fig. 15).

SYMBOL	PARAMETER	REMARKS	VALUE
t_w	trigger pulse width	see BT139 data sheet	75 µs
R_S	synchronization resistor	see Fig. 13	180 kΩ
R_G	gate resistor	see Fig. 6	110 Ω
$I_{3(AV)}$	max. average gate current	see Fig.8	4.1 mA
R4	hysteresis resistor	see Table 1	n.c.
R5	proportional band resistor	see Table 1	n.c.
$I_{16(AV)}$	min. required supply current		11.1 mA
R_D	mains dropping resistor	see Fig. 10	6.2 kΩ
P_{RD}	power dissipated in R_D	see Fig.10	4.6 W
C_T	timing capacitor (eff. value)	see Table 2	68 µF
VDR	voltage dependent resistor	cat. no. 2322 593 62512	250 V AC
D1	rectifier diode		BYW56
R1	resistor to pin 11	1% tolerance	18.7 kΩ
R_{NTC}	NTC thermistor (at 25 °C)	B = 4200 K cat no. 2322 642 12223	22 kΩ
R_p	potentiometer		22 kΩ
C1	capacitor between pins 6 and 9		47 nF
C_S	smoothing capacitor		220 µF; 16 V
If R_D and D1 are replaced by C_D and R_{SD}			
C_D	mains dropping capacitor		470 nF
R_{SD}	series dropping resistor		390 Ω
P_{RSD}	power dissipated in R_{SD}	see Fig.14	0.6 W
VDR	voltage dependent resistor	cat. no. 2322 594 62512	250 V AC

Notes

1. ON/OFF control: pin 12 connected to pin 13.
2. If translation circuit is not required: slider of R_p to pin 7; pin 8 open; pin 9 connected to pin 11.

Battery low-level indicator TEA1041T

FEATURES

- Optical signal following battery low-level detection
- Additional warning ('recharge needed') at end of system operation
- One or two LED indication
- Trigger level adjustable
- Low stand-by current
- Insensitive to interference
- Few external components

APPLICATIONS

- Battery operated systems

GENERAL DESCRIPTION

Intended for use with battery operated systems, the TEA1041T generates an optical alarm via one or two LEDs when the battery supply voltage falls below a preset threshold level.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_p	supply voltage	1.8	-	4.0	V
I_{sb}	stand-by current	-	-	10	µA
P_{tot}	total power dissipation	-	-	150	mW
I_L	output current LED outputs	-	-	59	mA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1041T	8	SO8	plastic	SOT96A

FUNCTIONAL DESCRIPTION

Supply (pin 8)

The supply voltage, which may range from 1.8 to 4.0 V, is connected to pin 8.

Voltage sense input (pin 1)

Pin 1 is connected to a trigger circuit consisting of a trigger amplifier and a Schmitt trigger.

An up / down counter in the control and timing logic is enabled when the potential at pin 1 falls below 1.25 V. Unless this voltage increases above 1.25 V the counter will operate for approximately two seconds. When the voltage increases or the count is timed-out, the counter will then begin counting-down. The circuit is thus protected from any disturbance of less than two seconds duration. LED 1 becomes lit on the next occasion that for two seconds the potential on pin 1 is less than 1.25 V.

Following low level detection the circuit is de-activated by operation of S1. For a period of 4 seconds LEDs 1 and 2 will then each be alternately lit for a duration of approximately 500 ms.

LED 1 and LED 2 connections (pin 7, 6)

The cathodes of LEDs 1 and 2 must be connected respectively to pins 7 and 6. The circuit will also function with only LED 1 connected.

Oscillator capacitor connection (pin 4)

Circuit timing is provided by the internal oscillator, the frequency of which is determind by a capacitor connected to pin 4.

Forcing a current (max. 5 mA) into pin 4 permits direct monitoring of the trigger circuit at pins 6 and 7. When V_1 is above 1.25 V, pin 7 will be LOW and pin 6 will be HIGH. Alternatively, when V_1 is below the 1.25 V threshold level pin 7 will be HIGH while pin 6 will be rendered LOW. This feature facilitates easier circuit adjustment.

Pin 2 Test Pin

An external clock signal may be connected to pin 2 for test purposes. This may be used to shorten the test time (see also test and application information).

Battery low-level indicator TEA1041T

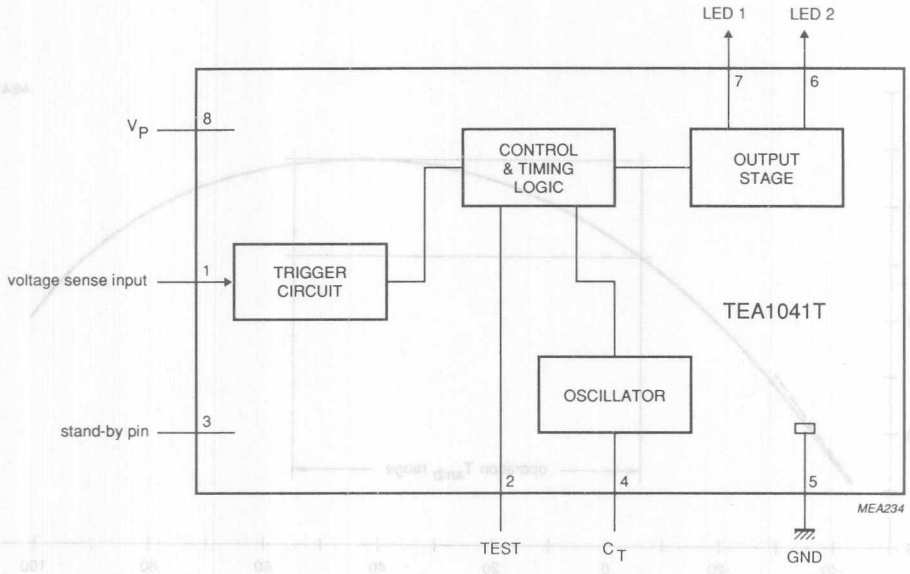


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_I	1	voltage sense input
TEST	2	test pin
V_{sw}	3	stand-by
C_T	4	oscillator capacitor
GND	5	ground
L2	6	LED 2
L1	7	LED 1
V_p	8	supply voltage

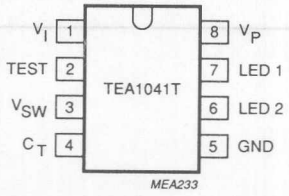


Fig.2 Pin configuration.

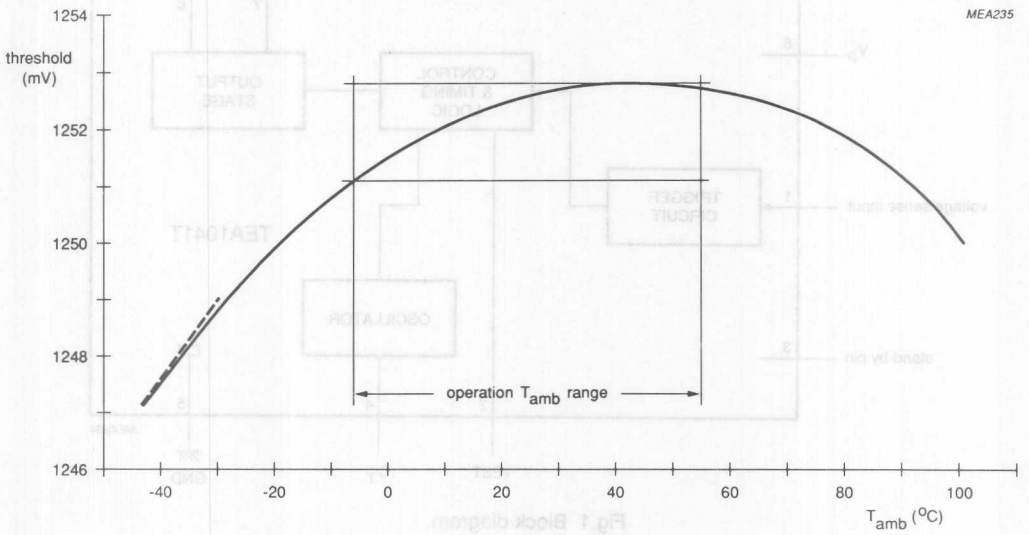


Fig.3 Thermal drift of the input threshold.

LIMITING VALUES

In accordance with the absolute maximum system (IEX 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_j	junction temperature	–25	+125	°C
T_{stg}	storage temperature range	–25	+125	°C
V_{max}	maximum voltage (pins 1, 3 and 8)	–0.5	4	V
V_{max}	maximum voltage (pins 6 and 7)	–0.5	5.5	V
I_4	maximum current into pin 4	-	5	mA
	during 1 µs into V_p	-	90	mA
I_{max}	maximum current into test pin	-	0.5	mA
P_{tot}	total power dissipation	-	150	mW
T_{amb}	operating ambient temperature range	–5	+55	°C

Note

Voltages with respect to 0 V unless otherwise specified

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT.
R_{th}	thermal resistance	mounted on PC board	-	240	-	K/W
R_{th}		mounted on ceramic	-	170	-	K/W
R_{th}		mounted with heatsink on ceramic	-	120	-	K/W

CHARACTERISTICS

Voltages with respect to 0 V; $Tamb_{min} < Tamb < Tamb_{max}$; $V_{SW} = 0$ V, $V_p = 1.8$ to 4.0 V; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_p	supply voltage range		1.8	-	4	V
V_{cl}	clamp voltage V_p; V_{SW}; V_I	I = 10 mA	-	7.5	8.5	V
I_{SW}	supply current	$V_p = 1.8$ - 4 V	0.65	-	2.2	mA
I_p		$V_p = 1.8$ V; FF is not triggered	2.2	-	4.4	mA
I_p		$V_p = 4$ V; FF is triggered	4	-	8	mA
I_{sb}	stand-by current	measured 1 s after S1 is opened; $V_p = 4$ V	-	-	10	µA
Trigger amplifier T						
V_I	threshold	$T_j = 25$ °C	1.17	1.25	1.33	V
	temperature coefficient		–250	-	+250	10^{-6}/°C
ΔV_I	lifetime drift threshold level		-	1	-	mV/1000h
	hysteresis at input V_I due to Schmitt trigger		3	5	7	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing circuitry						
t_{PLH}	propagation delay during adjustment	from passing threshold at input to 50% of output switching edge at I_O = 1 mA	-	1	10	µs
t_s	settling time of IC during adjustment		-	-	1	ms
f_{osc}	oscillator frequency	C = 10 nF; V_p = 2 to 2.8 V	5.7	8.2	10.7	kHz
I_c	required current I_c to switch adjusting circuitry		2.2	-	2.8	mA
Output circuit						
I_{L1}	output current	$V_{L1} = V_{LB2}$ = 0.5 V; V_p = 1.8 V	14	20	39	mA
I_{L2}		$V_{L1} = C_{L2}$ = 2.5 V V_p = 4 V	-	-	59	mA
ΔI_L	output current difference 100 (I_{L1} - I_{L2} / (I_{L1} + I_{L2}) / 2)		–15	-	+15	%
V_{sat}	output saturation voltage	I_{L1}; I_{L2} = 10 mA	-	-	200	mV
	output leakage current	$T_j \leq 55°C$; V_p = 4 V	-	-	10	µA
Test pin TP						
V_2	high voltage level	used as output	450	-	-	mV
V_2	low voltage level	used as output	-	-	150	mV
$+I_{TP}$	required input current high	used as input	300	-	-	µA
$-I_{TP}$	input current low	used as input	-	-	40	µA
f_{test}	maximum input frequency		10	-	-	kHz

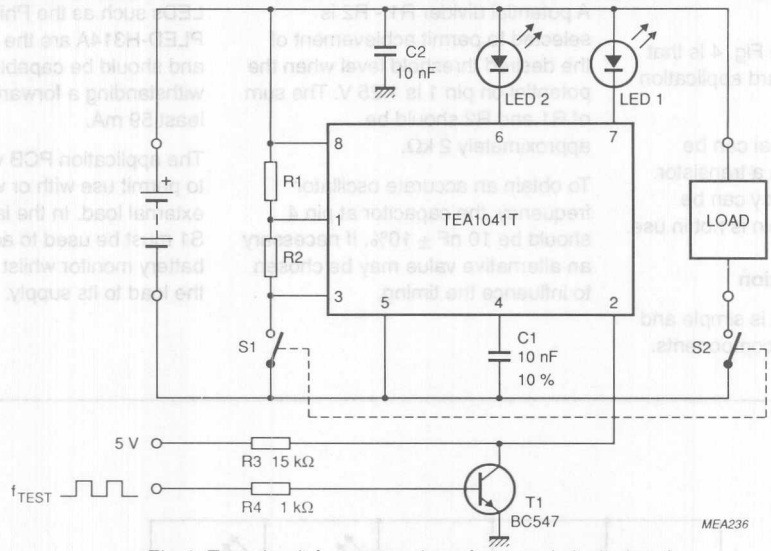


Fig.4 Test circuit for connection of external clock signal.

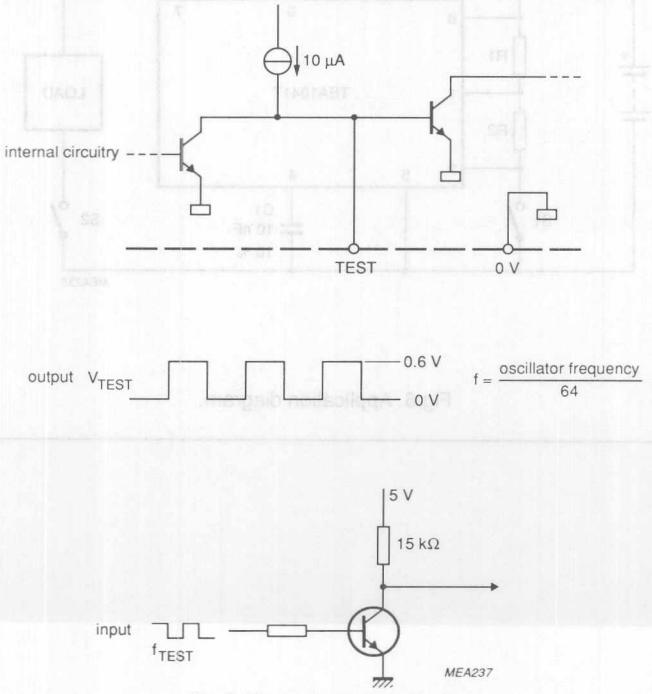


Fig.5 Test information pin 2.

Test information

The circuit depicted in Fig. 4 is that realized on the standard application PCB.

An external clock signal can be connected to pin 2 via a transistor. The oscillator frequency can be monitored when this pin is not in use.

Application information

The application circuit is simple and requires few external components.

A potential divider R1 - R2 is selected to permit achievement of the desired threshold level when the potential on pin 1 is 1.25 V. The sum of R1 and R2 should be approximately 2 kΩ.

To obtain an accurate oscillator frequency, the capacitor at pin 4 should be 10 nF ± 10%. If necessary an alternative value may be chosen to influence the timing.

LEDs such as the Philips PLED-H314A are the most suitable and should be capable of withstanding a forward current of at least 59 mA.

The application PCB was designed to permit use with or without an external load. In the latter instance S1 must be used to activate the battery monitor whilst S2 connects the load to its supply.

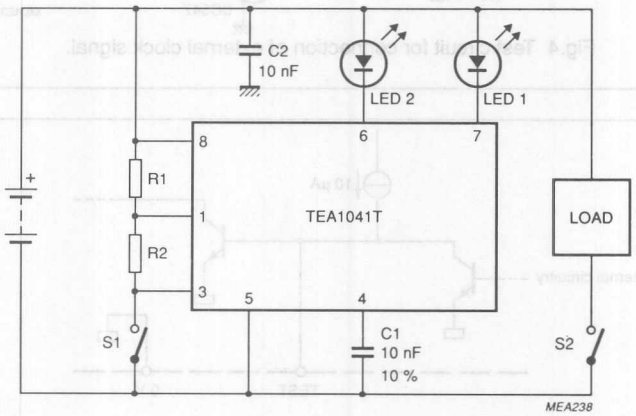
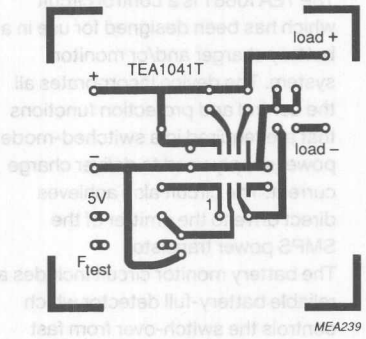


Fig.6 Application diagram.



Printed circuit board copper side, scale 2:1

Fig.7 Application PCB details.

APPLICATION CIRCUIT COMPONENT DETAILS

REFERENCE	TYPE	VALUE	UNIT
R1 + R2	-	±2	kΩ
R3	-	15	kΩ
R4	-	1	kΩ
C1	-	10 ±10%	nF
C2	-	10	nF
LED1, LED2	PLED-H314A	-	-
T1	BC547	-	-

Note

The TEA1041 must be soldered to the copper side of the printed-circuit board.

Switched-mode power supply battery charger control circuit

TEA1088T

FEATURES

- SMPS control circuit
  fixed frequency/duty factor regulation
  emitter drive for power switch
  current mode control
  dynamic primary current limiting
- Charge control circuit
  accurate output current setting
  fast, two stages, charge mode
  two hours fast charge protection limit
  trickle charge mode for full batteries
- Voltage control circuit
  voltage regulation for connected mains and load
- Battery monitor circuit
  accurate fully charged detection (– dV phenomenon)
  LOW-level detection and indication
  protection against faulty batteries, short or open-circuit
  data output for condition of charge processing
  very LOW stand-by current, < 10 μA

GENERAL DESCRIPTION

The TEA1088T is a control circuit which has been designed for use in a battery charger and/or monitor system. The device incorporates all the control and protection functions that are required in a switched-mode power supply used to deliver charge current. The circuit also achieves direct drive to the emitter of the SMPS power transistor.
The battery monitor circuit includes a reliable battery-full detector which controls the switch-over from fast charge to trickle charge mode and, in the discharge mode, a battery-LOW detector with two outputs for an LED or buzzer warning indicator.
Protections are provided against open-circuit, short-circuit or faulty batteries.
The device is primarily designed to control two batteries in series. The number of cells can be extended by using a tap.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1088T	16	SO16	plastic	SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_6	supply voltage	charge	5.5	-	31.0	V
I_6	supply current	charge	-	-	19	mA
I_{10}	supply current	discharge	-	-	12	mA
I_{10}	stand by current		-	-	10	µA
I_1	SMPS transistor bias current		-	–2	-	mA
V_2-V_3	saturation voltage emitter switch	I_2 = 350 mA	0.9	-	1.4	V
V_{10}	battery voltage range	2 cells	1.8	-	4.0	V
V_{11}	threshold battery LOW indication		1.17	-	1.33	V
$I_{13,14}$	LED output currents	$V_{13,14}$ = 0.5 V	21	30	39	mA
V_{10}	voltage range of battery full detection		2.3	-	4.3	V
V_{10}	threshold for full indication		-	–22	-	mV

Switched-mode power supply battery charger control circuit

TEA1088T

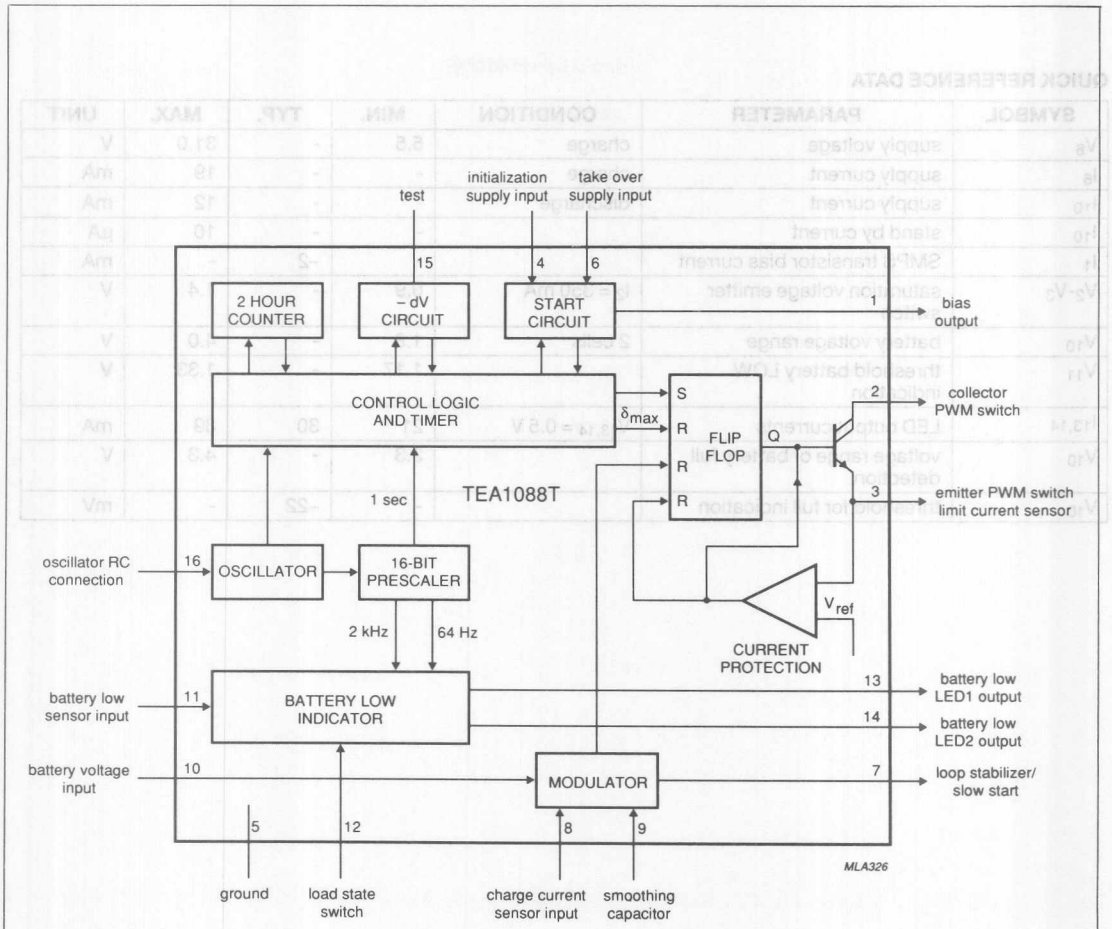


Fig.1 Block diagram.

Switched-mode power supply battery charger control circuit TEA1088T

PINNING

SYMBOL	PIN	DESCRIPTION
O2	1	bias output
O1	2	collector PWM switch
IT	3	emitter PWM switch/limit current sensor
V_{IC}	4	initialization supply input
GND	5	ground
V_{AT}	6	take over supply input
MI	7	loop stabilizer/slow start
I_{IN}	8	charge current sense input
V_{IN}	9	"V_{AC}" smoothing capacitor
V_{AC}	10	battery voltage input
BLI	11	battery LOW sense input
LS	12	load state switch
L1	13	battery LOW LED1 output
L2	14	battery LOW LED2 output
TEST	15	test pin
OSC	16	oscillator RC connection

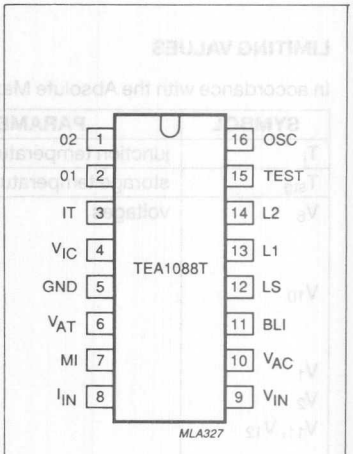


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The pin description of the device refers to external components as illustrated in the test circuit diagram (Fig.9). In this circuit the TEA1088T directly drives the emitter of the SMPS Darlington power transistor to provide fast switching and a wide reverse bias SOAR.
The supply output characteristics are shown in Fig.4 and the operational cycles of the charger system are shown in Fig.5.

The battery monitor circuit includes a reliable battery-full detector which controls switch-over from the fast charge to the trickle charge mode. The battery-full detector employs the phenomenon of an increase in battery voltage during charge due to the conversion of charge current into stored energy and, when the battery is full, a slight decrease in voltage due to a negative temperature coefficient when the charge current is only dissipative.
During charging the battery voltage is carefully sampled every second, the SMPS is then stopped to prevent interference. When a reducing voltage, –dV, is measured in succession the detector circuit sets the trickle charge mode.

In the discharge mode the battery LOW detector monitors the battery voltage and an output is given when the voltage drops below a set value. The output signals on the L1 and L2 pins are given in Figure 6. The device can also be employed purely as a monitor, this is because the monitor circuit is separate from the charge circuit. Figure 8 gives an application example.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134); voltage with respect to O V.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_j	junction temperature		–25	+125	°C
T_{stg}	storage temperature range		–25	+125	°C
V_6	voltages	continuous	–2.0	31	V
		peak during 100 ms; non-repetition	-	45	V
V_{10}		continuous	-	4.0	V
		peak during 2 µs; 50 ms repetition	-	12	V
V_1			–5.0	15	V
V_2		I_2 = 0 mA	–0.5	30	V
V_{11}, V_{12}			–0.5	4.0	V
		V_{10} < 4 V	–0.5	V_{10} +0.3	V
V_8			–0.5	0.5	V
V_{13}, V_{14}			–0.5	10	V
I_2, I_3	currents	continuous	0	350	mA
		peak 1 µs	0	1.0	A
I_8,I_9,I_{11}			-	2.0	mA
I_{13}			-	10	mA
I_{14}	battery LOW LED1 output		-	50	mA
P_{tot}	total power dissipation	Fig.3	-	500	mW

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	90	K/W

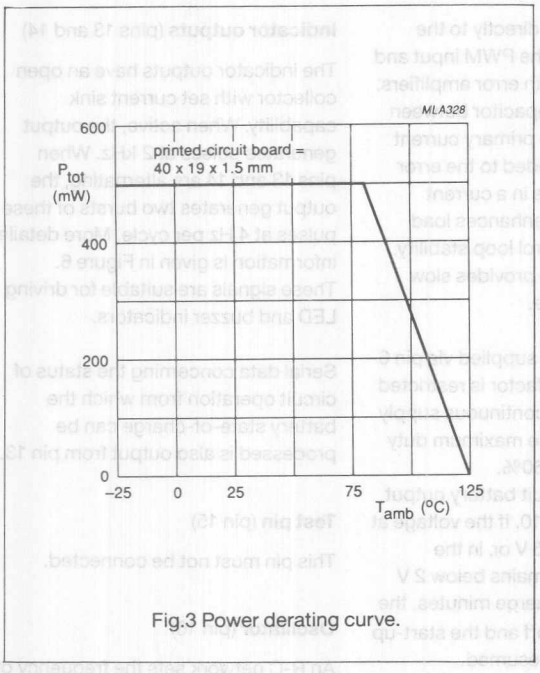


Fig.3 Power derating curve.

Supply (pins 4 and 6)

Pin 6 is the main supply input for the device if it is employed as a battery charger. It can be fed from a DC or AC voltage source; the latter can be provided by a SMPS transformer winding. The positive value of an AC voltage has to be between 7 and 31 V (45 V peak) while the negative value is restricted to –2 V.

Internally, the main supply voltage is series regulated to approximately 6 V which is available at pin 4 for connection of a smoothing capacitor. Initialization is also accomplished via pin 4 by pre-charging the capacitor up to 7.5 V via a resistor from the system power source. At the start of system operation the supply on pin 6 must take over.

When the voltage at pin 4 drops below 3.9 V the circuit switches off and restart occurs via initialization.

Output stage (pins 1, 2 and 3)

The PWM output stage consists of a Darlington power transistor with the collector and emmitter connected to pins 2 and pin 3 respectively. The current capability is 500 mA peak. This transistor drives a Darlington high voltage transistor switch directly at its emitter to ensure a large reverse bias SOAR and fast switching. The base of the Darlington high voltage transistor is biased by a current source (>1 mA) from pin 1 in combination with an external Zener diode and capacitor (pre-charged at initialization) in order to provide a low impedance base path during switching.

Dynamic primary current limit (cycle-by-cycle) (pin 3)

The primary switching current is sensed across an external resistor connected to the emitter of the PWM output switch at pin 3. Internally, the voltage on pin 3 is compared to a reference voltage which in turn is inversely proportional to the voltage difference between V_{AT} (pin 6) and V_{AC} (pin 10). This voltage difference reflects the input voltage of the system. This method compensates for primary current overshoot variations with input voltage which are caused by internal delay in the IC and storage time in the power transistor. The voltage reference level is defined by:

$V_{ref} = 0.44 - 5 \times 10^{-3} \times V_{IN}/N$ [V]

where (N = transformer winding ratio)

If the sense voltage rises above V_{ref} then the output is terminated every cycle.

Modulator (pins 7 to 10)

The PWM is connected with two error amplifiers for regulation of the SMPS output current and voltage. Voltage regulation is enabled only when the SMPS is operative and while the batteries are loaded (pin 12 connected to ground). The current feedback input, pin 8, receives the current information from a resistor R_S in the output current loop. The voltage waveform across this resistor is negative-going but is shifted to a positive value by addition of a voltage I_8 x R8 and integration with C8. (I_8 is a reference current from pin 8). This feedback voltage is compared and regulated to the common potential, the output current is defined by:
$I_O = R9/R_S$.
The value of the reference current I_8 depends on the operational state set by the control block which distinguishes:

- First 17 minutes of charge I_8(typ.) = 40 µA (2C)
- Proceeding charge = 20 µA (1C)
- Trickle charge (on/off = 1/9) = 20 µA (0.1C)
- Current limit at voltage regulation = 46 µA

In the voltage regulation mode the battery output voltage is sensed at pin 10. Internally, this voltage is divided by two and made available at pin 9, for smoothing purpose only, and compared with a 1.25 V reference voltage.

Pin 7 is connected directly to the summing point of the PWM input and the output from both error amplifiers. By connecting a capacitor between pin 7 and pin 3, the primary current sense voltage is added to the error signal which results in a current mode control that enhances load response and control loop stability. This capacitor also provides slow start at a start cycle.

When the device is supplied via pin 6 the minimum duty factor is restricted to 3% to ensure a continuous supply from the SMPS. The maximum duty factor is limited to 60%.
Open or short-circuit battery output is detected via pin 10. If the voltage at pin 10 rises above 5 V or, in the charging mode, remains below 2 V during the first 4 charge minutes, the circuit will switch off and the start-up procedure will be resumed.

Load identification (pin 12)

The switch input recognizes a load connected to the output by the state of switch S1. The difference between a closed switch or an open switch with short-circuit or flat batteries is identified if the external resistance value of R11 + R12 is greater than 4.2 kΩ.

Battery LOW sense (pin 11)

In the battery discharge mode the battery voltage is protected at pin 11 via a resistor divider. The input is immune to any spurious interference from the load. When the voltage level drops below 1.25 V the indicator output at pin 13 is set. At load switch OFF (S1 open) the indicator outputs (pin 13 and pin 14) will give alternating bursts for 4 seconds.

Indicator outputs (pins 13 and 14)

The indicator outputs have an open collector with set current sink capability. When active, the output generates pulses at 2 kHz. When pins 13 and 14 are alternating, the output generates two bursts of these pulses at 4 Hz per cycle. More detailed information is given in Figure 6. These signals are suitable for driving LED and buzzer indicators.

Serial data concerning the status of circuit operation from which the battery state-of-charge can be processed is also output from pin 13.

Test pin (pin 15)

This pin must not be connected.

Oscillator (pin 16)

An R-C network sets the frequency of the oscillator. The switching frequency of the SMPS and all the internal timing is derived from this oscillator which should be nominally 33 kHz. The capacitor is charged via pin 16 (flyback) and discharged by the parallel resistor. The required frequency is set with R = 36 kΩ and C = 560 pF.

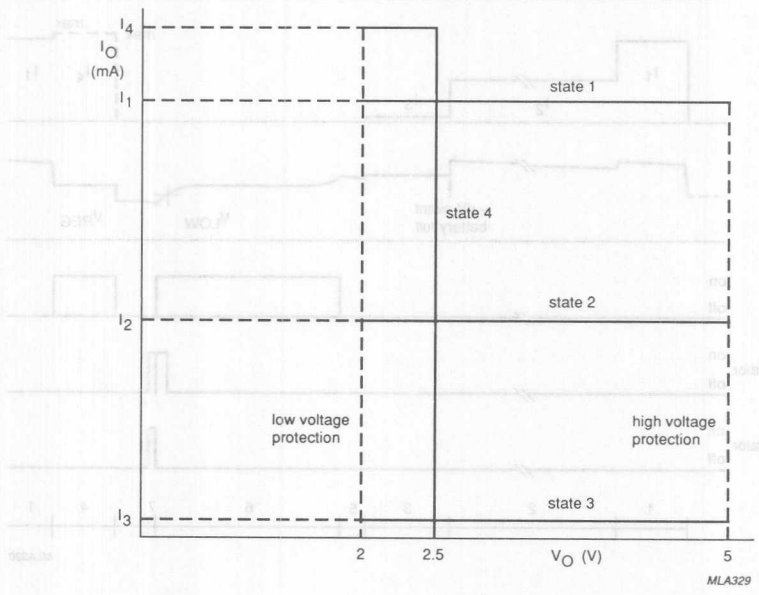
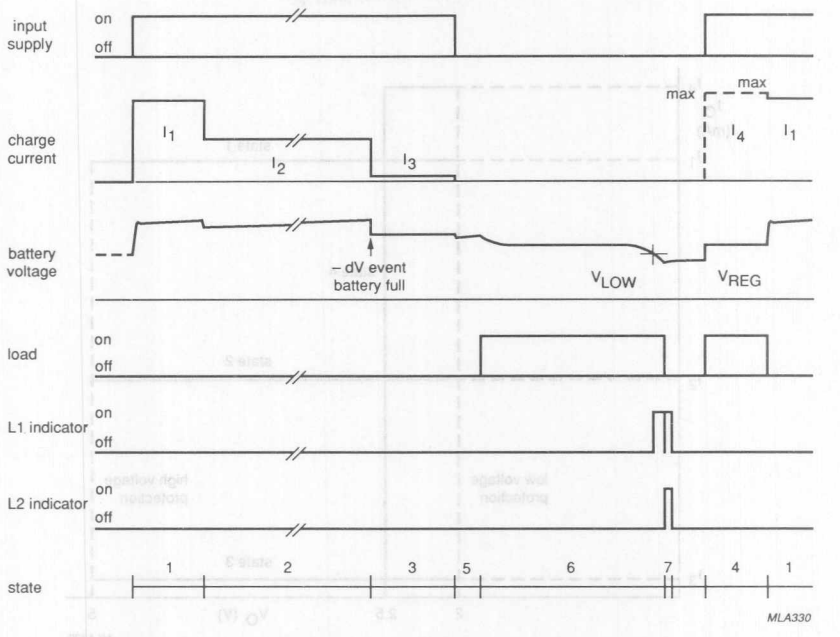


Fig.4 Supply output characteristics.



State 1; Boost charge. $I_1 = 2 \times I_2$
State 2; Fast charge.
$I_2 = (20 \times 10^{-6}) \times R8/R_S$.
State 3; Trickle charge. $I_3 = 0.1 \times I_2$
(i.e. I_2 pulsed with 10% duty factor at 1 Hz rate.
State 4; Voltage regulation.
$V_O = 2.5$ V; $I_{O(max)} = 2.3 \times I_2$.

Fig.5 Operational cycles of the SMPS charger system.

State 1; Boost charge current during 17 minutes after supply turn on. The current I_1 is twice the fast charge current I_2. This state helps completely empty batteries, possibly reversed in polarity, to quickly regain their charge store potential. Within the first 4 charge minutes the battery voltage should rise above 2 V otherwise protection occurs by stop and initialization in repeating succession.

State 2; Fast charge current that proceeds until either battery full is detected (–dV) or a maximum charge time of 2 hrs is reached.

State 3; Trickle charge which keeps the batteries fully charged. This current is sufficiently low not to harm the batteries when maintained for a long period.

State 4; Output voltage regulation when both the charger is on and a load is applied to the batteries. This provides direct output power to the load even when the batteries are empty.

State 5; Stand-by at neither input nor output. Negligible IC current (to keep the internal memories active) is drawn from the batteries.

State 6; Discharge of the batteries. The monitor circuit is activated and senses the battery voltage. Signal output (L1) is given when the sense voltage drops below a set value (V_{LOW}).

State 7; By removing the load after state 6, both indicator outputs give signals in an alternating mode for 4 seconds (see also Fig.6).

CHARACTERISTICS

V_6 = 10 V; V_{10} = 2.5 V; R16 = 36 kΩ; C16 = 560 pF; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_6	take over supply		5.5	-	31.0	V
I_6	supply current		10	15	19	mA
V_4	initialization level		6.5	7.0	7.5	V
V_4	internal supply voltage output		5.4	6.5	6.9	V
I_4	supply current	V_6 = 0 V	6.5	9.5	12.5	mA
I_{10}	input current	stand-by	-	5.0	10.0	µA
		battery discharge	6.0	9.0	12.0	mA
		BLI blinking	7.0	10.5	14	mA
		count 2 hr timer	4.9	7.8	10.8	mA
		charging	0.3	0.5	0.7	mA
Protection circuits						
V_4	LOW supply protection		3.0	3.5	3.9	V
V_{10}	minimum input voltage	charge period > 4 min.	1.8	2.0	2.2	V
V_{10}	maximum input voltage		4.5	5.0	5.5	V
Oscillator (supplied via V_4 or V_{10} = V_P)						
V_{16}	voltage level HIGH		-	4/5 V_P	-	V
V_{16}	voltage level LOW		-	1/5 V_P	-	V
	initial accuracy excluding external components	V_4 = 5.7 V	−10.0	-	+10.0	%
Δf	frequency deviation	V_4 to V_{10} supply	-	1.5	3.0	%
f	frequency	R = 36 kΩ; C = 560 pF	-	33.0	-	kHz
TC_f	temperature coefficient of frequency		-	−150	-	10^{-6}/°C
BLI function						
V_{10}	input voltage range		1.8	-	4.0	V
V_{11}	BLI reference voltage		1.17	-	1.33	V
TC_{ref}	temperature coefficient reference		−250	-	+250	10^{-6}/°C
ϕ	hysteresis reference voltage output		2.0	3.5	6.0	mV
$I_{13,14}$	BLI output current	V_O = 0.5 V	21	30	39	mA
I_{13}/I_{14}	output currents match		0.9	1.0	1.1	mA
$V_{13,14}$	saturation voltage	I_O = 10 mA	-	-	200	mV
$I_{13,14}$	leakage current	V_O = 4 V	-	-	10	µA
V_{13}	breakdown voltage	I_O = 10 mA	15.0	17.0	18.5	V
V_{14}	breakdown voltage	I_O = 50 mA during burst	15.0	17.0	18.5	V
$f_{13,14}$	frequency output signal		-	2	-	kHz
$f_{13,14}$	burst frequency	load switch off	-	1	-	Hz
$f_{13,14}$	alternating frequency	load switch off	-	4	-	Hz
−dV detector						
V_{10}	minimum input level		-	2.3	2.5	V
V_{10}	maximum input level		4.0	4.3	-	V
$-dV_{10}$	detector threshold		15	22	30	mV
t_m	sampling time		-	1	-	ms
t_{rep}	sampling repetition		-	1	-	s

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SMPS outputs						
I_1	bias output		1.0	2.0	4.0	mA
V_2-V_3	saturation voltage	I_2 = 350 mA	0.9	-	1.4	V
V_3	current protection threshold voltage	V_6-V_{10} = 3 V	340	425	510	mV
		V_6-V_{10} = 22 V	262	328	394	mV
t_p(V2)	minimum output pulse	V_6-V_{10} > 25 V	0.3	0.6	1.6	µs
t_d	current trip delay to output	V_3 = 1.2 x $V_{threshold}$	-	0.6	-	µs
Modulator						
V_{10}	reference level	voltage regulation	2.4	2.55	2.7	V
TC	temperature coefficient $V_{reference}$		-	+25	-	10^{-6}/°C
I_8	reference input current	fast charge	−10	−20	−30	µA
		boost charge	−20	−40	−60	µA
		voltage regulation	−26	−46	−69	µA
	ratio reference current	boost/fast charge	1.9	2.0	2.1	
		voltage regulator/ boost charge	1.09	1.15	1.21	
V_8	reference level	current regulation	−10	-	+10	mV
I_7	PWM input source current	voltage level HIGH	−6.5	−10.0	−13.5	µA
	PWM input sink current	voltage level LOW	6.5	10.0	13.5	µA
V_7	maximum PWM input voltage	slow start	-	0.8 x V_4	-	V
d	maximum duty factor		55	60	65	%
Periods						
t_{inh}	inhibit time of −dV circuit	start boost charge	-	4.3	-	min
		start fast charge	-	4.3	-	min
t_{bc}	boost charge duration		-	17	-	min
t_{fc}	maximum fast charge time		-	2.1	-	hr
Computer control interface						
I_{13}	status indication current source at L1		−490	−820	−1150	µA

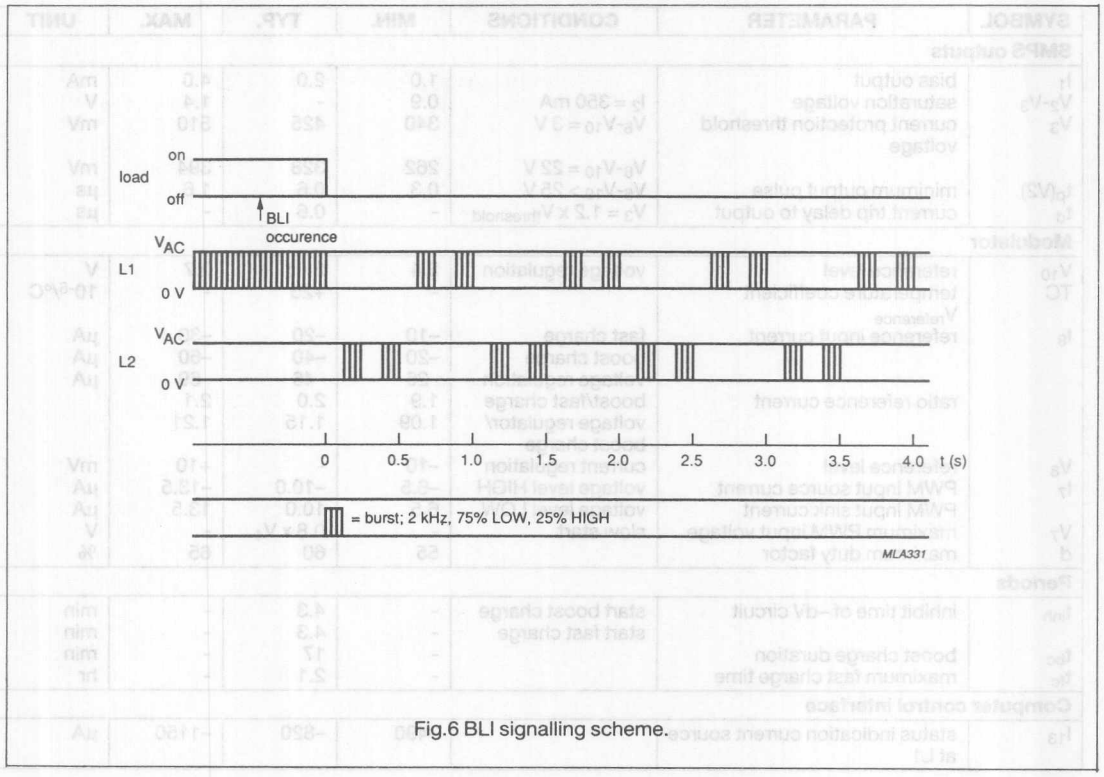


Fig.6 BLI signalling scheme.

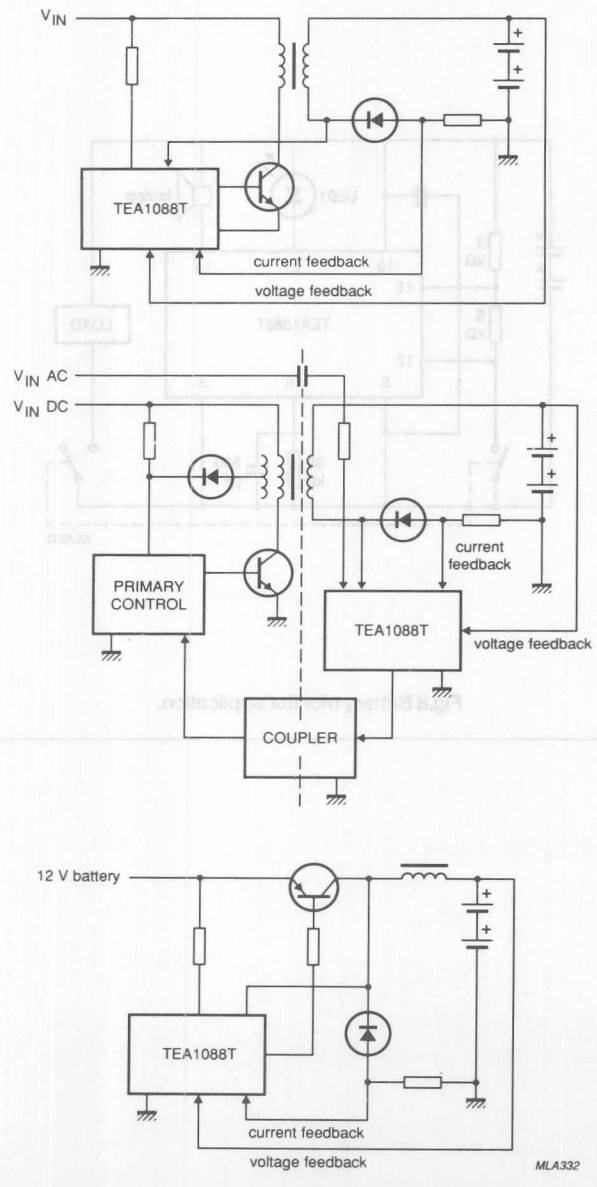


Fig.7 Simplified charger configurations.

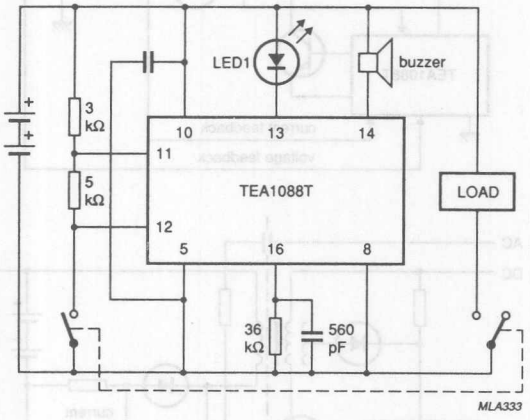


Fig.8 Battery monitor application.

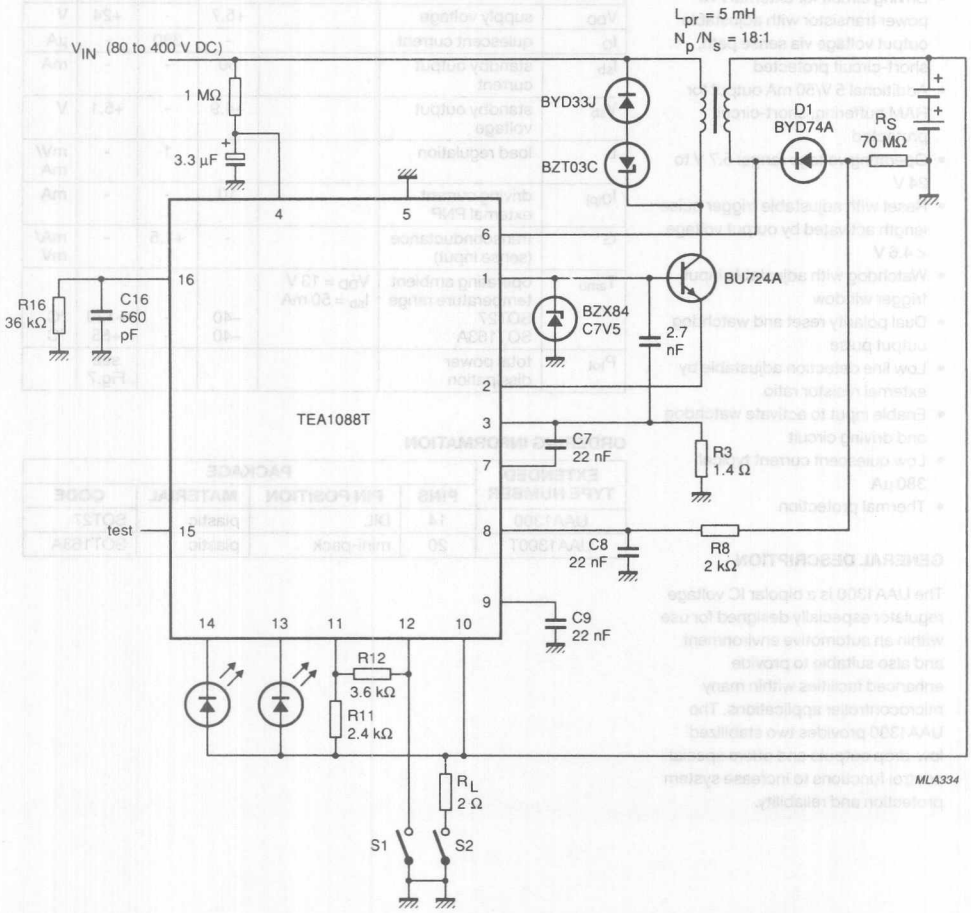


Fig.9 Test circuit.

Note

1. $I_{charge} = I_{ref} \times (R8/R_S)$

With I_{ref} = 20 µA, R8 = 2 kΩ and R_S = 70 MΩ, the charge current level is 570 mA which is approximately 1C for 'half sub C' cells.

Voltage regulator with watchdog for microprocessor/controller systems

UAA1300

FEATURES

- Driving circuit for external PNP power transistor with adjustable output voltage via sense path, short-circuit protected
- Additional 5 V/50 mA output for RAM buffering, short-circuit protected
- Operating voltage range: 5.7 V to 24 V
- Reset with adjustable trigger pulse length activated by output voltage < 4.6 V
- Watchdog with adjustable input trigger window
- Dual polarity reset and watchdog output pulse
- Low line detection adjustable by external resistor ratio
- Enable input to activate watchdog and driving circuit
- Low quiescent current typical: 380 µA
- Thermal protection

GENERAL DESCRIPTION

The UAA1300 is a bipolar IC voltage regulator especially designed for use within an automotive environment and also suitable to provide enhanced facilities within many microcontroller applications. The UAA1300 provides two stabilized low-drop outputs and offers special control functions to increase system protection and reliability.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		+5.7	-	+24	V
I_Q	quiescent current		-	380	-	µA
I_{sb}	standby output current		50	-	-	mA
V_{sb}	standby output voltage		+4.9	-	+5.1	V
L	load regulation		-	1	-	mV/mA
$I_{O(p)}$	driving current external PNP		10	-	-	mA
G	transconductance (sense input)		-	+1.5	-	mA/mV
T_{amb}	operating ambient temperature range SOT27 SOT163A	V_{DD} = 13 V I_{sb} = 50 mA	 –40 –40	 - -	 +130 +85	 °C °C
P_{tot}	total power dissipation				see Fig.7	

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UAA1300	14	DIL	plastic	SOT27
UAA1300T	20	mini-pack	plastic	SOT163A

Voltage regulator with watchdog for microprocessor/controller systems

UAA1300

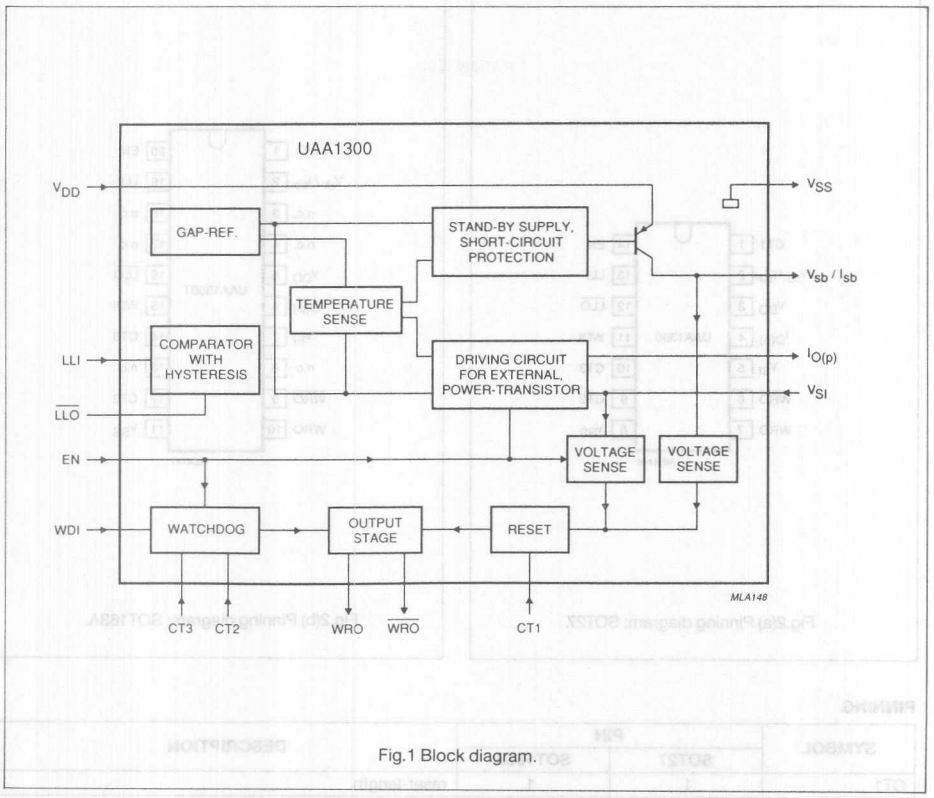


Fig.1 Block diagram.

Voltage regulator with watchdog for microprocessor/controller systems

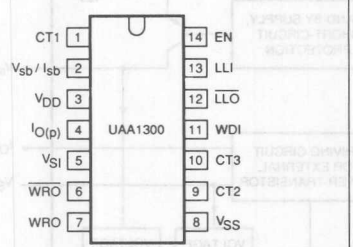


Fig.2(a) Pinning diagram; SOT27.

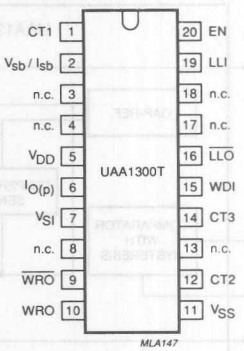


Fig.2(b) Pinning diagram; SOT163A.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT27	SOT163A	
CT1	1	1	reset-length
V_{sb}/I_{sb}	2	2	standby output: 5 V/50 mA
V_{DD}	3	5	supply voltage (line)
$I_{O(p)}$	4	6	driving current external pnp
V_{SI}	5	7	sense input external pnp
$\overline{WRO}$	6	9	watchdog reset output active LOW
WRO	7	10	watchdog reset output active HIGH
V_{SS}	8	11	ground
CT2	9	12	maximum watchdog period
CT3	10	14	minimum watchdog period
WDI	11	15	watchdog input
$\overline{LLO}$	12	16	low line output
LLI	13	19	low line input
EN	14	20	enable input

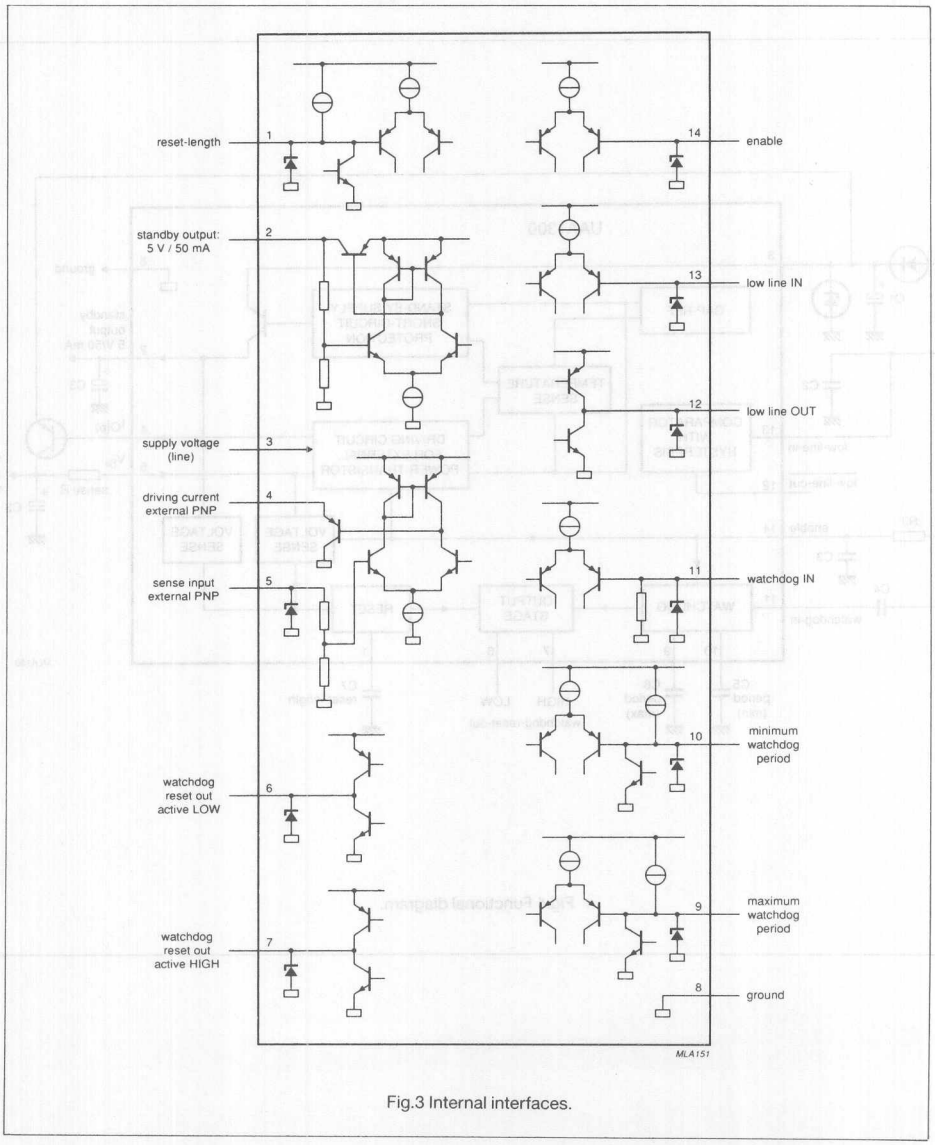


Fig.3 Internal interfaces.

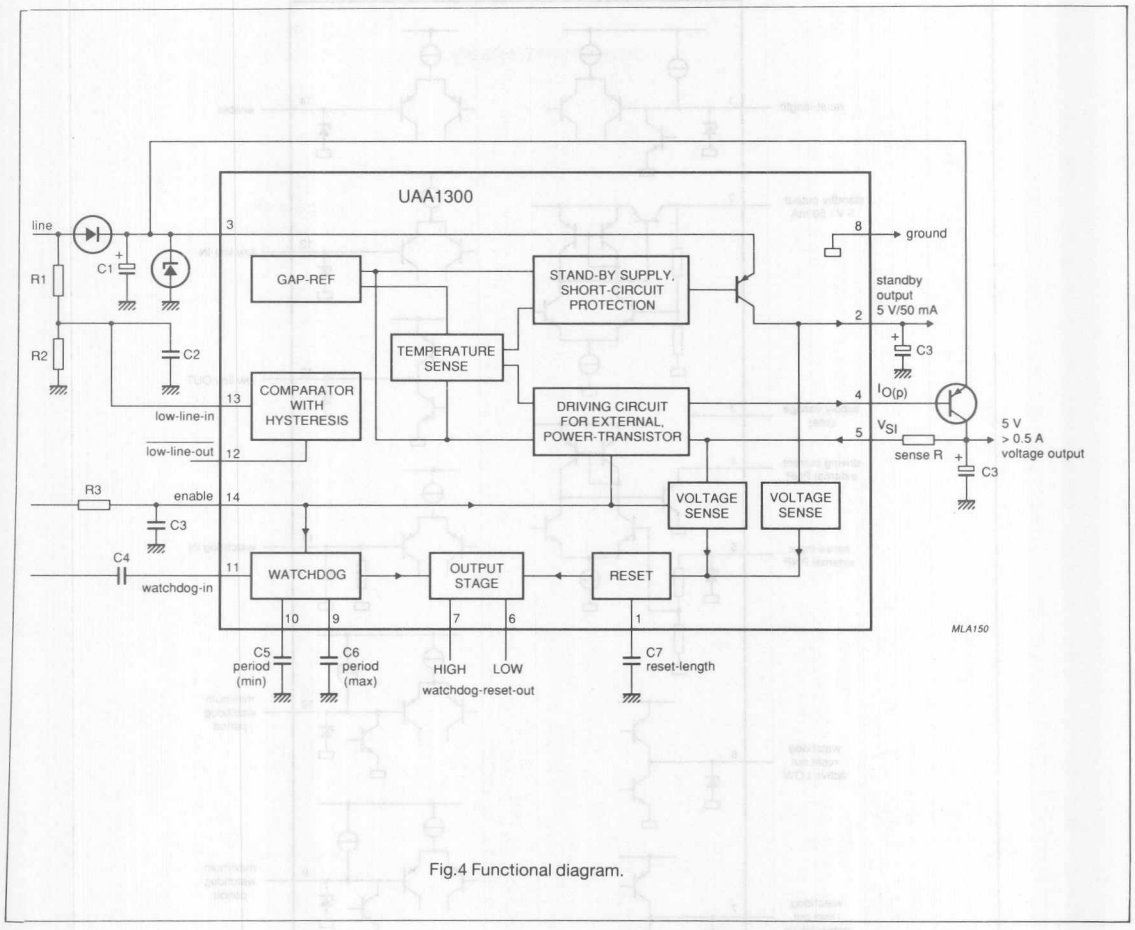


Fig.4 Functional diagram.

FUNCTIONAL DESCRIPTION

The following features of the UAA1300 are described below:

- operating voltage range
- outputs
- $\overline{WRO}$/WRO activated by low output voltage
- $\overline{WRO}$/WRO activated by WDI pulse timing
- LLI detection
- enable input
- thermal protection

Operating voltage range

The UAA1300 operates within a supply voltage range of +5.7 V to +24 V and provides reverse polarity protection and low line voltage detection.

Outputs

Two stabilized short-circuit protected; low drop outputs are provided:

Output current $I_{O(p)}$ drives an external PNP power transistor when switched on by the enable input (EN). Voltage sense input (V_{SI}) regulates the current at the external power transistor. With R = 0 Ω the voltage is 5 V ± 100 mV. Using a resistor > 0 Ω the output will be regulated to a voltage > 5 V (see Figs 4, 16, 17).

A fixed 5 V/50 mA output V_{sb}/I_{sb} supplies for example, storage circuits in microprocessor/controller systems. Not switched by enable input (EN).

$\overline{WRO}$/WRO activated by low output voltage

When either power or standby output voltage (pinning references $I_{O(p)}$, V_{sb}/I_{sb}) < 4.6 V, the watchdog output stage is triggered by a signal from the voltage sense stages and forces a static watchdog reset output pulse ($\overline{WRO}$/WRO) when both the power and standby output voltage rise above 4.7 V. The duration of the pulse width is determined by the value of external capacitor C7 (see Figs 5 and 18). To operate with external series control transistor, the watchdog function must first be switched on by the enable input (EN).

$\overline{WRO}$/WRO activated by watchdog input pulse (WDI) timing

The watchdog input pulse (WDI) from the µC/µP must be received within a time window determined by external capacitors C5 and C6. When this is not achieved the watchdog output stage generates a $\overline{WRO}$/WRO pulse with fixed width of 40 µs. Each rising edge at WDI restarts the timing cycle (see Figs 6 and 19). To operate, this watchdog function must first be switched on by the enable input (EN).

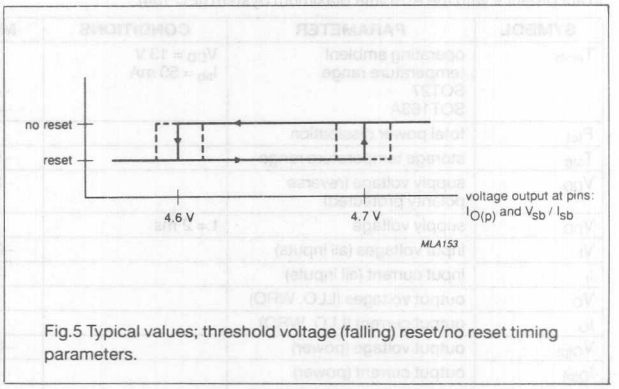


Fig.5 Typical values; threshold voltage (falling) reset/no reset timing parameters.

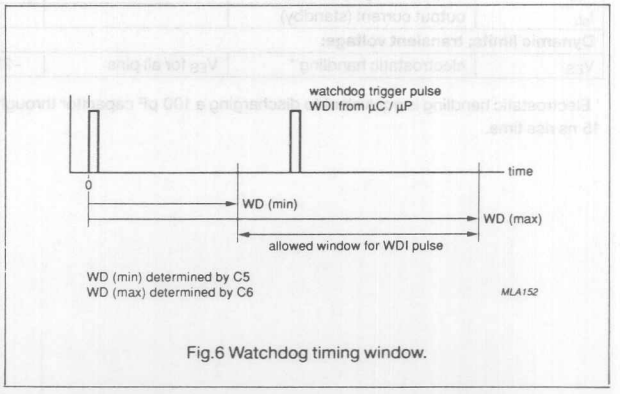


Fig.6 Watchdog timing window.

Voltage regulator with watchdog for microprocessor/controller systems

UAA1300

LLI detection

The UAA1300 provides detection for low line input (LLI).
This is achieved by use of a comparator which generates a low line output pulse ($\overline{LLO}$) on detection of a low line input voltage (LLI) < 1.24 V. When the LLI < 1.24 V it is considered LOW (V). When the LLI > 1.34 V it is considered HIGH (V). The threshold voltage is adjusted by the external resistor ratio of R1/R2.

An additional external capacitor C2 prevents an initiation of an $\overline{LLO}$ pulse which might otherwise be caused by short duration (transient) LLI voltage drops (see Fig.4).

Enable input

When the Enable input (EN) is > 2 V the driving circuit for the external power transistor is switched on and the watchdog functions are activated.

Thermal protection

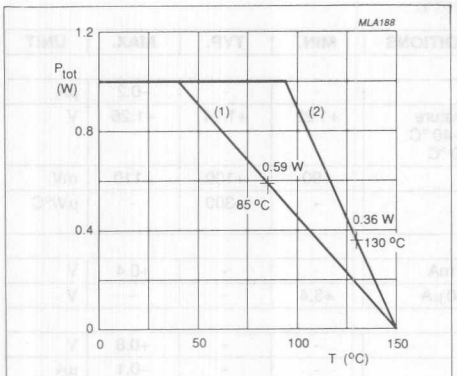
Outputs (pinning references $I_{O(p)}$ and V_{sb}/I_{sb}) are controlled by an internal temperature sense switch module which operates at a crystal temperature > 150 °C switching off these outputs. The temperature sense switch resets at a crystal temperature ≤ +130 °C and switches on both outputs.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{amb}	operating ambient temperature range SOT27 SOT163A	V_{DD} = 13 V I_{sb} = 50 mA	 −40 −40	 - -	 +130 +85	 °C °C
P_{tot}	total power dissipation				see Fig.7	
T_{stg}	storage temperature range		−55	-	+150	°C
V_{DD}	supply voltage (reverse polarity protected)		−25	-	+25	V
V_{DD}	supply voltage	t = 2 ms	-	-	+30	V
V_I	input voltages (all inputs)		−0.5	-	+7	V
I_I	input current (all inputs)		−5	-	5	mA
V_O	output voltages (LLO, WRO)		-	-	+7	V
I_O	output current (LLO, WRO)		-	-	10	mA
$V_{O(p)}$	output voltage (power)		−0.5	-	V_{DD}	V
$I_{O(p)}$	output current (power)		-	-	25	mA
V_{sb}	output voltage (standby)		-	-	V_{DD}	V
I_{sb}	output current (standby)		-	-	100	mA
Dynamic limits; transient voltage:						
V_{ES}	electrostatic handling *	V_{ES} for all pins	−2000	-	+2000	V

* Electrostatic handling is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a 15 ns rise time.



(1) = SO20; SOT163A

(2) = SOT27 (IDF14)

$P_{tot} \approx (V_{DD} - 5\ V) \times I_{sb} + V_{DD} \times I_D$

Fig.7 Power derating diagram.

CHARACTERISTICS

V_{DD} = 13 V, T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range for logic functions		+4.2	-	+24	V
I_{DD}	supply current without load	input EN = LOW	-	380	-	µA
T_{amb}	operating ambient temperature range		−40	-	+130	°C
Standby output						
V_{sb}	output voltage	V_{DD} min = +5.7 V	+4.9	+5	+5.1	V
I_{sb}	current capability		−50	-	-	mA
L	load regulation		-	-	1	mV/mA
TC_{sb}	temperature coefficient of output voltage		-	±400	-	µV/°C
RR	ripple rejection	f = 100 Hz	-	50	-	dB
Reference for external pnp-transistor						
I_O	current capability		10	-	-	mA
V_O	limits for external voltage		+5	-	V_{DD}	V
G	transconductance (sense input)		0.4	1.5	-	mA/mV
I_S	sense current	V_{SI} = +5V	37.5	50	62.5	µA
R_S	input resistance		75	100	125	kΩ
Temperature sense						
δS	threshold for rising temperature		-	+150	-	°C
δΔ	hysteresis of temperature sense		-	+30	-	°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Low-line detection						
$I_{LLI/LOW}$	input current LOW		-	-	−0.2	µA
V_{THL}	threshold voltage for falling voltage	temperature range −40 °C to +130 °C	+1.22	+1.24	+1.26	V
V_{THU}	hysteresis		+90	+100	+110	mV
T_C	temperature coefficient for hysteresis		-	+300	-	µV/°C
Low-line output						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	-	-	+0.4	V
V_{OH}	output voltage HIGH	I_{OH} = 50 µA	+3.4	-	-	V
Enable input						
V_{IL}	enable input voltage LOW		-	-	+0.8	V
I_{IL}	enable input current LOW		-	-	−0.1	µA
V_{IH}	enable input voltage HIGH		+2	-	-	V
Watchdog input						
V_{LW}	watchdog input voltage LOW		-	-	+0.8	V
I_{LW}	watchdog input current LOW		-	-	−0.2	µA
V_{HW}	watchdog input voltage HIGH		+2	-	-	V
Z_I	input impedance		28	50	72	kΩ
t_{WDI}	minimum input pulse length		40	-	-	µs
Minimum and maximum Watchdog Period						
I_{WD}	output current (pin shorted to ground)		−1	−1.25	−1.50	µA
t_{CIWD}	temperature coefficient of output current		-	−0.6	-	‰/°C
V_{TH}	threshold for internal comparator		-	+1.24	-	V
Timing of watchdog function Range of useful external film-capacitors: 100 pF to 1 µF (C5/C6)						
t_{WP}	watchdog minimum period	C5 = 100 pF	70	100	130	µs
t_{WP}	watchdog maximum period	C6 = 1 µF	700	1000	1300	ms
t_{WDO}	duration of the watchdog output pulse		25	40	55	µs
Reset function: timing						
t_{RO}	duration of the reset pulse	C7 = 100 pF	-	100	-	µs
t_{RO}	duration of the reset pulse	C7 = 100 nF	-	100	-	ms
Reset function: DC conditions						
V_{th}	threshold voltage (falling) for reset on		4.5	4.6	4.7	V
δ	hysteresis		-	100	-	mV
T_C	temperature coefficient of hysteresis		-	100	-	µV/°C

TEST VALUES, ADJUSTMENTS AND APPLICATION EXAMPLE

The following figures (Figs 8 to 19) provide a test circuit, typical test values and voltage and timing adjustments. Figure 20 provides an application example for automotive environment.

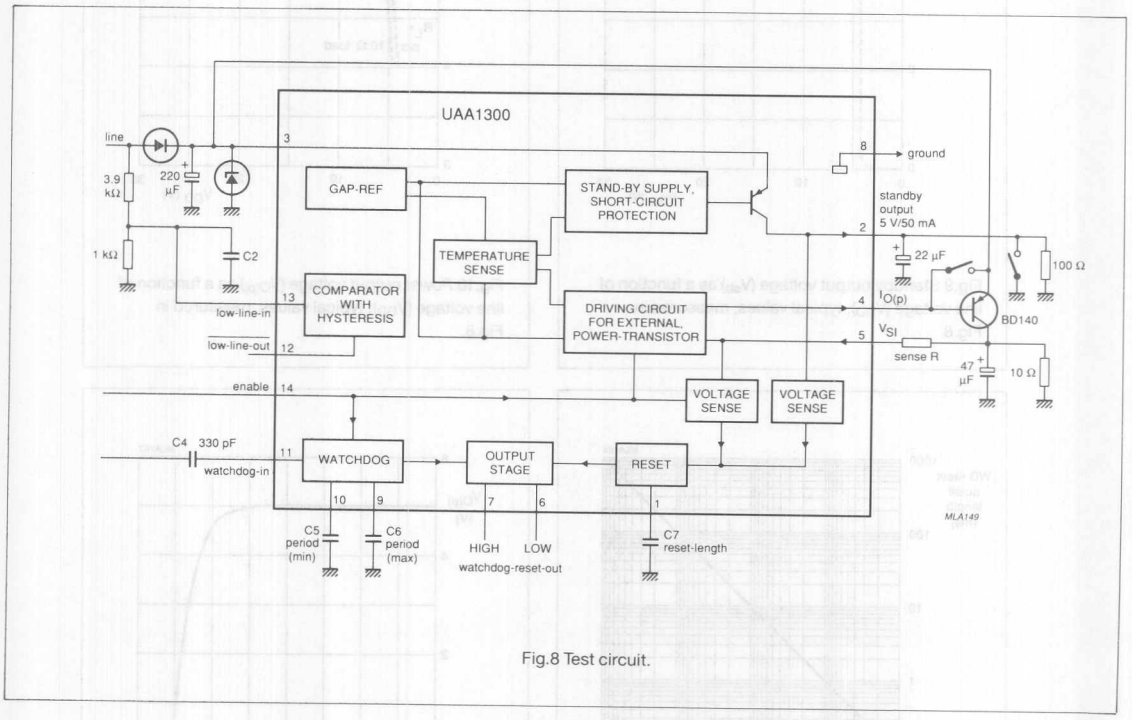


Fig.8 Test circuit.

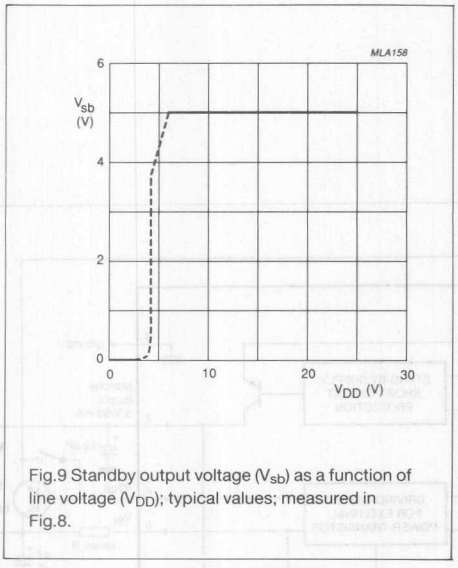


Fig.9 Standby output voltage (V_{sb}) as a function of line voltage (V_{DD}); typical values; measured in Fig.8.

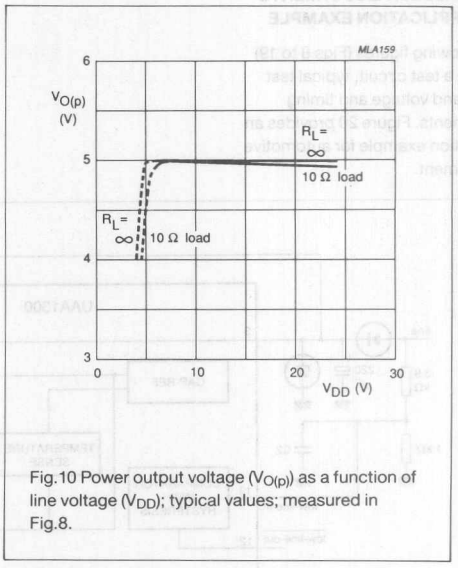


Fig.10 Power output voltage ($V_{O(p)}$) as a function of line voltage (V_{DD}); typical values; measured in Fig.8.

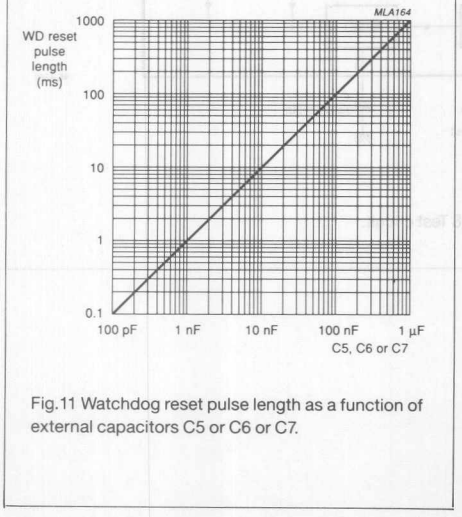


Fig.11 Watchdog reset pulse length as a function of external capacitors C5 or C6 or C7.

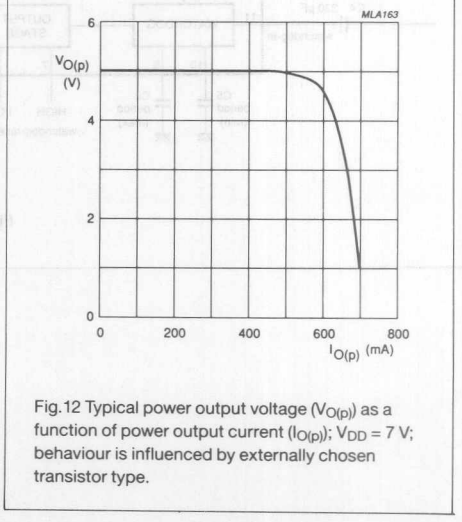


Fig.12 Typical power output voltage ($V_{O(p)}$) as a function of power output current ($I_{O(p)}$); V_{DD} = 7 V; behaviour is influenced by externally chosen transistor type.

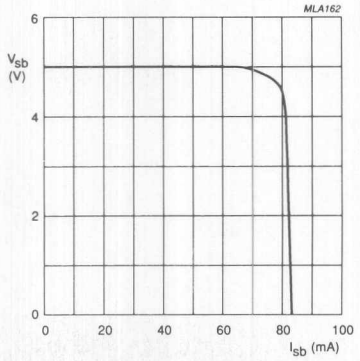


Fig.13 Typical standby output voltage (V_{sb}) as a function of standby output current (I_{sb}); V_{DD} = 7 V.

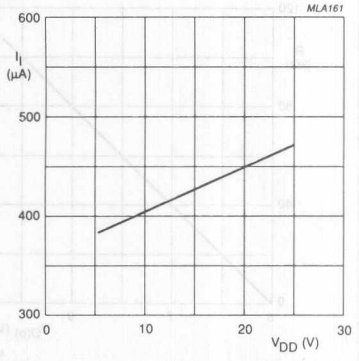


Fig.14 Quiescent current (I_I) as a function of line voltage (V_{DD}); no load at standby output voltage (V_{sb}); enable (EN) not active.

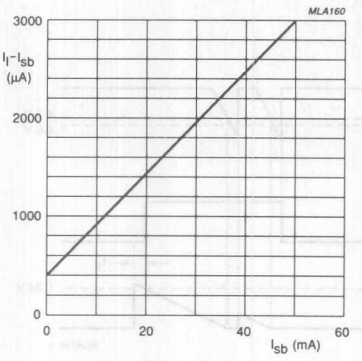


Fig.15 Quiescent current (I_I) minus standby output current (I_{sb}) as a function of standby output current (I_{sb}); V_{DD} = 13 V.

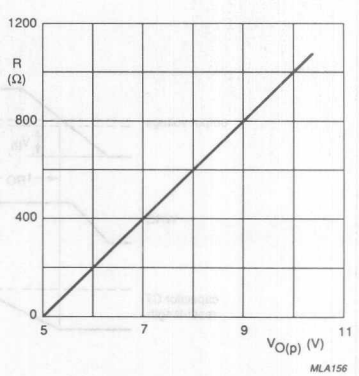


Fig.16 Adjustment of power output voltage ($V_{O(p)}$); typical values of external adjustment resistors: circuit with high accuracy.

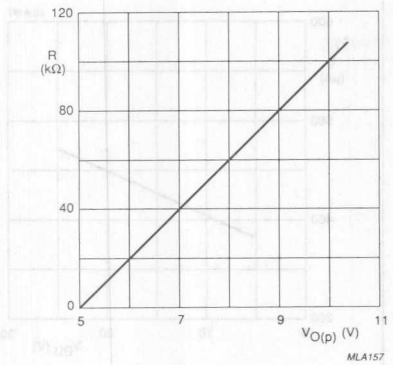


Fig.17 Adjustment of power output voltage ($V_{O(p)}$); typical values of external adjustment resistors: circuit with less accuracy but reduced current consumption of the application.

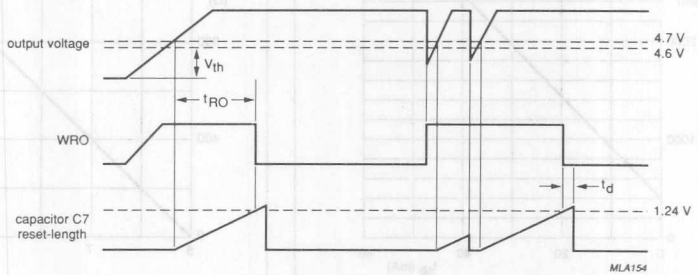
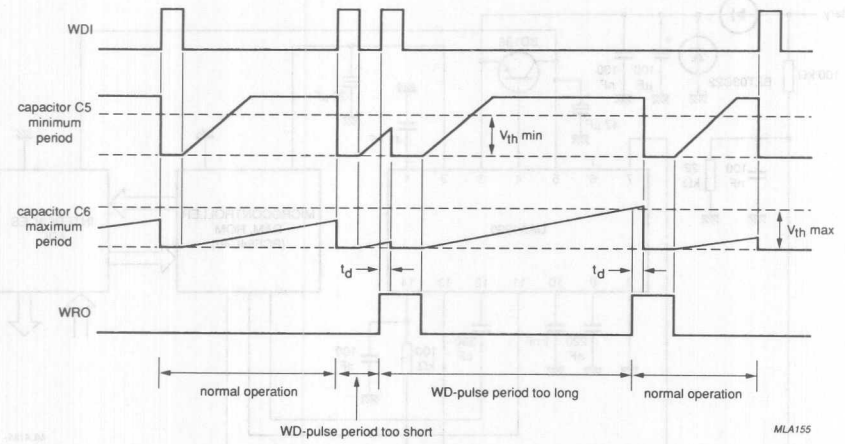


Fig.18 Reset behaviour: watchdog reset output (WRO) timing as a function of output voltage (power $V_{O(p)}$ or standby V_{sb}) with external capacitor C7 as a parameter.



V_{th}min = threshold voltage for WD(min)

V_{th}max = threshold voltage for WD(max)

t_d = internal delay

normal operation: V_{th}min must already be achieved

V_{th}max must not be achieved

if these conditions are not present a WDI pulse will force a $\overline{WRO}$/WRO pulse at the output stage

Fig.19 Reset behaviour: watchdog reset output (WRO) timing as a function of watchdog input (WDI) with external capacitors C5 and C6 as parameters.

APPLICATION INFORMATION

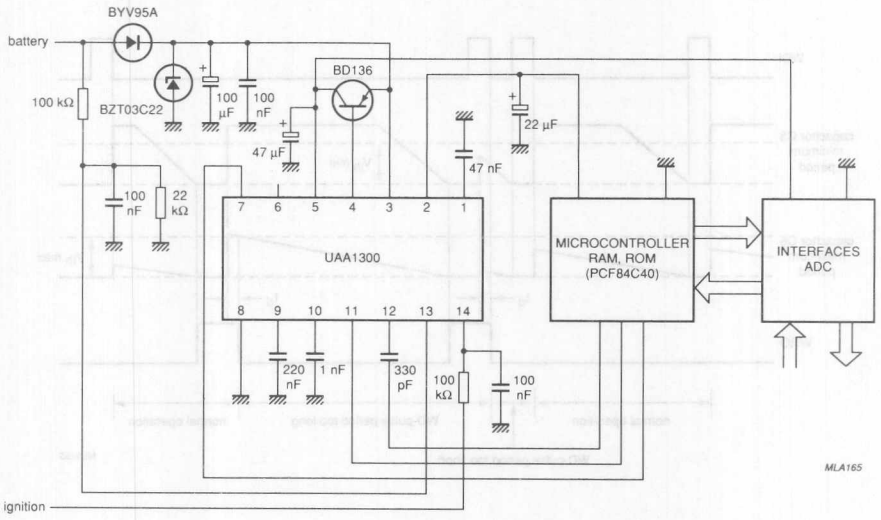


Fig.20 Application example for automotive environment.

Section 14
Switched-Mode Power Supply Circuits/Trigger Circuits

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Section 14
Switched-Mode Power Supply Circuits/Trigger Circuits

General Purpose/Linear ICs

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Switched-mode power supply control circuit NE/SE5560

DESCRIPTION

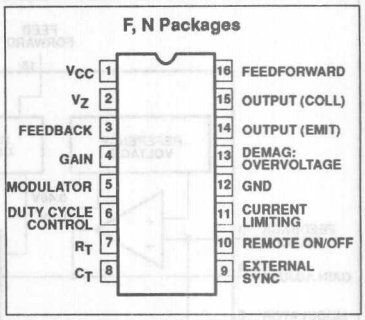
The NE/SE5560 is a control circuit for use in switched-mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched-mode power supplies, including an internal temperature-compensated reference source, internal Zener references, sawtooth generator, pulse-width modulator, output stage and various protection circuits.

FEATURES

- Stabilized power supply
- Temperature-compensated reference source
- Sawtooth generator
- Pulse-width modulator
- Remote on/off switching
- Current limiting
- Low supply voltage protection
- Loop fault protection
- Demagnetization/overvoltage protection
- Maximum duty cycle clamp
- Feed-forward control
- External synchronization

PIN CONFIGURATION

F, N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to 70°C	NE5560N
16-Pin Plastic Dip	-55°C to 125°C	SE5560N
16-Pin Cerdip	-55°C to 125°C	SE5560F

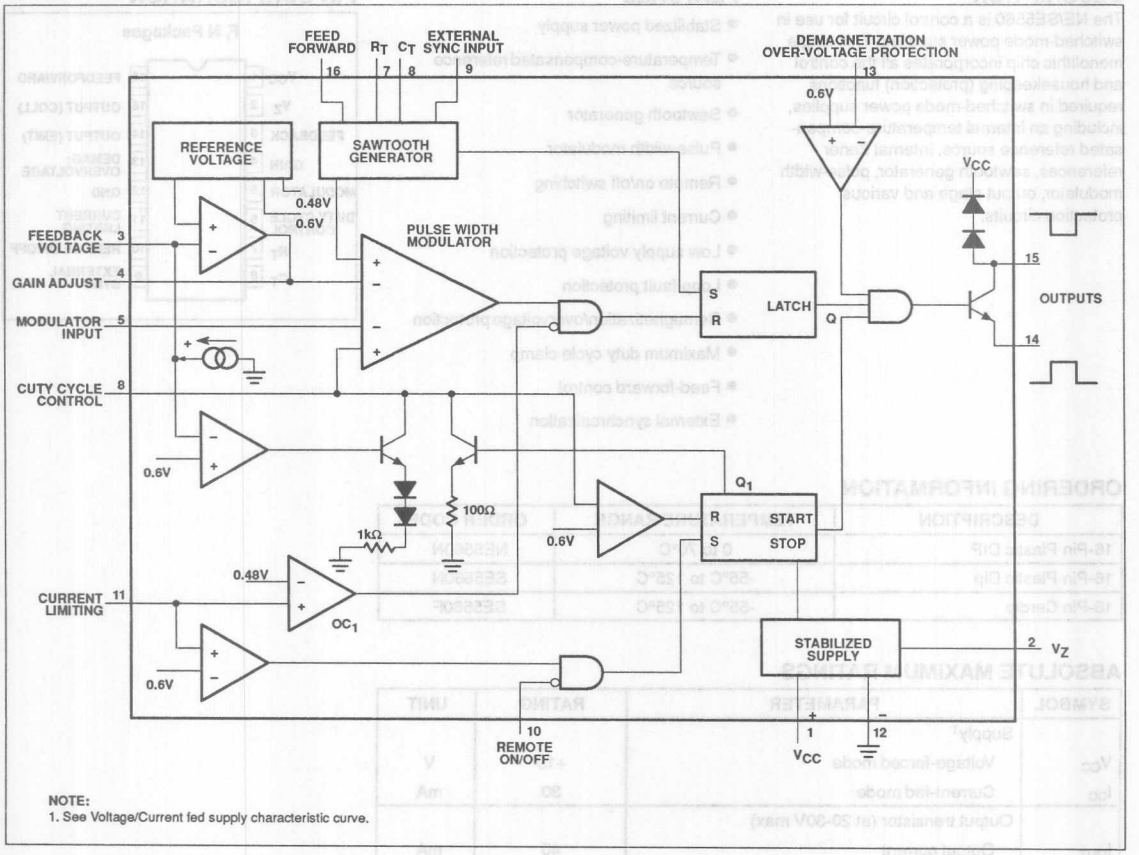
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply[1]		
V_{CC}	Voltage-forced mode	+18	V
I_{CC}	Current-fed mode	30	mA
	Output transistor (at 20-30V max)		
I_{OUT}	Output current	40	mA
	Collector voltage (Pin 15)	V_{CC}+1.4V	V
	Max. emitter voltage (Pin 14)	+5	V
T_A	Operating ambient temperature range		
	SE5560	-55 to +125	°C
	NE5560	0 to 70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:

1. Does not include current for timing resistors or capacitors.

BLOCK DIAGRAM



NOTE:
1. See Voltage/Current fed supply characteristic curve.

DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC}=12V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
			Min	Typ	Max	Min	Typ	Max	
Reference sections									
V_{REF}	Internal reference voltage	25°C	3.69	3.72	3.81	3.57	3.72	3.95	V
		Over temperature	3.65		3.85	3.53		4.00	V
	Temperature coefficient of V_{REF}			-100			-100		ppm/°C
V_Z	Internal Zener reference	I_L=-7mA	7.8	8.4	8.8	7.8	8.4	8.8	V
	Temperature coefficient of V_Z			200			200		ppm/°C
Oscillator section									
	Frequency range	Over temperature	50		100k	50		100k	Hz
	Initial accuracy oscillator	R=5kΩ		5			5		%
	Duty cycle range	f_O=20kHz	0		98	0		98	%
Modulator									
	Modulation input current	Voltage at Pin 5=2V Over temperature		0.2	20		0.2	20	µA
Housekeeping function									
I_{IN}	Pin 6, input current	At 2V							
		Over temperature		0.2	20		0.2	20	µA
	Pin 6, duty cycle limit control	For 50% max duty cycle 15kHz to 50kHz/41% of V_Z	40	50	60	40	50	60	% of duty cycle
	Pin 1, low supply voltage protection thresholds		8	9.0	10.5	8	9.0	10.5	V
	Pin 3, feedback loop protection trip threshold		400	600	720	400	600	720	mV
		At 2V							
	Pin 3, pull-up current		-7	-15	-35	-7	-15	-35	µA
	Pin 13, demagnetization/over-voltage protection trip on threshold	Over temperature	470	600	720	470	600	720	mV
		At 0.25V							
I_{IN}	Pin 13, input current	25°C		-0.6	-10		-0.6	-10	µA
		Over temperature			-20			-20	
	Pin 16, feed-forward duty cycle control	Voltage at Pin 16=2V_Z	30	40	50	30	40	50	% original duty cycle
		At 16V, V_{CC}=18V							
	*Pin 16, feed-forward input current	25°C		0.2	5		0.2	5	µA
		Over temperature			10			10	µA
External synchronization									
	Pin 9 Off		0		0.8	0		0.8	V
	On		2		V_Z	2		V_Z	V
	Sink current	Voltage at Pin 9=0V, 25°C		-65	-100		-65	-125	µA
		Over temperature			-125			-125	µA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
			Min	Typ	Max	Min	Typ	Max	
Remote									
	Pin 10 Off		0		0.8	0		0.8	V
	On		2		V_Z	2		V_Z	V
		At 0V							
	Sink current	25°C		-85	-100		-85	-125	µA
		Over temperature			-125			-125	µA
Current limiting									
I_{IN}	Pin 11 Input current	Voltage at Pin 11=250mV		-2	-20		-2	-20	µA
		25°C							
		Over temperature			-40			-40	µA
	Single pulse inhibit delay	Inhibit delay time for 20% overdrive at 40mA I_{OUT}		0.7	0.8		0.7	0.8	µs
OC_1	Trip Levels: Shut down, slow start, low level		0.500	0.600	0.700	0.500	0.600	0.700	V
OC_2	Current limit, high level		0.400	0.480	0.560	0.400	0.560	0.500	V
ΔOC	Low Level in terms of high level, OC_1		0.750	0.800	0.850	0.750	0.800	0.850	V
Error amplifier									
V_{OH}	Output voltage swing		6.2		9.5	6.2		9.5	V
V_{OL}	Output voltage swing				0.7			0.7	V
	Open-loop gain		54	60		54	60		dB
R_F	Feedback resistor		10k			10k			Ω
BW	Small-signal bandwidth			3			3		MHz
Output stage									
	V_{CE}(SAT) I_C=40mA				0.5			0.5	V
	Output current (Pin 15)		40			40			mA
	Max. emitter voltage (Pin 14)		5	6		5	6		V
Supply voltage/current[1]									
I_{CC}	Supply current	I_Z=0, voltage-forced, V_{CC}=12V, 25°C			10			10	mA
		Over temp.			15			15	mA
V_{CC}	Supply voltage	I_{CC}=10mA current-fed	20		23	19		24	V
V_{CC}	Supply voltage	I_{CC}=30mA current-fed	20		30	20		30	V

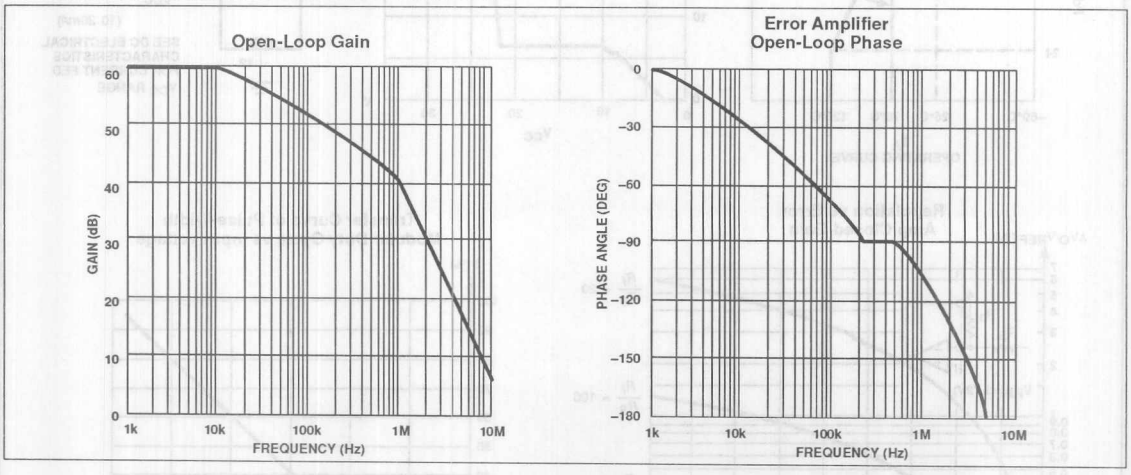
NOTES:
1. Does not include current for timing resistors or capacitors.

MAXIMUM PIN VOLTAGES

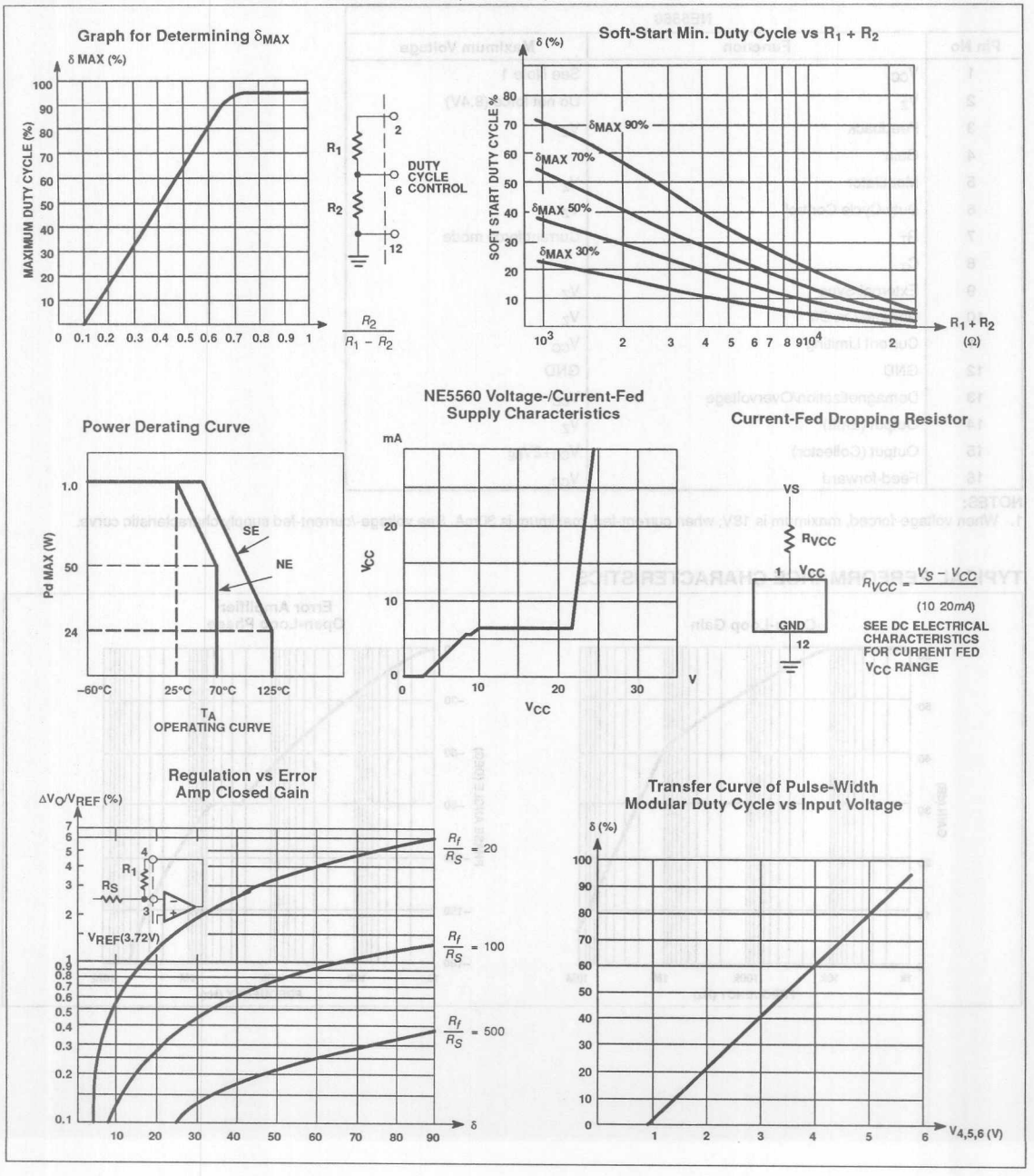
NE5560		
Pin No	Function	Maximum Voltage
1	V_{CC}	See Note 1
2	V_Z	Do not force (8.4V)
3	Feedback	V_Z
4	Gain	
5	Modulator	V_Z
6	Duty Cycle Control	V_Z
7	R_T	Current force mode
8	C_T	
9	External Sync	V_Z
10	Remote On/Off	V_Z
11	Current Limiting	V_{CC}
12	GND	GND
13	Demagnetization/Overvoltage	V_{CC}
14	Output (Emit)	V_Z
15	Output (Collector)	$V_{CC}+2V_{BE}$
16	Feed-forward	V_{CC}

NOTES:
1. When voltage-forced, maximum is 18V; when current-fed, maximum is 30mA. See voltage-/current-fed supply characteristic curve.

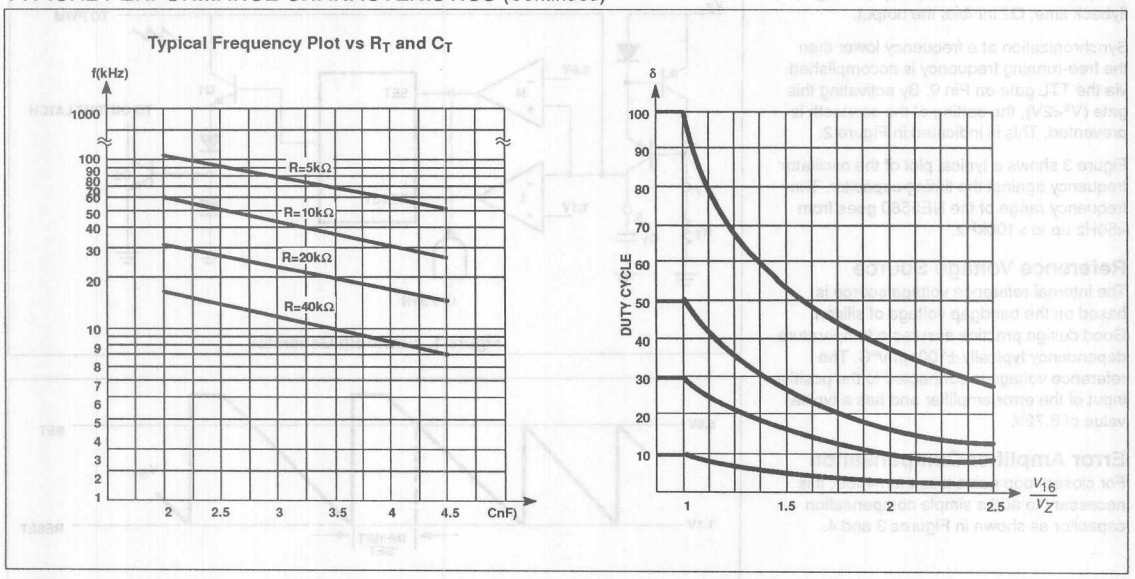
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



THEORY OF OPERATION

The following functions are incorporated:

- A temperature-compensated reference source.
- An error amplifier with Pin 3 as input. The output is connected to Pin 4 so that the gain is adjustable with external resistors.
- A sawtooth generator with a TTL-compatible synchronization input (Pins 7, 8, 9).
- A pulse-width modulator with a duty cycle range from 0 to 95%.

The PWM has two additional inputs:

Pin 6 can be used for a precise setting of δ_{MAX}

Pin 5 gives a direct access to the modulator, allowing for real constant-current operation:

- A gate at the output of the PWM provides a simple dynamic current limit.
- A latch that is set by the flyback of the sawtooth and reset by the output pulse of the above mentioned gate prohibits double pulsing.
- Another latch functions as a start-stop circuit; it provides a fast switch-off and a slow start.
- A current protection circuit that operates via the start-stop circuit. This is a combined function with the current limit circuit, therefore Pin 11 has two trip-on levels; the lower one for cycle-by-cycle current limiting, the upper one for current protection by means of switch-off and slow-start.
- A TTL-compatible remote on/off input at Pin 10, also operating via the start-stop circuit.
- An inhibit input at Pin 13. The output pulse can be inhibited immediately.
- An output gate that is commanded by the latches and the inhibit circuit.
- An output transistor of which both the collector (Pin 15) and the emitter (Pin 14) are externally available. This allows for normal or inverse output pulses.
- A power supply that can be either voltage- or current-driven (Pins 1 and 12). The internally-generated stabilized output voltage VZ is connected to Pin 2.
- A special function is the so-called feed-forward at Pin 16. The amplitude of the sawtooth generator is modulated in such a way that the duty cycle becomes inversely proportional to the voltage on this pin: $\delta \sim 1/V16$.
- Loop fault protection circuits assure that the duty cycle is reduced to zero or a low value for open- or short-circuited feedback loops.

Stabilized Power Supply (Pins 1, 2, 12)

The power supply of the NE5560 is of the well known series regulation type and provides a stabilized output voltage of typically 8.5V.

This voltage V_Z is also present at Pin 2 and can be used for precise setting of δ_{MAX} and to supply external circuitry. Its max. current capability is 5mA.

The circuit can be fed directly from a DC voltage source between 10.5V and 18V or can be current-driven via a limiting resistor. In the latter case, internal pinch-off resistors will limit the maximum supply voltage: typical 23V for 10mA and max. 30V for 30mA.

The low supply voltage protection is active when $V_{(1-12)}$ is below 10.5V and inhibits the output pulse (no hysteresis).

When the supply voltage surpasses the 10.5V level, the IC starts delivering output pulses via the slow-start function.

The current consumption at 12V is less than 10mA, provided that no current is drawn from V_Z and $R_{(7-12)} \geq 20k\Omega$.

The Sawtooth Generator

Figure 1 shows the principal circuitry of the oscillator. A resistor between Pin 7 and Pin 12 (GND) determines the constant current that charges the timing capacitor $C_{(8-12)}$.

This causes a linear increasing voltage on Pin 8 until the upper level of 5.6V is reached. Comparator H sets the RS flip-flop and Q1 discharges $C_{(8-12)}$ down to 1.1V, where

comparator L resets the flip-flop. During this flyback time, Q2 inhibits the output.

Synchronization at a frequency lower than the free-running frequency is accomplished via the TTL gate on Pin 9. By activating this gate (V^9<2V), the setting of the sawtooth is prevented. This is indicated in Figure 2.

Figure 3 shows a typical plot of the oscillator frequency against the timing capacitor. The frequency range of the NE5560 goes from <50Hz up to >100kHz.

Reference Voltage Source

The internal reference voltage source is based on the bandgap voltage of silicon. Good design practice assures a temperature dependency typically ±100ppm/°C. The reference voltage is connected to the positive input of the error amplifier and has a typical value of 3.72V.

Error Amplifier Compensation

For closed-loop gains less than 40dB, it is necessary to add a simple compensation capacitor as shown in Figures 3 and 4.

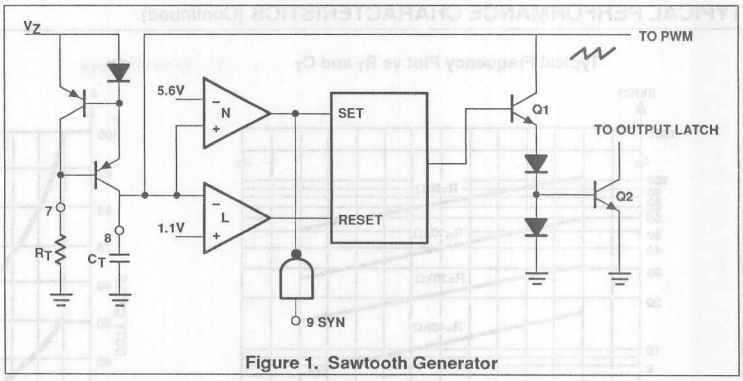


Figure 1. Sawtooth Generator

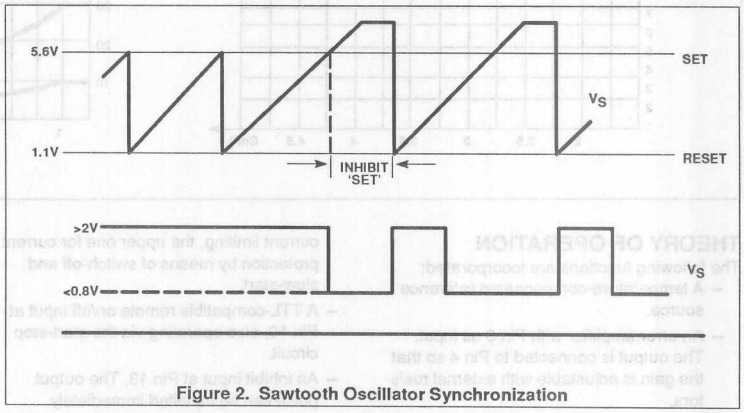


Figure 2. Sawtooth Oscillator Synchronization

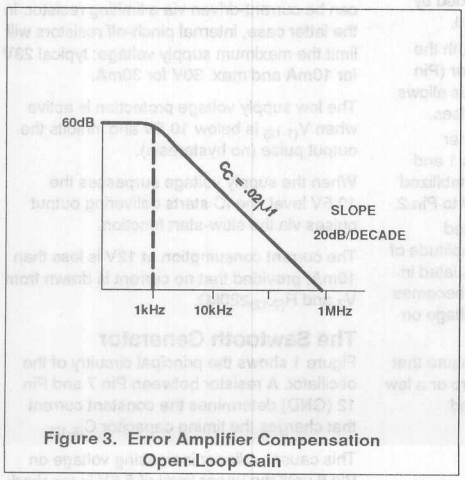


Figure 3. Error Amplifier Compensation Open-Loop Gain

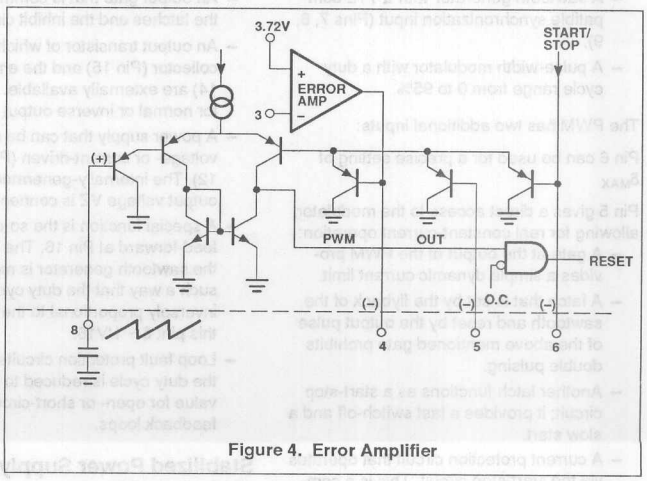


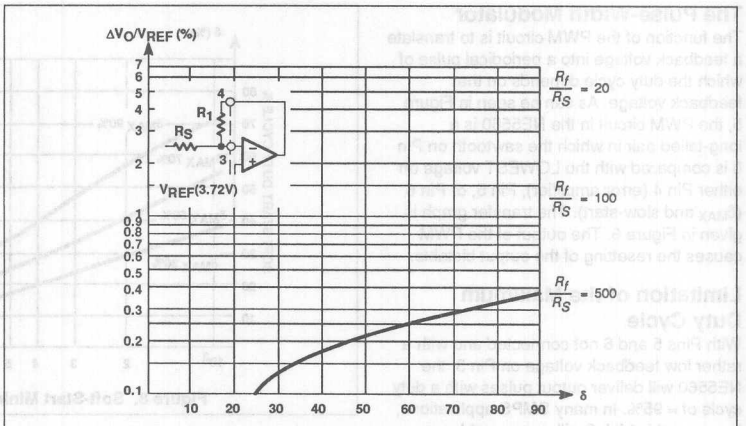
Figure 4. Error Amplifier

Error Amplifier with Loop-Fault Protection Circuits

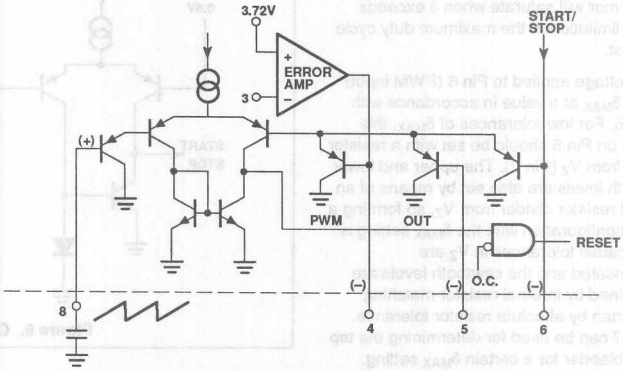
This operational amplifier is of a generally used concept and has an open-loop gain of typically 60dB. As can be seen in Figure 4, the inverting input is connected to Pin 3 for a feedback information proportional to V_O.

The output goes to the PWM circuit, but is also connected to Pin 4, so that the required gain can be set with R_S and $R_{(3-4)}$. This is indicated in Figure 4, showing the relative change of the feedback voltage as a function of the duty cycle. Additionally, Pin 4 can be used for phase shift networks that improve the loop stability.

When the SMPS feedback loop is interrupted, the error amplifier would settle in the middle of its active region because of the feedback via $R_{(3-4)}$. This would result in a large duty cycle. A current source on Pin 3 prevents this by pushing the input voltage high via the voltage drop over $R_{(3-4)}$. As a result, the duty cycle will become zero, provided that $R_{(3-4)}$>100k. When the feedback loop is short-circuited, the duty cycle would jump to the adjusted maximum duty cycle. Therefore, an additional comparator is active for feedback voltages at Pin 3 below 0.6V. Now an internal resistor of typically 1k is shunted to the impedance on the δ_{MAX} setting Pin 6. Depending on this impedance, δ will be reduced to a value δ_0. This will be discussed further.



a. Duty Cycle — δ — % Regulation



b. Pulse-Width Modulation

Figure 5.

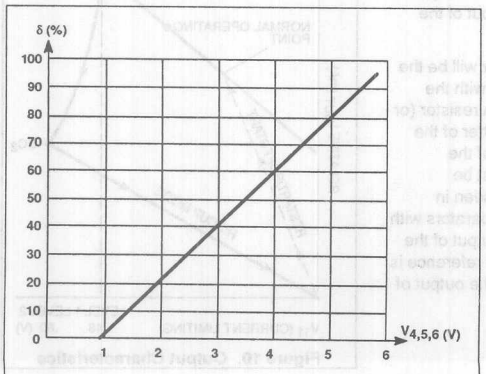


Figure 6. Transfer Curve of Pulse-Width Modulator Duty Cycle vs Input Voltage

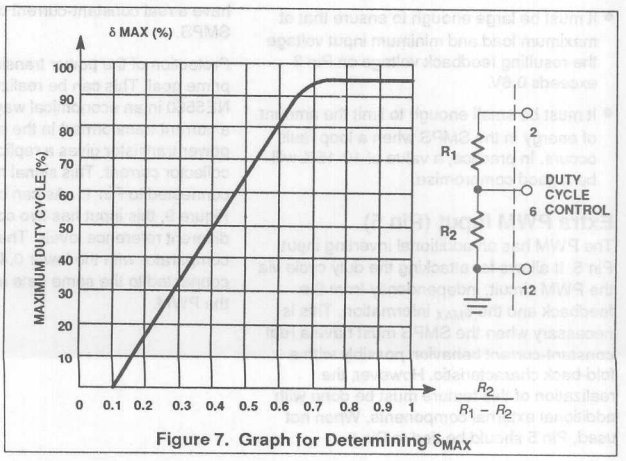


Figure 7. Graph for Determining δ_{MAX}

The Pulse-Width Modulator

The function of the PWM circuit is to translate a feedback voltage into a periodical pulse of which the duty cycle depends on that feedback voltage. As can be seen in Figure 5, the PWM circuit in the NE5560 is a long-tailed pair in which the sawtooth on Pin 8 is compared with the LOWEST voltage on either Pin 4 (error amplifier), Pin 5, or Pin 6 (δ_{MAX} and slow-start). The transfer graph is given in Figure 6. The output of the PWM causes the resetting of the output bistable.

Limitation of the Maximum Duty Cycle

With Pins 5 and 6 not connected and with a rather low feedback voltage on Pin 3, the NE5560 will deliver output pulses with a duty cycle of ≈ 95%. In many SMPS applications, however, this high δ will cause problems. Especially in forward converters, where the transformer will saturate when δ exceeds 50%, a limitation of the maximum duty cycle is a must.

A DC voltage applied to Pin 6 (PWM input) will set δ_{MAX} at a value in accordance with Figure 6. For low tolerances of δ_{MAX}, this voltage on Pin 6 should be set with a resistor divider from V_Z (Pin 2). The upper and lower sawtooth levels are also set by means of an internal resistor divider from V_Z, so forming a bridge configuration with the δ_{MAX} setting is low because tolerances in V_Z are compensated and the sawtooth levels are determined by internal resistor matching rather than by absolute resistor tolerance. Figure 7 can be used for determining the tap on the bleeder for a certain δ_{MAX} setting.

As already mentioned, Figure 8 gives a graphical representation of this. The value δo is limited to the lower and the higher side;

- It must be large enough to ensure that at maximum load and minimum input voltage the resulting feedback voltage on Pin 3 exceeds 0.6V.
- It must be small enough to limit the amount of energy in the SMPS when a loop fault occurs. In practice, a value of 10-15% will be a good compromise.

Extra PWM Input (Pin 5)

The PWM has an additional inverting input: Pin 5. It allows for attacking the duty cycle via the PWM circuit, independently from the feedback and the δ_{MAX} information. This is necessary when the SMPS must have a real constant-current behavior, possibly with a fold-back characteristic. However, the realization of this feature must be done with additional external components. When not used, Pin 5 should be tied to Pin 6.

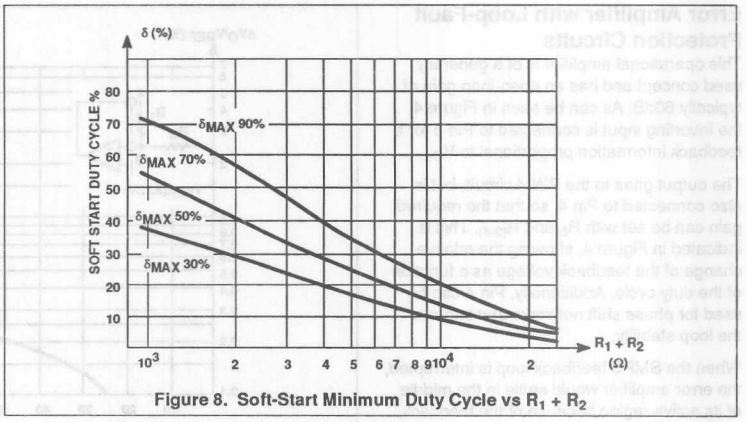


Figure 8. Soft-Start Minimum Duty Cycle vs $R_1 + R_2$

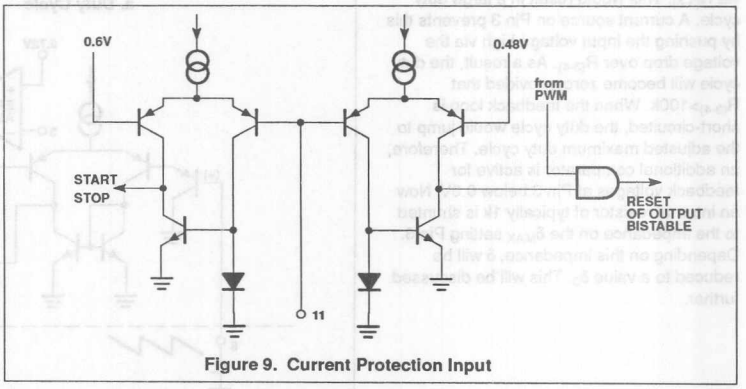


Figure 9. Current Protection Input

Dynamic Current Limit and Current Protection (Pin 11)

In many applications, it is not necessary to have a real constant-current output of the SMPS.

Protection of the power transistor will be the prime goal. This can be realized with the NE5560 in an economical way. A resistor (or a current transformer) in the emitter of the power transistor gives a replica of the collector current. This signal must be connected to Pin 11. As can be seen in Figure 9, this input has two comparators with different reference levels. The output of the comparator with the lower 0.48V reference is connected to the same gate as the output of the PWM.

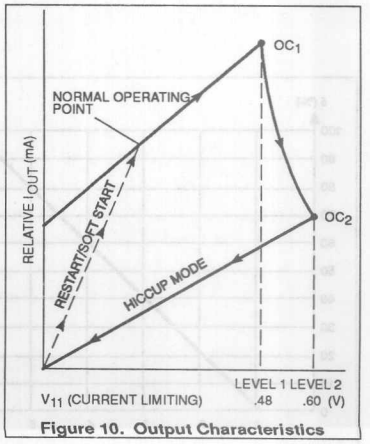


Figure 10. Output Characteristics

When activated, it will immediately reset the output flip-flop, so reducing the duty cycle. The effectiveness of this cycle-by-cycle current limit diminishes at low duty cycle values. When δ becomes very small, the storage time of the power transistor becomes dominant. The current will now increase again, until it surpasses the reference of the second comparator. The output of this comparator activates the start-stop circuit and causes an immediate inhibit of the output pulses. After a certain deadtime, the circuit starts again with very narrow output pulses. The effect of this two-level current protection circuit is visualized in Figure 10.

The Start-Stop Circuit

The function of this protection circuit is to stop the output pulses as soon as a fault occurs and to keep the output stopped for several periods. After this dead-time, the output starts with a very small, gradually increasing duty cycle. When the fault is persistent, this will cause a cyclic switch-off/switch-on condition. This "hiccup" mode effectively limits the energy during fault conditions. The realization and the working of the circuit are indicated in Figures 12 and 13. The dead time and the soft-start are determined by an external capacitor that is connected to Pin 6 (δ_{MAX} setting).

An RS flip-flop can be set by three different functions:
1. Remote on/off on Pin 10.
2. Overcurrent protection on Pin 11.
3. Low supply voltage protection (internal).

As soon as one of these functions cause a setting of the flip-flop, the output pulses are blocked via the output gate. In the same time transistor Q1 is forward-biased, resulting in a discharge of the capacitor on Pin 6.

The discharging current is limited by an internal 150Ω resistor in the emitter of Q1. The voltage at Pin 6 decreases to below the lower level of the sawtooth. When V6 has dropped to 0.6V, this will activate a comparator and the flip-flop is reset. The output stage is no longer blocked and Q1 is cut off. Now V_Z will charge the capacitor via R1 to the normal δ_{MAX} voltage. The output starts delivering very narrow pulses as soon as V6 exceeds the lower sawtooth level. The duty cycle of the output pulse now gradually increases to a value determined by the feedback on Pin 3, or by the static δ_{MAX} setting on Pin 6.

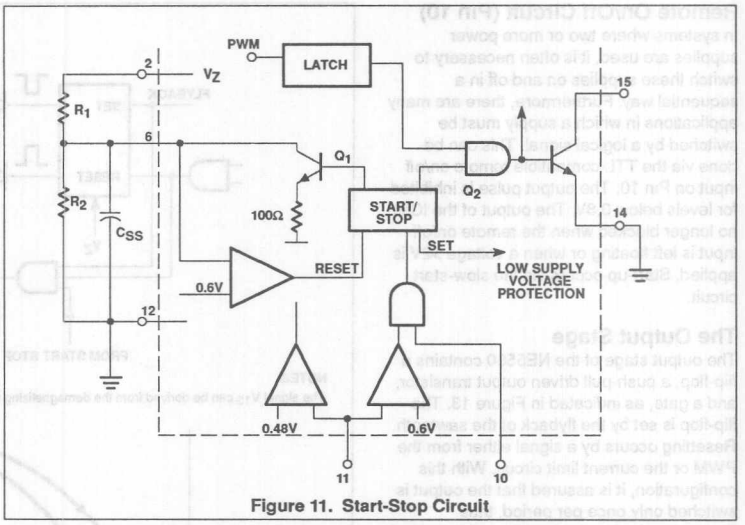


Figure 11. Start-Stop Circuit

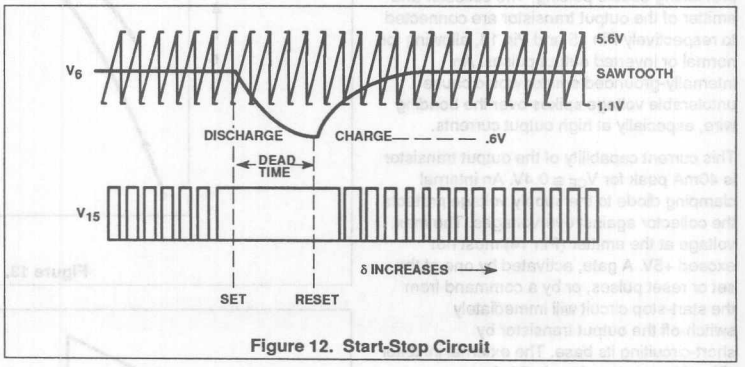


Figure 12. Start-Stop Circuit

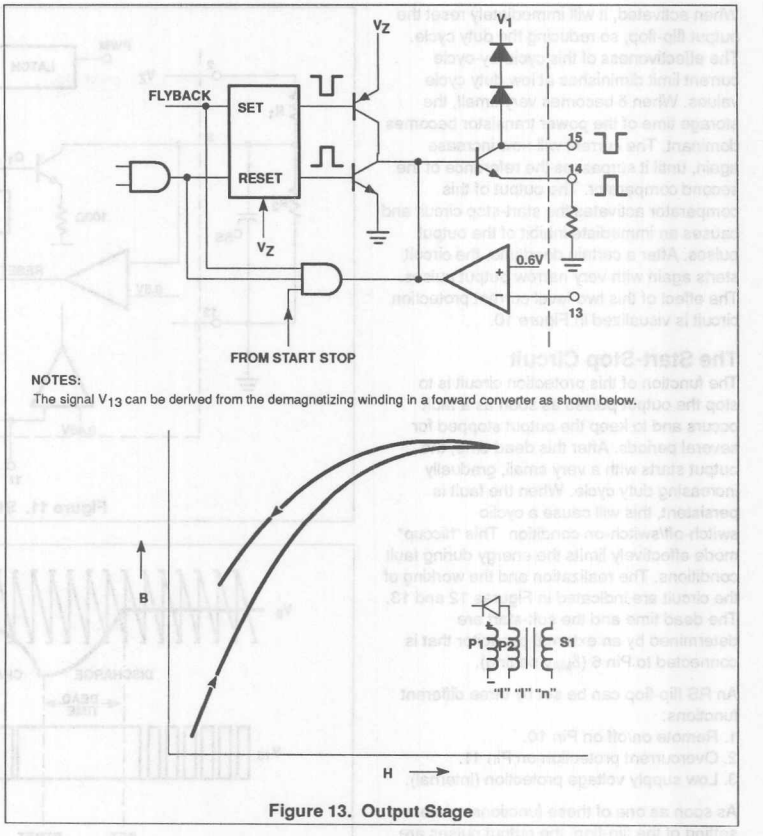
Remote On/Off Circuit (Pin 10)

In systems where two or more power supplies are used, it is often necessary to switch these supplies on and off in a sequential way. Furthermore, there are many applications in which a supply must be switched by a logical signal. This can be done via the TTL-compatible remote on/off input on Pin 10. The output pulse is inhibited for levels below 0.8V. The output of the IC is no longer blocked when the remote on/off input is left floating or when a voltage >2V is applied. Start-up occurs via the slow-start circuit.

The Output Stage

The output stage of the NE5560 contains a flip-flop, a push-pull driven output transistor, and a gate, as indicated in Figure 13. The flip-flop is set by the flyback of the sawtooth. Resetting occurs by a signal either from the PWM or the current limit circuit. With this configuration, it is assured that the output is switched only once per period, thus prohibiting double pulsing. The collector and emitter of the output transistor are connected to respectively Pin 15 and Pin 14, allowing for normal or inverted output pulses. An internally-grounded emitter would cause untolerable voltage spikes over the bonding wire, especially at high output currents.

This current capability of the output transistor is 40mA peak for $V_{CE} \cong 0.4V$. An internal clamping diode to the supply voltage protects the collector against overvoltages. The max. voltage at the emitter (Pin 14) must not exceed +5V. A gate, activated by one of the set or reset pulses, or by a command from the start-stop circuit will immediately switch-off the output transistor by short-circuiting its base. The external inhibitor (Pin 13) operates also via this base.



NOTES:
The signal V_{13} can be derived from the demagnetizing winding in a forward converter as shown below.

Figure 13. Output Stage

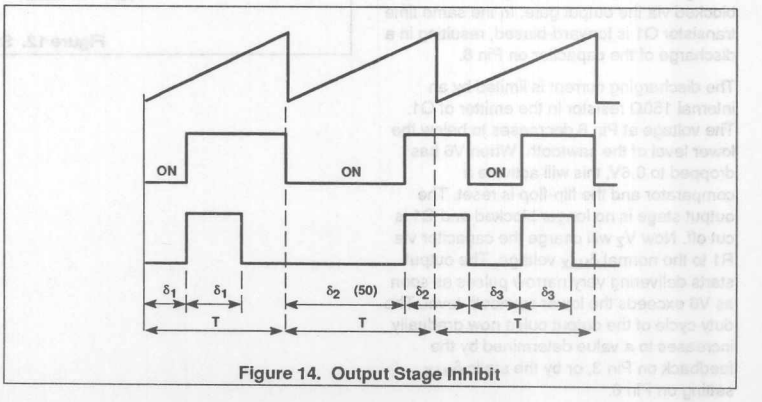


Figure 14. Output Stage Inhibit

Demagnetization Sense

As indicated in Figure 13, the output of this NPN comparator will block the output pulse, when a voltage above 0.6V is applied to Pin 13. A specific application for this function is to prevent saturation of forward-converter transformers. This is indicated in Figure 14.

Feed-Forward (Pin 16)

The basic formula for a forward converter is

$$V_{OUT} = \frac{dV_{IN}}{n} \quad (n = \textit{transformer ratio})$$

This means that in order to keep V_{OUT} at a constant value, the duty cycle δ must be made inversely proportional to the input voltage. A preregulation (feed-forward) with the function $\delta \sim 1/V_{IN}$ can ease the feedback-loop design.

This loop now only has to regulate for laod variations which require only a low feedback gain in the normal operation area. The transformer of a forward converter must be designed in such a way that it does not saturate, even under transient conditions, where the max. inductance is determined by $\delta_{MAX} \times V_{IN}$ max. A regulation of $\delta_{MAX} \sim 1/V_{IN}$ will allow for a considerable reduction or simplification of the transformer. The function of $\delta \sim 1/V_{IN}$ can be realized by using Pin 16 of the NE5560.

Figure 15 shows the electrical realization. When the voltage at Pin 16 exceeds the stabilized voltage V_Z (Pin 2), it will increase the charging current for the timing capacitor on Pin 8.

The operating frequency is not affected, because the upper trip level for sawtooth increases also. Note that the δ_{MAX} voltage on Pin 6 remains constant because it is set via V_Z. Figure 16 visualizes the effect on δ_{MAX} and the normal operating duty cycle δ. For $V_{16}=2 \times V_Z$, these duty cycles have halved. The graph for $\delta=f(V_{16})$ is given in Figure 17.

NOTE:
V_{16} must be less than Pin 1 voltage.

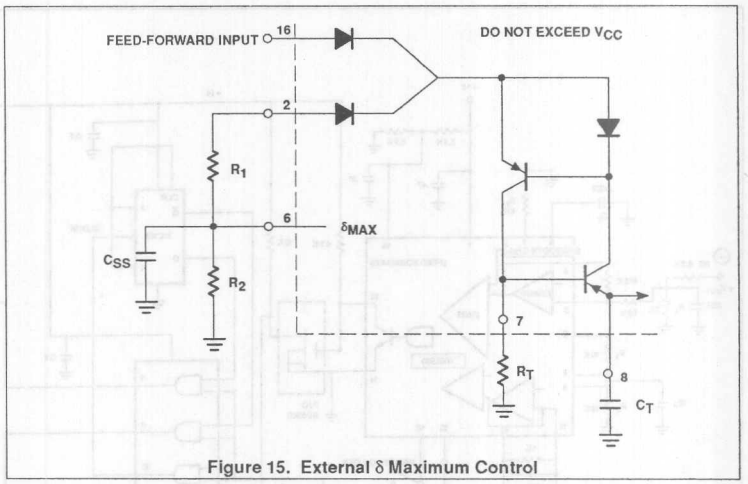


Figure 15. External δ Maximum Control

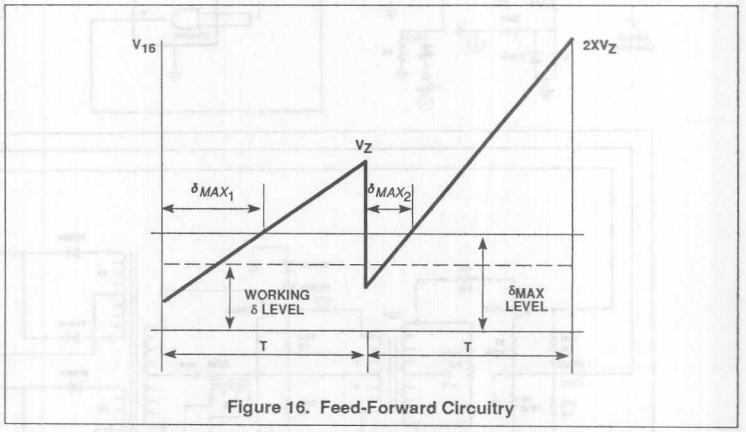


Figure 16. Feed-Forward Circuitry

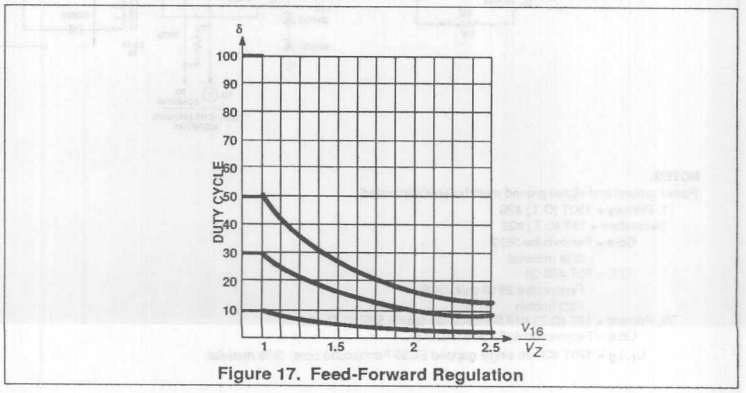


Figure 17. Feed-Forward Regulation

APPLICATIONS

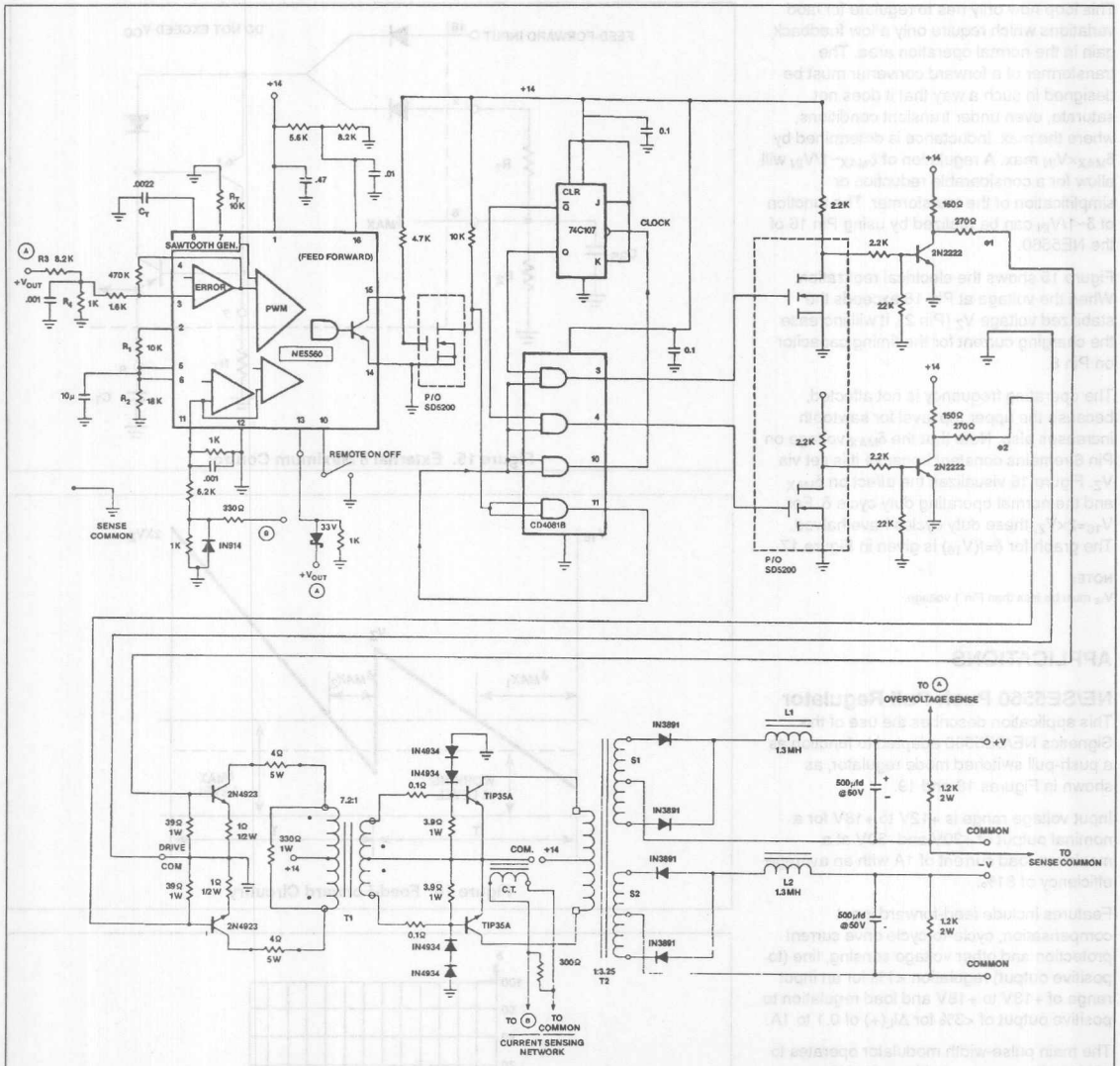
NE/SE5560 Push-Pull Regulator

This application describes the use of the Signetics NE/SE5560 adapted to function as a push-pull switched mode regulator, as shown in Figures 18 and 19.

Input voltage range is +12V to +18V for a nominal output of +30V and -30V at a maximum load current of 1A with an average efficiency of 81%.

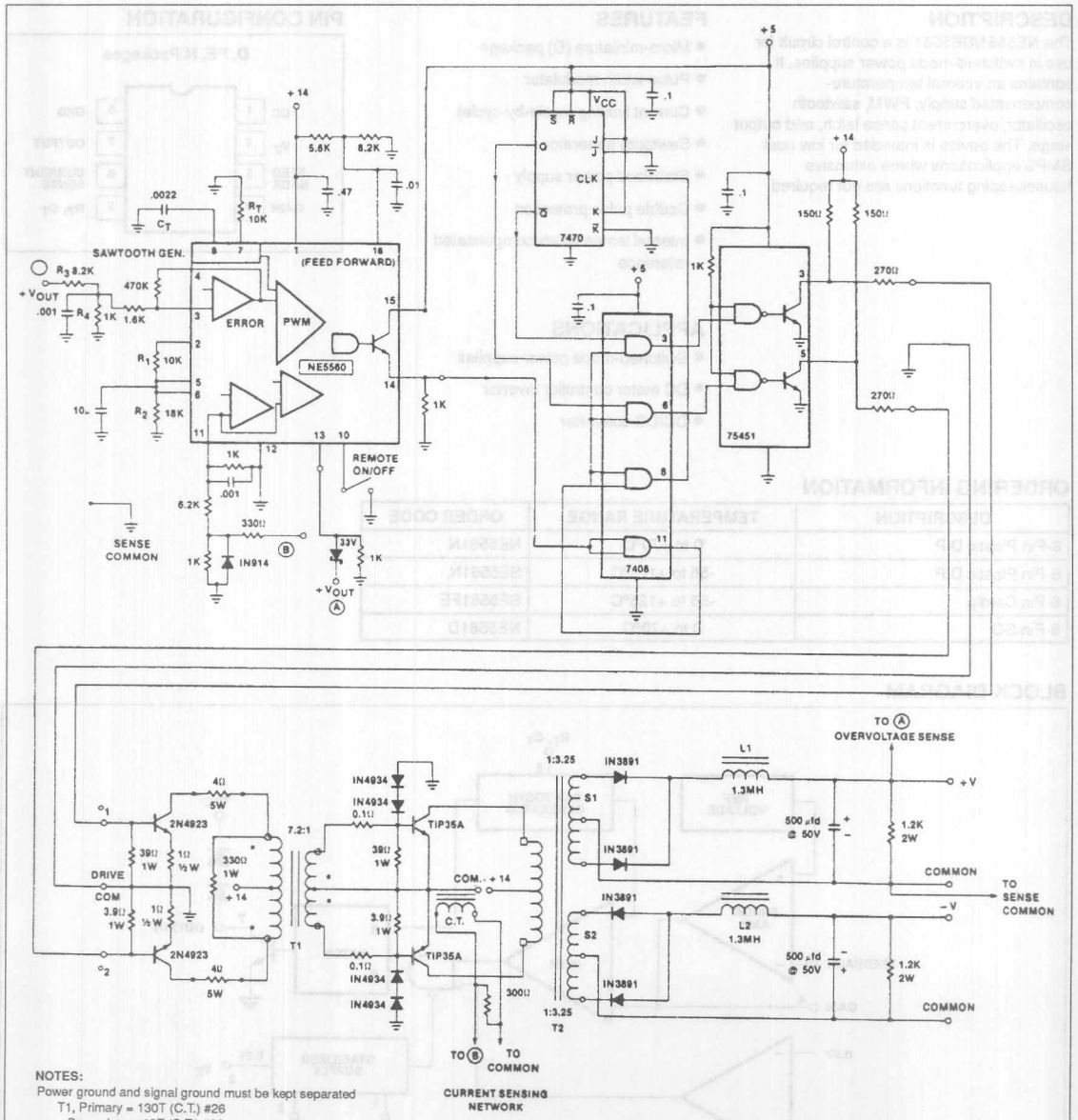
Features include feed-forward input compensation, cycle-to-cycle drive current protection and other voltage sensing, line (to positive output) regulation <1% for an input range of +13V to +18V and load regulation to positive output of <3% for $\Delta I_L(+)$ of 0.1 to 1A.

The main pulse-width modulator operates to 48kHz with power switching at 24kHz.



NOTES:
Power ground and signal ground must be kept separated
T1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622
3C8 material
C.T. = 50T #26 0n
Ferroxcube 2616 core (3C8)
F2D bobbin
T2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22
Core = Ferroxcube 4229 3C8 material
L_1, L_2 = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material.

Figure 18. NE/SE5560 Push-Pull Switched-Mode Regulated Supply with CMOS Drive Conversion Logic



NOTES:
Power ground and signal ground must be kept separated
T1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622
3C8 material
C.T. = 50T #26 0n
Ferroxcube 2616 core (3C8)
F2D bobbin
T2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22
Core = Ferroxcube 4229 3C8 material
L_1, L_2 = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material.

Figure 19. NE/SE5560 Push-Pull Switched-Mode Regulated With TTL Drive Conversion Logic

Switched-mode power supply control circuit NE/SE5561

DESCRIPTION

The NE5561/SE5561 is a control circuit for use in switched-mode power supplies. It contains an internal temperature-compensated supply, PWM, sawtooth oscillator, overcurrent sense latch, and output stage. The device is intended for low cost SMPS applications where extensive housekeeping functions are not required.

FEATURES

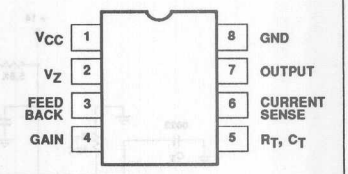
- Micro-miniature (D) package
- Pulse-width modulator
- Current limiting (cycle-by-cycle)
- Sawtooth generator
- Stabilized power supply
- Double pulse protection
- Internal temperature-compensated reference

APPLICATIONS

- Switched-mode power supplies
- DC motor controller inverter
- DC/DC converter

PIN CONFIGURATION

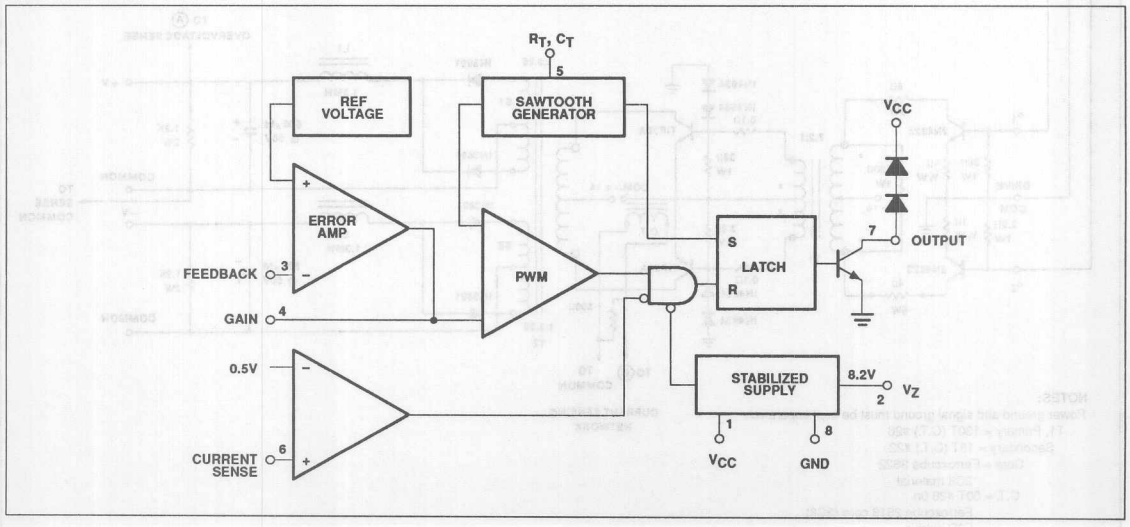
D, FE, N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5561N
8-Pin Plastic DIP	-55 to +125°C	SE5561N
8-Pin Cerdip	-55 to +125°C	SE5561FE
8-Pin SO	0 to +70°C	NE5561D

BLOCK DIAGRAM



Switched-mode power supply control circuit NE/SE5561

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply[1]		
	Voltage-forced mode	+18	V
	Current-fed mode	30	mA
	Output transistor (at 20-30V max)		
I_{OUT}	Output current	40	mA
V_{OUT}	Output voltage	V_{CC}+1.4V	V
	Output duty cycle	98	%
P_D	Maximum total power dissipation	0.75	W
T_A	Operating temperature range		
	SE5561	-55 to +125	°C
	NE5561	0 to 70	°C

NOTES:
1. See Voltage-Current-fed supply characteristic curve.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=12V, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5561			NE5561			UNIT
				Min	Typ	Max	Min	Typ	Max	
Reference section										
V_{REF}	Internal ref voltage	T_A=25°C		3.69	3.75	3.84	3.57	3.75	3.96	V
		Over temperature		3.65		3.88	3.55		3.98	V
V_Z	Internal zener ref	*I_L=7mA		7.8	8.2	8.8	7.8	8.2	8.8	V
	Temp. coefficient of V_{REF}				±100			±100		ppm/°C
	Temp. coefficient of V_Z				±200			±200		ppm/°C
Oscillator section										
	Frequency range	Over temperature		50		100k	50		100k	Hz
	Initial accuracy	R_T and C_T constant			5			5		%
	Duty cycle range	f_O=20kHz		0		98	0		98	%
Current limiting										
I_{IN}	Input current	Pin 6=250mV	T_A=25°C		-2	-10		-2	-10	µA
			Over temp.			-20			-20	µA
	Single pulse inhibit delay	Inhibit delay time for 20% overdrive at	I_{OUT}=20mA		0.88	1.10		0.88	1.10	µs
			I_{OUT}=40mA		0.7	0.8		0.7	0.8	µs
	Current limit trip level			.400	.500	.600	.400	.500	.600	V
Error amplifier										
	Open-loop gain				60			60		dB
	Feedback resistor			10k			10k			Ω
BW	Small-signal bandwidth				3			3		MHz
V_{OH}	Output voltage swing			6.2			6.2			V
V_{OL}	Output voltage swing					0.7			0.7	V
Output stage										
I_{OUT}	Output current	Over temperature		20			20			mA
V_{CE}	Sat	I_C=20mA, Over temp.				0.4			0.4	V

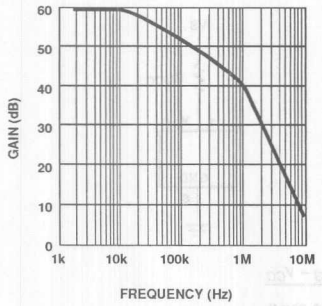
DC ELECTRICAL CHARACTERISTICS

V_{CC}=12V, T_A=25°C, unless otherwise specified.

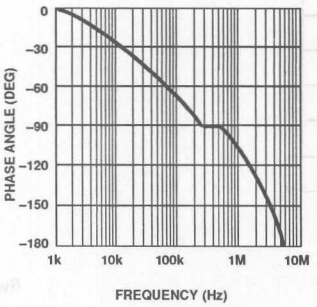
SYMBOL	PARAMETER	TEST CONDITIONS		SE5561			NE5561			UNIT
				Min	Typ	Max	Min	Typ	Max	
Supply voltage/current										
I_{CC}	Supply current	I_Z=0, voltage-forced	T_A=25°C			10.0			10.0	mA
			Over temp.			13.0			13.0	mA
V_{CC}	Supply voltage	I_{CC}=10mA, current-fed		20.0	21.0	22.0	19.0	21.0	24.0	V
		I_{CC}=30mA current		20.0		30.0	20.0		30.0	V
Low supply protection										
	Pin 1 threshold			8	9	10.5	8	9	10.5	V

TYPICAL PERFORMANCE CHARACTERISTICS

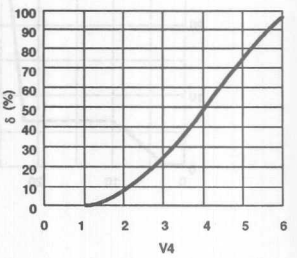
Error Amplifier Open-Loop Gain



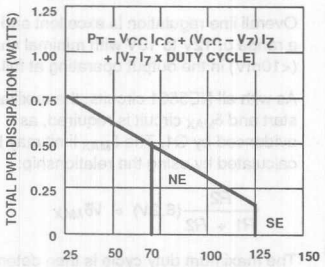
Error Amplifier Open-Loop Phase



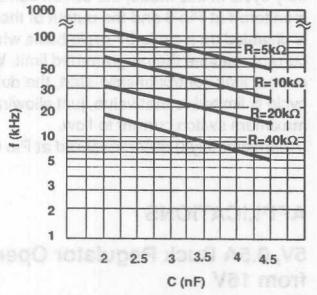
Transfer Curve of Pulse-Width Modulator Duty Cycle vs Input Voltage

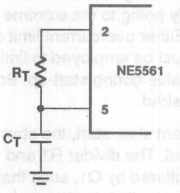


Power Derating Curve

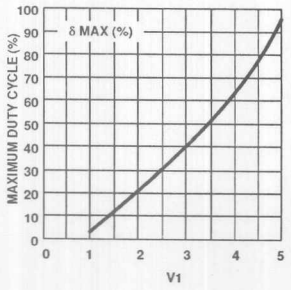


Typical Frequency Plot vs R_T and C_T

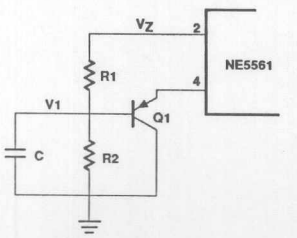




Maximum Duty Cycle vs Base Voltage on Q1

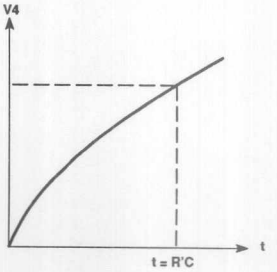


Start-Up Circuit

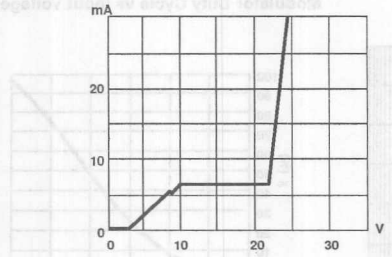


δ max is a function of $f\left[\frac{R2}{R1 + R2} V_Z + V_{BEQ1}\right]$

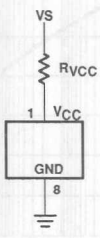
Slow-Start Voltage



NE5561 Voltage-Current-Fed Supply Characteristics



Current-Fed Dropping Resistor



$$R_{VCC} = \frac{V_S - V_{CC}}{(10\ 20mA)}$$

NOTE:
See DC Electrical Characteristics for Current Fed V_{CC} Range.

NE5561 START-UP

The start-up, or initial turn-on, of this device requires some degree of external protective duty cycle limiting to prevent the duty cycle from initially going to the extreme maximum (δ>90%). Either overcurrent limit or slow-start circuitry must be employed to limit duty cycle to a safe value during start-up. Both may be used, if desired.

To implement slow-start, the start-up circuit can be used. The divider R1 and R2 sets a voltage, buffered by Q1, such that the output of the error amplifier is clamped to a maximum output voltage, thereby limiting the maximum duty cycle. The addition of capacitor C will cause this voltage to ramp-up slowly when power is applied, causing the duty cycle to ramp-up simultaneously.

Overcurrent limit may be used also. To limit duty cycle in this mode, the switch current is monitored at Pin 6 and the output of the 5561 is disabled on a cycle-by-cycle basis when current reaches the programmed limit. With current limit control of slow-start, the duty cycle is limited to that value, just allowing maximum switch current to flow. (Approximately 0.50V measured at Pin 6.)

APPLICATIONS

5V, 0.5A Buck Regulator Operates from 15V

The converter design shows how simple it is to derive a TTL supply from a system supply of 15V (see Figure 1). The NE5561 drives a 2N4920 PNP transistor directly to provide switching current to the inductor.

Overall line regulation is excellent and covers a range of 12V to 18V with minimal change (<10mV) in the output operating at full load.

As with all NE5561 circuits, the auxiliary slow start and δ_{MAX} circuit is required, as evidenced by Q1. The δ_{MAX} limit may be calculated by using the relationship:

$$\frac{R2}{R1 + R2}(8.2V) = V\delta_{MAX}$$

The maximum duty cycle is then determined from the pulse-width modulator transfer graph, with R1 and R2 being defined from the desired conditions.

Switched-mode power supply control circuit NE/SE5562

DESCRIPTION

The NE/SE5562 is a single-output control circuit for switched-mode power supplies. This single monolithic IC contains all control and protection features needed for full-featured switched-mode power supplies.

The 100mA source/sink output is designed to drive power FETs directly. The associated output logic is designed to prevent double pulsing or cross-conduction current spiking on the output.

All of the control and protect features work cycle-by-cycle up to the maximum operating frequency of 600kHz.

For ease of interface, all digital inputs are TTL or CMOS compatible.

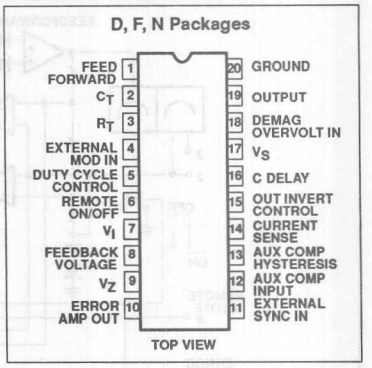
The NE5562 is supplied in 20-pin glass/ceramic (Cerdip), plastic DIP, and plastic SO packages. The NE grade part is characterized and guaranteed over the commercial ambient temperature range of 0°C to +70°C and junction temperature range of 0°C to +85°C. The SE5562 is supplied in the glass/ceramic (Cerdip) package. The SE grade part is characterized and guaranteed over the ambient temperature range of -55 to +125°C and junction temperature range of -55 to +135°C.

FEATURES

- Stabilized power supply
- Temperature-compensated reference source
- Sawtooth generator
- Pulse width modulator
- Remote on/off switching
- Current limiting (2 levels)
- Auxiliary comparator, with adjustable hysteresis
- Loop fault protection
- Demagnetization/overvoltage protection
- Duty cycle adjust and clamp
- Feed-forward control
- External synchronization
- Total shutdown after adjustable number of overcurrent faults
- Soft-start

PIN CONFIGURATION

D, F, N Packages

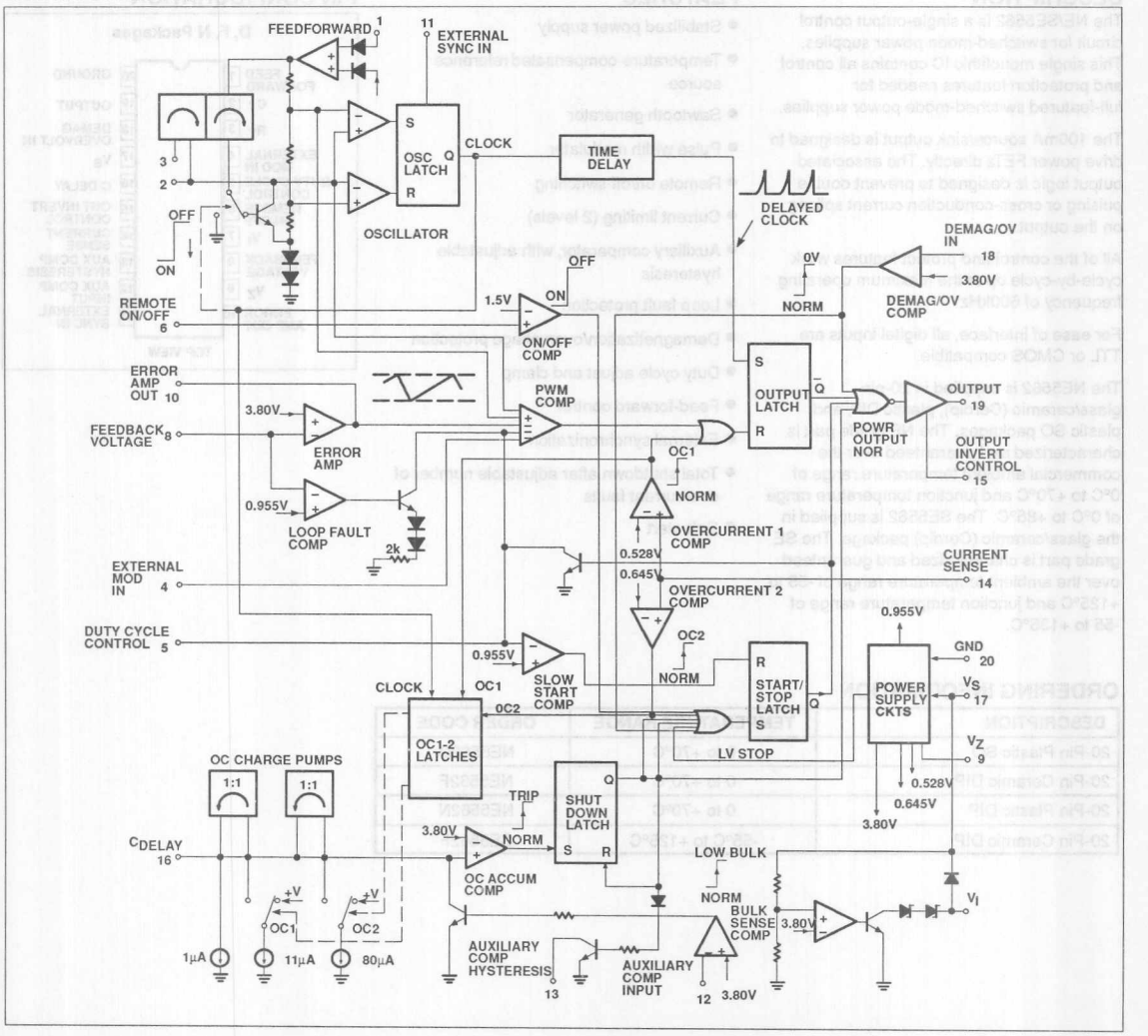


TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SO	0 to +70°C	NE5562D
20-Pin Ceramic DIP	0 to +70°C	NE5562F
20-Pin Plastic DIP	0 to +70°C	NE5562N
20-Pin Ceramic DIP	-55°C to +125°C	SE5562F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply		
V_S	voltage-fed mode (Pin 17)	16	V
I_{CC}	current-fed mode (Pin 7)	30	mA
	Output transistor output current	100	mA
	Sync (Pin 11)	V_S	V
	Duty cycle control (Pin 5)	V_Z	V
	Remote on/off (Pin 6)	V_S	V
	Output invert control (Pin 15)	V_S	V
	Feedback pin (Pin 8)	V_Z	V
	C_{DELAY} (Pin 16)	V_Z	V
	External mod in (Pin 4)	V_S	V
FF	Feed-forward (Pin 1)	V_S	V
	Demag/overvoltage in (Pin 18)	V_Z	V
	Current sense (Pin 14)	V_S	V
	80Low supply sense and hysteresis (Pins 12, 13)	V_S	V
T_J	Operating junction temperature	135	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec)	300	°C

NOTES:
1. Ground Pin 20 must always be the most negative pin.
2. For power dissipation, see the application section which follows.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
	Supply		
	voltage-fed	10 to 16	V
	current-fed	15	mA
T_A	Ambient temperature range		
	NE grade	0 to +70	°C
	SE grade	-55 to +125	°C
T_J	Junction temperature range		
	NE grade	0 to +85	°C
	SE grade	-55 to +135	°C

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Internal reference										
V_{REF}	Reference voltage	Internal	T_A=25°C	3.76	3.80	3.84	3.76	3.80	3.84	V
V_{REF}	Reference voltage	Internal	Over temp.	3.72	3.8	3.90	3.725	3.8	3.870	V
	Temperature stability	Internal			30			30		ppm/°C
	Long-term stability	Internal			0.5			0.5		µV/1000 hrs

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 12V, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Reference										
V_Z	Zener voltage	9	I_L=7mA, T_A=25°C	7.35	7.60	7.75	7.35	7.6	7.75	V
V_Z	Zener voltage	9	I_L=7mA, Over temp.	7.25		7.80	7.20		7.78	V
$\Delta V_Z / \Delta T$	Temperature stability	9	I_L<1mA		50			50		ppm/°C
Low supply shutdown										
	80Comparator threshold voltage	Internal	T_A=25°C	8.30	8.45	8.75	8.30	8.45	8.75	V
	80Comparator threshold voltage	Internal	Over temp.	8.00	8.45	8.90	8.00	8.45	8.90	V
	Hysteresis	Internal		25	50	8.00	25	50	800	mV
Oscillator										
f_{MIN}	Frequency range, minimum	1, 2, 3, 11	R_T=42.7kΩ, C_T=0.47µF		60	80		60	80	Hz
f_{MAX}	Frequency range, maximum	1, 2, 3, 11	R_T=2.87kΩ, C_T=380pF	600			600			kHz
	Initial accuracy	1, 2, 3, 11	f_O=52kHz, R_T=16kΩ and C_T=0.0015µF, T_A=25°C	48.6	54	59.4	48.6	54	59.4	kHz
	Voltage stability	1, 2, 3, 11, 17	10V<V_S<18V		-215			-215		ppm/V
	Temperature stability	1, 2, 3, 11			300	500		300	500	ppm/°C
	Sawtooth peak voltage	2, 3	T_A=25°C[1]	5.00	5.25	5.40	5.00	5.25	5.40	V
		2, 3	Over temp.	4.80	5.25	5.60	4.80	5.25	5.60	V
	Sawtooth valley voltage	2, 3	T_A=25°C	1.25	1.70	2.00	1.25	1.70	2.00	V
		2, 3	Over temp.	1.0	1.7	2.1	1.25	1.7	2.0	V
	Sync. in high level	11		2.0		V_Z	2.0		V_Z	V
	Sync. in low level	11		0.0		0.8	0.0		0.8	V
	Sync. in bias current	11	(Sourced), V_{11}<0.8V		0.50	10.0		0.50	10.0	µA
	Feed-forward ratio, maximum	1			2			2		
	Feed-forward duty cycle reduction	1	V_{FF}=2V_Z, T_A=25°C	11	13.5	19	11	13.5	19	%
		1	Over temp.	6	13.5	22	8		22	%
	Feed-forward reference voltage	9			V_Z	V_S		V_Z	V_S	V
	Feed-forward bias current	1			2.5	50.0		2.5	50.0	µA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 12V, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Error amp										
I_{BIAS}	Input bias current	8			1.0	5.0		1.0	5.0	µA
A_{VOL}	DC open-loop gain	8, 10	R_L>100kΩ	60	86		60	86		dB
V_{OH}	High output voltage	10	I_{SOURCE}=1mA	5			5			V
V_{OL}	Low output voltage	10	I_{SINK}=1mA			2.0			2.0	V
	PSRR from V_Z and V_S	Internal	f_O<300kHz		-40			-40		dB
BW	Small-signal gain bandwidth product				8			8		MHz
	Feedback resistor range			1		240	1		240	kΩ
I_{SINK}	Output sink current		V8=V10=5V			10			10	mA
I_{SOURCE}	Output source current		V8=3V, V10=1V			5			5	mA
	Sawtooth feedthrough		A_V=100, 0% duty cycle		200			200		mV
PWM comparator and modulator										
	Minimum duty cycle	19	@V_{COMP}<, f=300kHz	0			0			%
	Maximum duty cycle	19	@V_{COMP}>, f=300kHz, V15=0V	95		98	95		98	%
A_{CC}	Duty cycle	10, 19	f=15kHz to 200kHz, V_{IN}=0.472 V_Z	41	49	55	41	49	55	%
t_{PD}	Propagation delay to output	2, 19	V_{15}=0		400			400		ns
I_{BIAS}	Bias current, external modulator input	4	(Sourced)		0.20	20		0.20	20	µA
I_{BIAS}	Bias current, duty cycle control	5	(Sourced)		0.20	20		0.20	20	µA
	Soft-start trip voltage	5		.910	0.955	0.990	0.922	0.955	0.988	V
Remote on/off (shutdown)										
	Output enabled	6		0		0.80	0		0.80	V
	Output disabled	6		2		V_Z	2		V_Z	V
I_{BIAS}	Bias current	6			1	10		1	10	µA
V_{IN}	Maximum input voltage	6		V_Z			V_Z			V
	Delay to output(s)	6, 19			400			400		ns
Current limit comparator(s)										
	Shutdown, OC2	14		.593	0.645	.697	0.593	0.645	0.697	V
	Minimum duty cycle, OC1	14		.486	0.528	.570	0.486	0.528	0.570	V
I_{BIAS}	Bias current	14	(Sourced)		0.5	50		0.5	50	µA
OC_1	C_{DELAY} charge current	16		-18.2	-13	-6.5	-18.2	-13	-7.8	µA
OC2	C_{DELAY} charge current	16		-770	-550	-250	-770	-550	-330	µA
C_{DELAY}	Discharge current	16	V12=V_Z	0.4	1.4	4.0	0.8	1.4	2.0	µA
C_{DELAY}	Shut off trip level	16	T_A=25°C	3.75	3.86	3.97	3.75	3.86	3.97	V

DC AND AC ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 12V, specifications apply over temperature, unless otherwise specified.

SYMBOL	PARAMETER	TEST PINS	TEST CONDITIONS	SE5562			NE5562			UNIT
				Min	Typ	Max	Min	Typ	Max	
Auxiliary comparator with shutdown										
I_{BIAS}	Bias current	12	(Sourced)		1	10		1	10	µA
	Threshold voltage	12		3.69	3.80	3.91	3.69	3.80	3.91	V
C_{DELAY}	Discharge current	12	V_{IN}=3V	5	10		5	10		mA
	Hysteresis	12, 13			10			10		mV
Demagnetization overvoltage comparator										
I_{BIAS}	Bias current	18			2	10		2	10	µA
	Threshold voltage	18		3.62	3.80	3.91	3.69	3.80	3.91	V
	Hysteresis	18			10			10		mV
Output stage										
V_{OH}	High output voltage	19	I_{SOURCE}=100mA	V_S-2.5	V_S-1.9		V_S-2.5	V_S-1.9		V
V_{OL}	Low output voltage	19	I_{SINK}=2mA		0.16	0.4		0.16	0.4	V
V_{OL}		19	I_{SINK}=100mA, T_A=25°C		1.4	2.0		1.4	2.0	V
		19	I_{SINK}=100mA, over temp.			2.25			2.25	V
	I_{SINK} max	19		100			100			mA
	I_{SOURCE} max	19		100			100			mA
t_R	Rise time	19	C_L=2000pF		160			160		ns
t_F	Fall time	19	C_L=2000pF		80			80		ns
Supply current/voltage										
I_{CC}	Supply current	17	10V<V_S<16V (Voltage-fed mode), V_I<V_S		9	15		9	15	mA
V_S	Input voltage	7, 17	I_I=15mA, (Current-fed mode) V_S=meter	14.2	15.3	16.7	14.2	15.3	16.7	V
Operating frequency range for all functions but feed-forward working cycle-by-cycle										
f_{MIN}	Minimum frequency	All	R_T=42.7kΩ, C_T=0.47µF		60	80		60	80	Hz
f_{MAX}	Maximum frequency	All	R_T=2.87kΩ, C_T=380pF	600	1000		600	1000		kHz

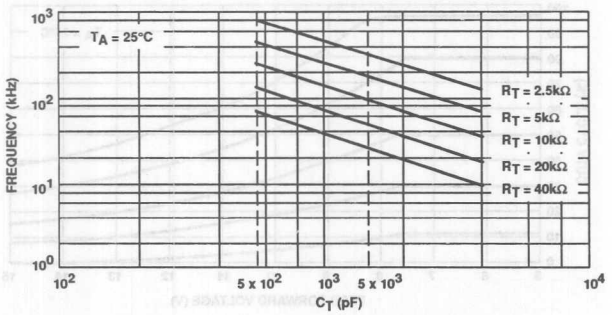


Figure 1. Frequency vs R_T, C_T NE/SE5562

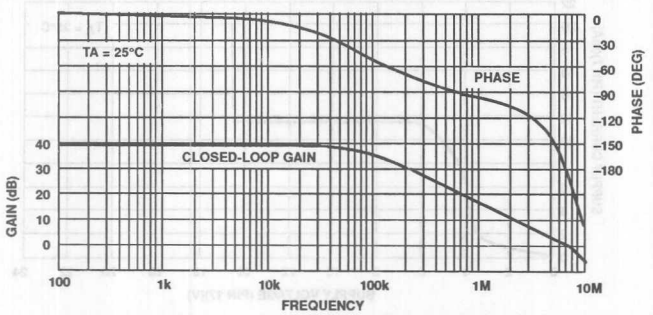


Figure 2. Error Amplifier Closed-Loop Response

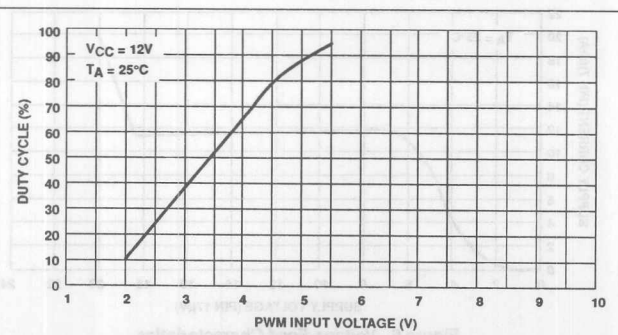


Figure 3. Duty Cycle vs PWM Input Voltage

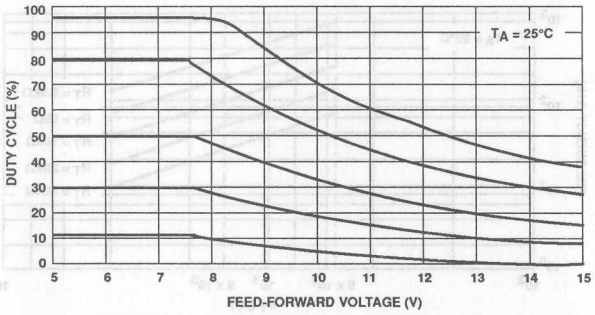


Figure 4. Duty Cycle vs Feed-forward Voltage

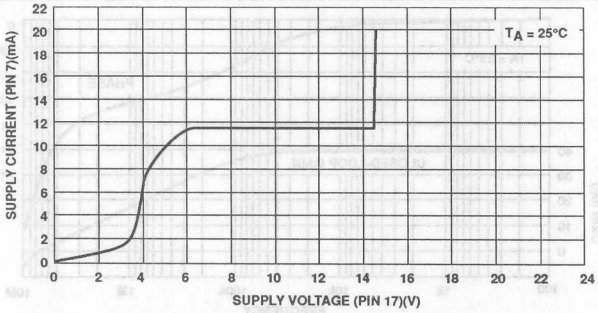


Figure 5. Current-Feed Characteristics

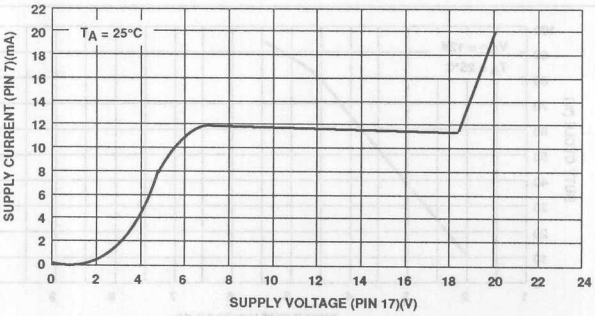


Figure 6. Voltage-Feed Characteristics

THE NE/SE5562 THEORY OF OPERATION

INTRODUCTION

Switched-mode power conversion relies on the principle of pulsed energy storage in an inductive or capacitive element. Capacitive switched converters are typically used with low power systems for which only tens of milliamperes are required. Medium and high power converters tend to use inductive storage elements as shown in Figures 7-9 with which a single switch may be moved around to create step-up (flyback) positive or negative polarity and step-down (forward or buck) conversion from a fixed-voltage source. The relationship between input and output voltage in each case is controlled by the switching on-to-off ratios, which is termed duty cycle. Duty cycle modulation is the common factor in this basic type of power control mechanism. By adding a high-gain operational amplifier, having one input tied to a stable DC reference voltage, configured in a negative feedback loop to maintain a constant output voltage as shown in Figure 10, the switched-mode controller becomes a dynamic voltage regulator. It is this single-switch topology that is most readily adapted to the NE/SE5562 SMPS Control IC.

The ability to switch inductor currents at rates up to 600kHz with state-of-the-art power FETs makes the design of small, efficient switching power converters an attainable reality. Protective features such as programmable slow-start and cycle-by-cycle current limiting allow safe, maintenance-free power supplies to be mass-produced at reduced cost to the manufacturer. Integrated technology makes long-term reliability a predictably achievable goal.

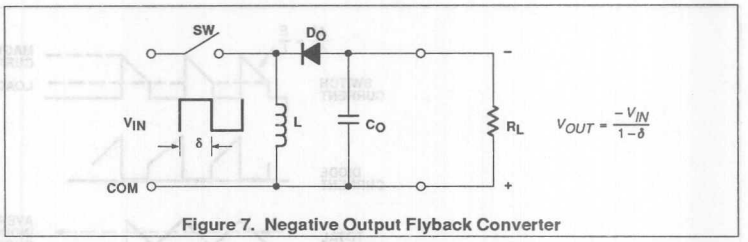


Figure 7. Negative Output Flyback Converter

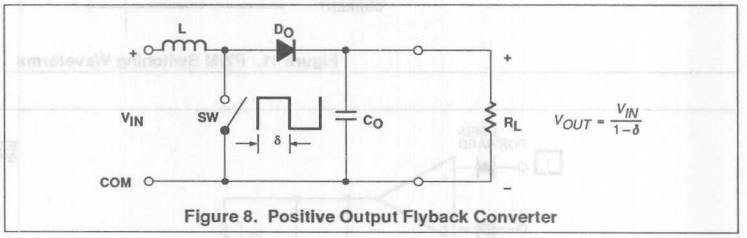


Figure 8. Positive Output Flyback Converter

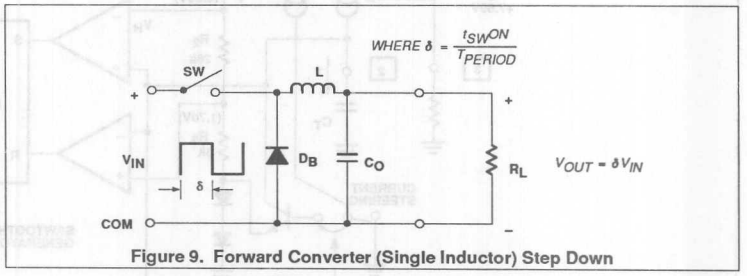


Figure 9. Forward Converter (Single Inductor) Step Down

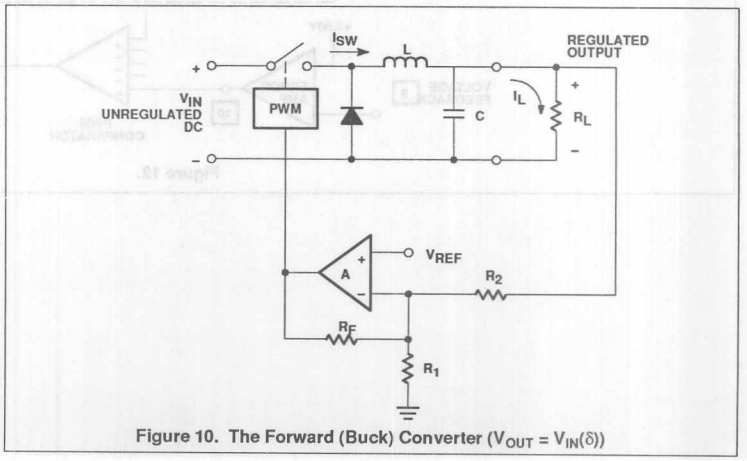


Figure 10. The Forward (Buck) Converter ($V_{OUT} = V_{IN}(\delta)$)

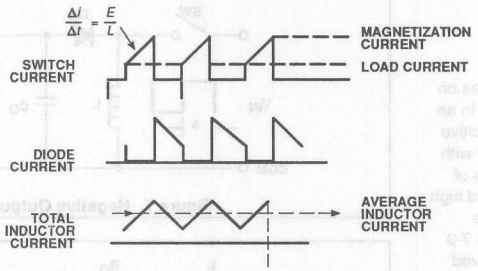


Figure 11. PWM Switching Waveforms

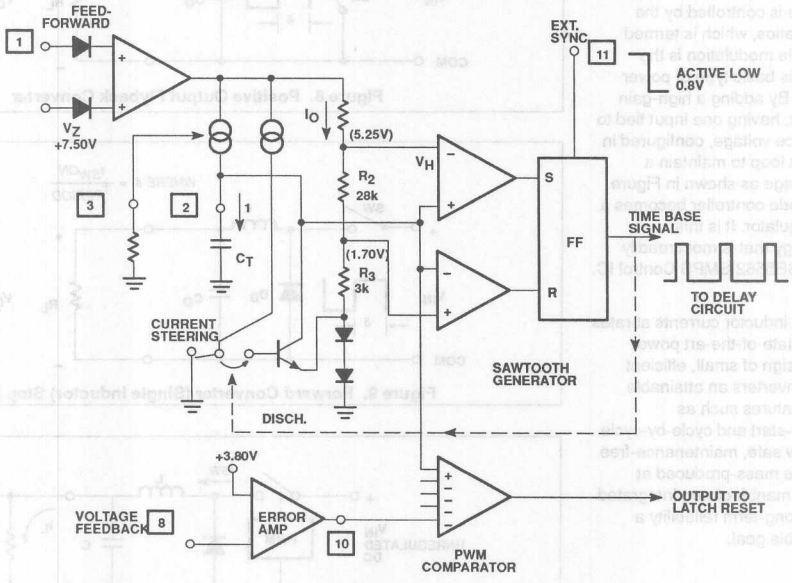


Figure 12.

THE NE/SE5562 THEORY OPERATION

The Sawtooth Oscillator

The sawtooth oscillator consists of a gated charge-discharge capacitor circuit with threshold comparators setting the peak and valley voltages of the ramp. The resistor divider R1-3 is supplied with a source voltage derived from either V_Z (7.50V) minus two diode drops, or, when feed-forward is in control, a voltage greater than V_Z and proportional to the main supply voltage. The nominal upper threshold voltage is 5.25V and the lower threshold 1.70V. These then determine the sawtooth peak and valley voltages, respectively.

Operation

Beginning with the charge cycle, ramp voltage builds up on the timing capacitor due to a constant current supplied to the node at Pin 2. When capacitor voltage reaches the upper threshold, comparator A switches, setting the latching flip-flop. The output of the latch goes high, generating a clock pulse. The discharge transistor is simultaneously turned on, reducing charge on the timing capacitor to the point at which the lower threshold voltage, 1.70V, is reached. The lower comparator is then activated, resetting the latch and terminating the clock pulse. Note that the discharge transistor is referenced to the same return diodes as the threshold resistor divider and the discharge current is made to track with the charge current. This charge and discharge tracking results in a true sawtooth waveform even at extended frequencies. Figure 15 shows a family of curves which explains the relationship between R_T, C_T, and the frequency of the sawtooth generator. The data sheet shows the initial accuracy of the oscillator at 60Hz and 600kHz.

THE PULSE WIDTH MODULATOR AND ERROR AMPLIFIER

The PWM consists of a multi-input voltage comparator (Figure 13) having its positive input tied to the sawtooth ramp voltage and the various negative inputs referenced to ORed control signal nodes. The primary control signal is the error amplifier output voltage node which sets the active duty cycle termination point of the PWM output waveform. As the error amplifier input signal derived from the power supply load voltage varies, for instance in a negative direction, the amplifier output moves upward, raising the PWM comparator toward longer duty cycles at the output on Pin 19. The start-up sequence begins with zero voltage at the input to the error amplifier. Since this could signal an open feedback loop, the loop fault comparator on Pin 8 clamps the PWM duty cycle until the feedback voltage exceeds 0.955V. A second comparator monitors the duty cycle control, Pin 5, with the same threshold level, inhibiting the output via the start-stop latch (Figure 14).

The charging of the slow-start capacitor provides a controlled ramp-up of the output duty cycle and a resultant gradual increase in energy fed to the output magnetics.

The dynamic response of the PWM comparator is shown in the simulated waveform drawing of Figure 15. The error amplifier output voltage is depicted as sloping positive (increasing) with time as referenced to the sawtooth waveform. This causes the duty cycle to increase with time. This is an indication of an increasing load on the power supply as output voltage is decreasing. The Pin 5 (δ_{MAX}) control voltage is also superimposed midway on the sawtooth, indicating the limits of duty cycle increase as the output waveform no longer increases in duty cycle after the δ_{MAX} threshold is crossed. A hypothetical overcurrent pulse (Pin 14) is shown to illustrate cycle termination immediately at the output (Pin 19).

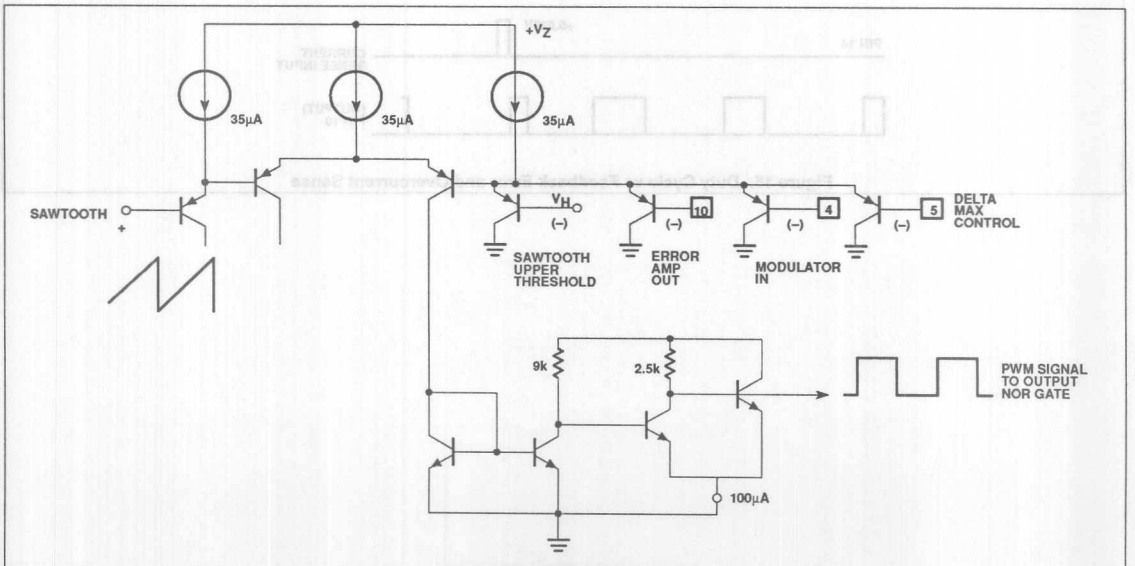


Figure 13. PWM Comparator

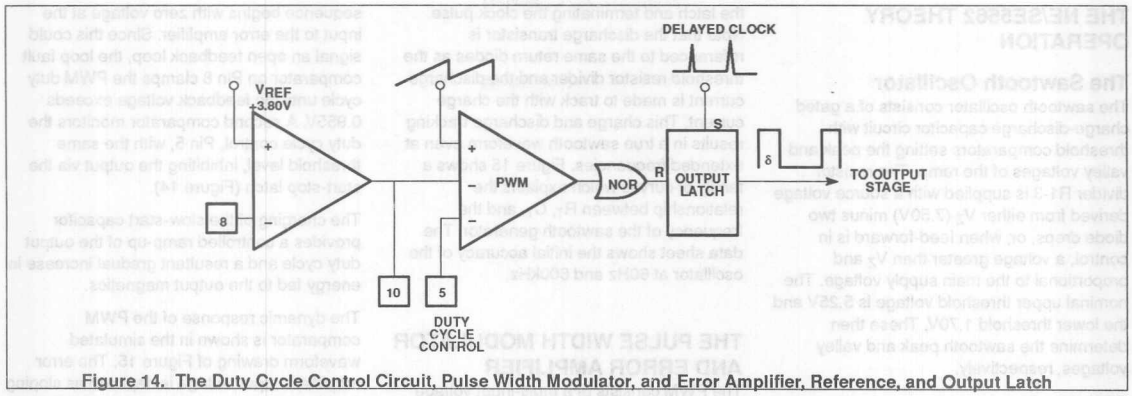


Figure 14. The Duty Cycle Control Circuit, Pulse Width Modulator, and Error Amplifier, Reference, and Output Latch

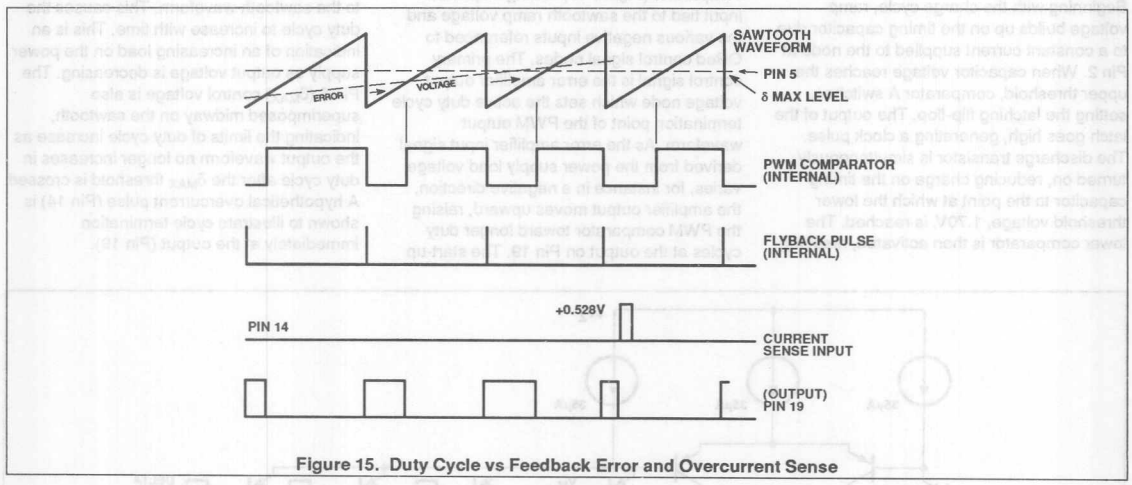


Figure 15. Duty Cycle vs Feedback Error and Overcurrent Sense

The error amplifier's non-inverting input is tied to a bandgap reference of 3.80V, accurate to ±2% at 25°C. The temperature stability of the voltage reference is 30ppm/°C.

The error amplifier is designed for an open-loop gain of 86dB having a small-signal unity gain bandwidth of 3MHz. Closed-loop gain is stable to 10dB, as shown in Figure 17. The DC output excursion of the amplifier is capable of controlling the full PWM range of 0 to 95%. The amplifier can sink 10mA and source 5mA. The nominal DC output for 50% duty cycle is 3.55V. Feedback control resistor value may range from 1kΩ to 240kΩ without overload or instability. However, low closed-loop gains must be compensated by lag lead network techniques for optimum stability. Loop compensation networks may intersect the open-loop gain curve with a slope 2 closure and must then be compensated to maintain overall phase and gain margin (Figure 16).

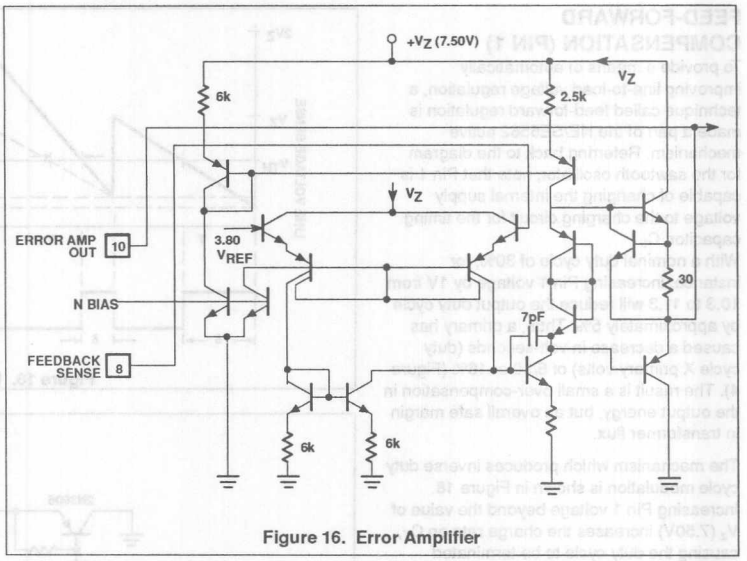


Figure 16. Error Amplifier

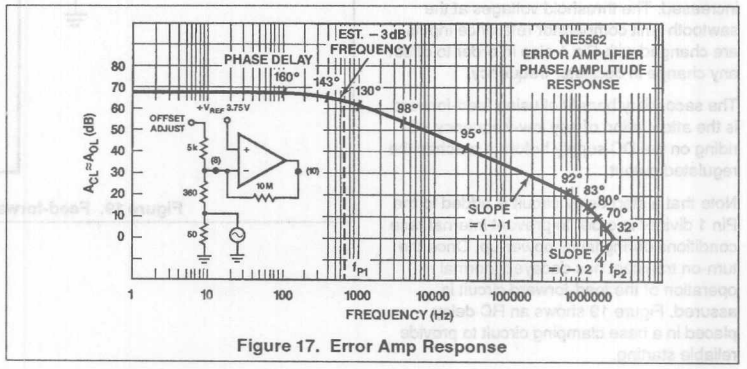


Figure 17. Error Amp Response

FEED-FORWARD COMPENSATION (PIN 1)

To provide a means of automatically improving line-to-load voltage regulation, a technique called feed-forward regulation is made a part of the NE/SE5562 active mechanism. Referring back to the diagram for the sawtooth oscillator, note that Pin 1 is capable of changing the internal supply voltage to the charging circuit for the timing capacitor, C_t.

With a nominal duty cycle of 30%, for instance, increasing Pin 1 voltage by 1V from 10.3 to 11.3 will reduce the output duty cycle by approximately 5%. Thus, a primary has caused a decrease in volt-seconds (duty cycle X primary volts) of 5/30 or 16% (Figure 4). The result is a small over-compensation in the output energy, but an overall safe margin in transformer flux.

The mechanism which produces inverse duty cycle modulation is shown in Figure 18. Increasing Pin 1 voltage beyond the value of V_Z (7.50V) increases the charge rate on C_T, causing the duty cycle to be terminated earlier for each cycle that input voltage is increased. The threshold voltages at the sawtooth limit comparator reference inputs are changed with Pin 1 also in order to offset any change in oscillator frequency.

The secondary benefit of using feed-forward is the attenuation of any low-frequency AC riding on the DC supply before it reaches the regulated output.

Note that a start delay circuit is added to the Pin 1 divider in order to prevent internal race conditions during initial power-up. Once the turn-on transient has decayed, normal operation of the feed-forward circuit is assured. Figure 19 shows an RC delay placed in a base clamping circuit to provide reliable starting.

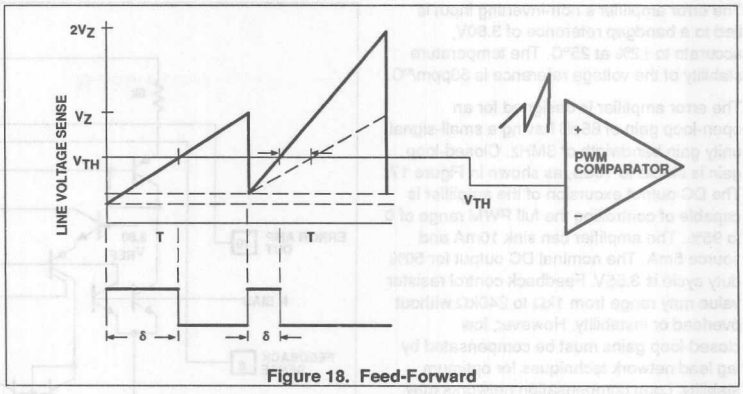


Figure 18. Feed-Forward

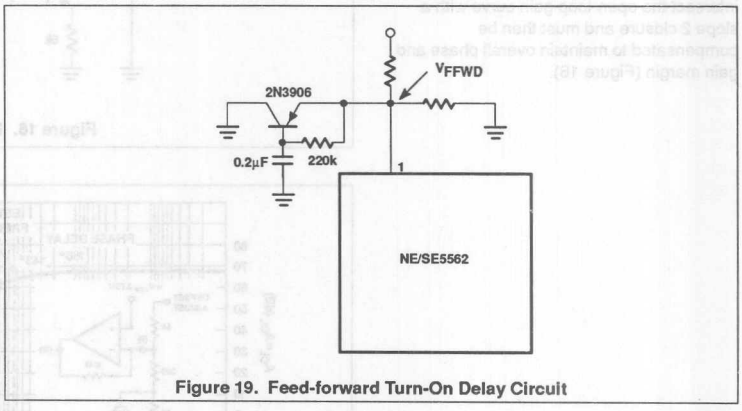


Figure 19. Feed-forward Turn-On Delay Circuit

SYNCHRONIZATION

The synchronization of the sawtooth oscillator to an external pulse of negative-going polarity is shown in Figure 20. When the sync input pulse crosses the 1.5V threshold, negative, the sawtooth oscillator is prevented from discharging the timing capacitor, causing the charge voltage on the capacitor to remain high (5.25V) until the sync pulse again goes above 1.5V, allowing reset. This action stretches the period of the oscillator and results in a lower frequency undersynchronization control than the free-running frequency.

The following relationship holds—

$$f_{free\text{-}run} > f_{sync}$$

$$f_{sync} = \frac{1}{t_0 + \tau}$$

A typical recommended starting point in calculating frequency for synchronous operation is to set the free-run frequency approximately 10% higher than the sync frequency. Then set the pulse width, τ, to 10% of t_0, the free-run period, with the desired new frequency determined by the sum as above.

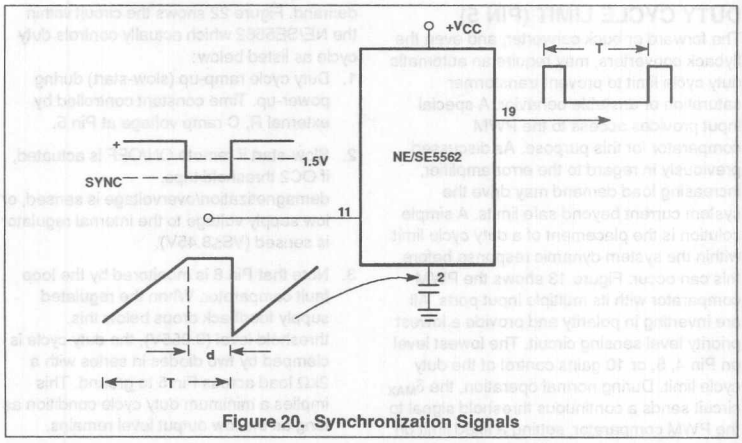


Figure 20. Synchronization Signals

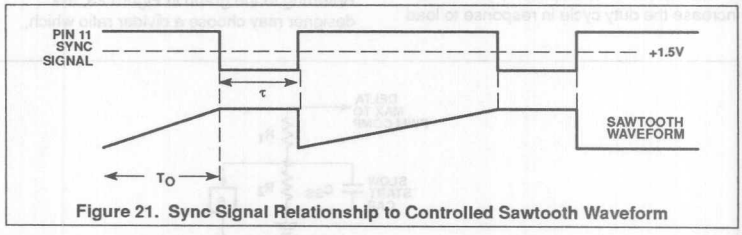


Figure 21. Sync Signal Relationship to Controlled Sawtooth Waveform

DUTY CYCLE LIMIT (PIN 5)

The forward or buck converter, and even the flyback converters, may require an automatic duty cycle limit to prevent transformer saturation or unstable behavior. A special input provides access to the PWM comparator for this purpose. As discussed previously in regard to the error amplifier, increasing load demand may drive the system current beyond safe limits. A simple solution is the placement of a duty cycle limit within the system dynamic response before this can occur. Figure 13 shows the PWM comparator with its multiple input ports. All are inverting in polarity and provide a lowest priority level sensing circuit. The lowest level on Pin 4, 5, or 10 gains control of the duty cycle limit. During normal operation, the δ_{MAX} circuit sends a continuous threshold signal to the PWM comparator, setting a fixed limit on how much the error amplifier is allowed to increase the duty cycle in response to load demand. Figure 22 shows the circuit within the NE/SE5562 which actually controls duty cycle as listed below:

1. Duty cycle ramp-up (slow-start) during power-up. Time constant controlled by external R, C ramp voltage at Pin 5.
2. Slow-start if remote ON/OFF is actuated, if OC2 threshold trips, demagnetization/overvoltage is sensed, or low supply voltage to the internal regulator is sensed (VS≤8.45V).
3. Note that Pin 8 is monitored by the loop fault comparator. When the regulated supply feedback drops below this threshold level (0.955V), the duty cycle is clamped by two diodes in series with a 2kΩ load across Pin 5 to ground. This implies a minimum duty cycle condition as long as the low output level remains.

Referring to the graph in Figure 23, the designer may choose a divider ratio which, when referenced to V_Z, 7.5V, provides an easy duty cycle limit control. For example, a 50% limit results in a ratio of 0.48. Setting R_2 at a nominal value between 10 and 20kΩ and solving for R_1, the proper limit is obtained.

Example:

A duty cycle limit of 50% is required for a forward converter.

$R_2 = 10k\Omega$, find R_1

$$\frac{R_2}{R_1 + R_2} = 0.48$$

$$\therefore R_2 = 0.48\,(R_1 + R_2)$$

$$0.48R_1 = R_2 - 0.48R_2$$

$$\therefore R_1 = \frac{R_2(1 - 0.48)}{0.48}$$

$$= \frac{10k\Omega\ (0.52)}{0.48}$$

$$= 10.8k\Omega$$

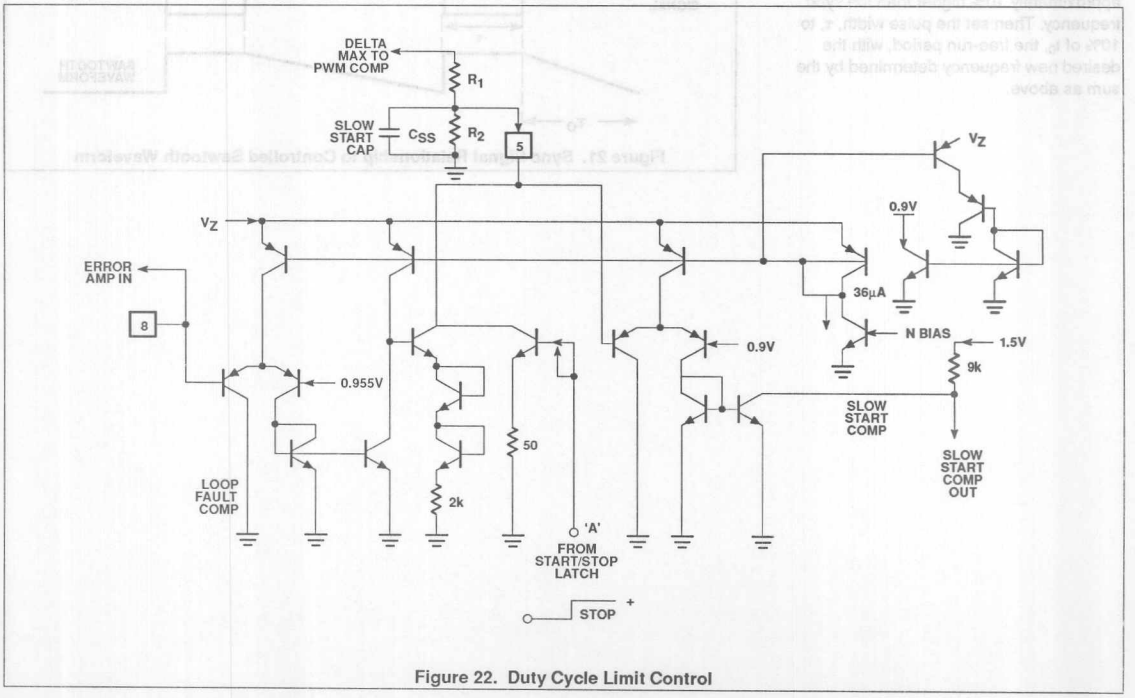


Figure 22. Duty Cycle Limit Control

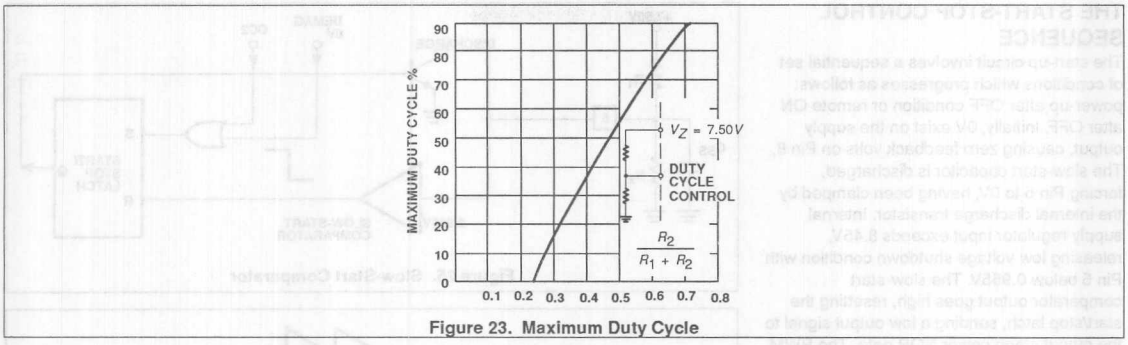


Figure 23. Maximum Duty Cycle

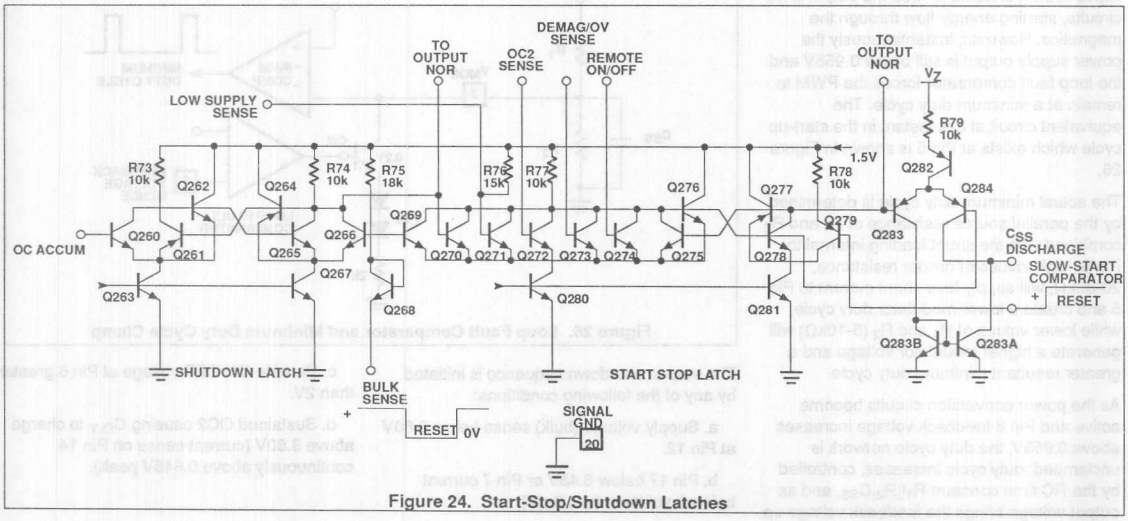


Figure 24. Start-Stop/Shutdown Latches

THE START-STOP CONTROL SEQUENCE

The start-up circuit involves a sequential set of conditions which progresses as follows: power-up after OFF condition or remote ON after OFF. Initially, 0V exist on the supply output, causing zero feedback volts on Pin 8. The slow-start capacitor is discharged, forcing Pin 5 to 0V, having been clamped by the internal discharge transistor. Internal supply regulator input exceeds 8.45V, releasing low voltage shutdown condition with Pin 5 below 0.955V. The slow-start comparator output goes high, resetting the start/stop latch, sending a low output signal to the output stage power NOR gate. The PWM signal is then enabled to feed the output drive circuits, starting energy flow through the magnetics. However, instantaneously the power supply output is still below 0.955V and the loop fault comparator forces the PWM to remain at a minimum duty cycle. The equivalent circuit at this instant in the start-up cycle which exists at Pin 5 is shown in Figure 26.

The actual minimum duty cycle is determined by the parallel source resistance of R_1 and R_2 combined with the shunt loading internal to Pin 5. High values of divider resistance, 20-30kΩ, will supply less shunt current to Pin 5 and create a lower modulator duty cycle, while lower values of R_1 and R_2 (5-10kΩ) will generate a higher modulator voltage and a greater resultant minimum duty cycle.

As the power conversion circuits become active and Pin 8 feedback voltage increases above 0.955V, the duty cycle network is unclamped; duty cycle increases, controlled by the RC time constant $R_1||R_2.C_{SS}$, and as output voltage brings the feedback voltage up to equal the reference voltage, 3.80V, the error amplifier takes control and the supply is in regulation.

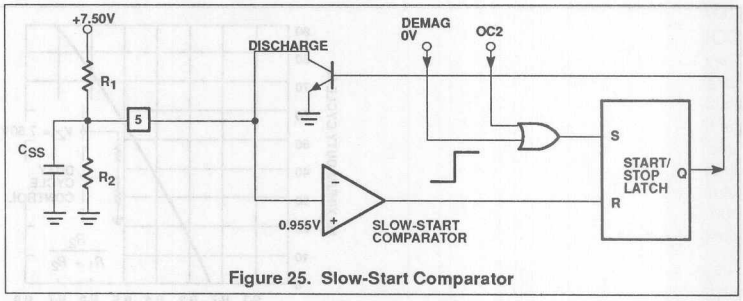


Figure 25. Slow-Start Comparator

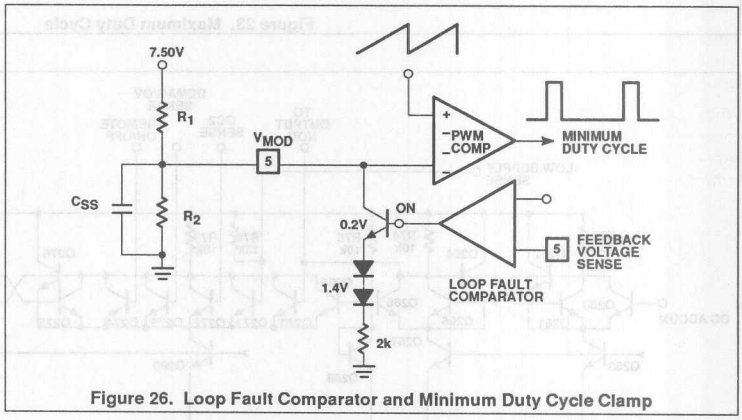


Figure 26. Loop Fault Comparator and Minimum Duty Cycle Clamp

The stop or shutdown sequence is initiated by any of the following conditions:

a. Supply voltage (bulk) sense below 3.80V at Pin 12.

b. Pin 17 below 8.45V or Pin 7 current below level (less than 9mA).

c. Remote ON/OFF voltage at Pin 6 greater than 2V.

d. Sustained OC2 causing C_{DLY} to charge above 3.80V (current sense on Pin 14 continuously above 0.645V peak).

DUAL-LEVEL OVERCURRENT COMPARATORS

The overcurrent sensing circuit (Figure 27) consists of a single PNP input buffer with emitter-follower tied to V_Z, 7.50V, feeding into the base of an NPN split-emitter transistor. This forms the input node to a set of dual-level voltage comparators with references of 0.528 and 0.645V, respectively. Current sources for the comparator are fixed biased NPNs.

The typical transition time delay for an overcurrent fault is 300ns. Bias current at the input averages 500nA.

If the overcurrent sense feature is not used, it is recommended that Pin 14 be tied to ground.

When used for sensing current-derived voltage impulses from the primary driver, a high-speed, low-impedance transient filter network is advised. An example is shown in Figure 28. Keep C_F close to the NE/SE5562.

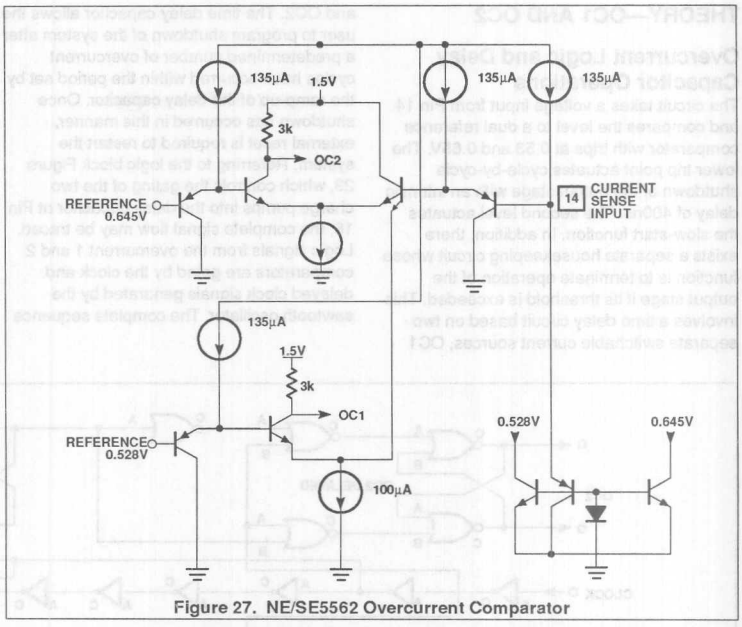


Figure 27. NE/SE5562 Overcurrent Comparator

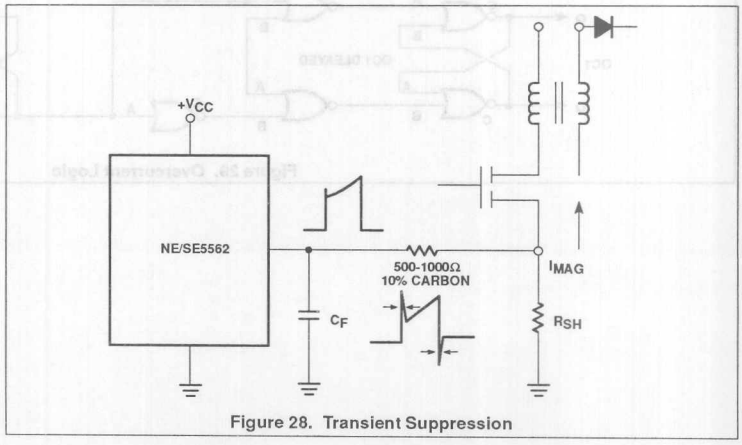


Figure 28. Transient Suppression

THEORY—OC1 AND OC2

Overcurrent Logic and Delay Capacitor Operations

The circuit takes a voltage input from Pin 14 and compares the level to a dual reference comparator with trips at 0.53 and 0.65V. The lower trip point actuates cycle-by-cycle shutdown of the output stage with an intrinsic delay of 400ns. The second level actuates the slow-start function. In addition, there exists a separate housekeeping circuit whose function is to terminate operation of the output stage if its threshold is exceeded. This involves a time delay circuit based on two separate switchable current sources, OC1 and OC2. The time delay capacitor allows the user to program shutdown of the system after a predetermined number of overcurrent cycles have occurred within the period set by the ramp-up of the delay capacitor. Once shutdown has occurred in this manner, external reset is required to restart the system. Referring to the logic block Figure 29, which controls the gating of the two charge pumps into the delay capacitor at Pin 16, the complete signal flow may be traced. Logic signals from the overcurrent 1 and 2 comparators are gated by the clock and delayed clock signals generated by the sawtooth oscillator. The complete sequence for an overcurrent fault may be understood by referring to Figure 30 for OC2. Here it is shown that an OC2 signal exists indicating that the 0.65V threshold has been exceeded by a signal at Pin 14.

Note that an overcurrent pulse within a particular clock frame turns on the respective OC2 charge ramp during the entire next clock frame. Consecutive overcurrent pulses of either OC1 or OC2 magnitude will activate the selected charge pump for the total duration that such overcurrent occurs. The charging cycle will continue until the delay capacitor reaches the 3.86V trip level.

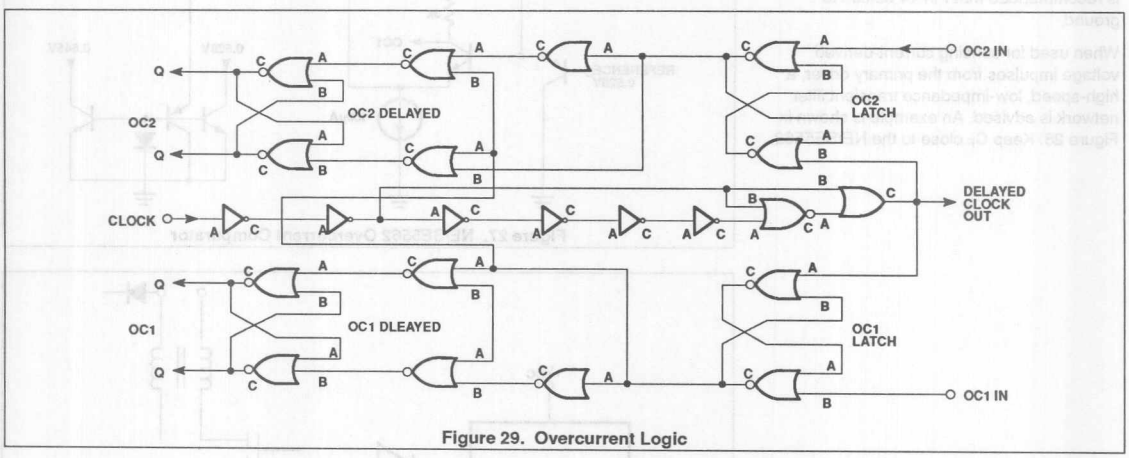


Figure 29. Overcurrent Logic

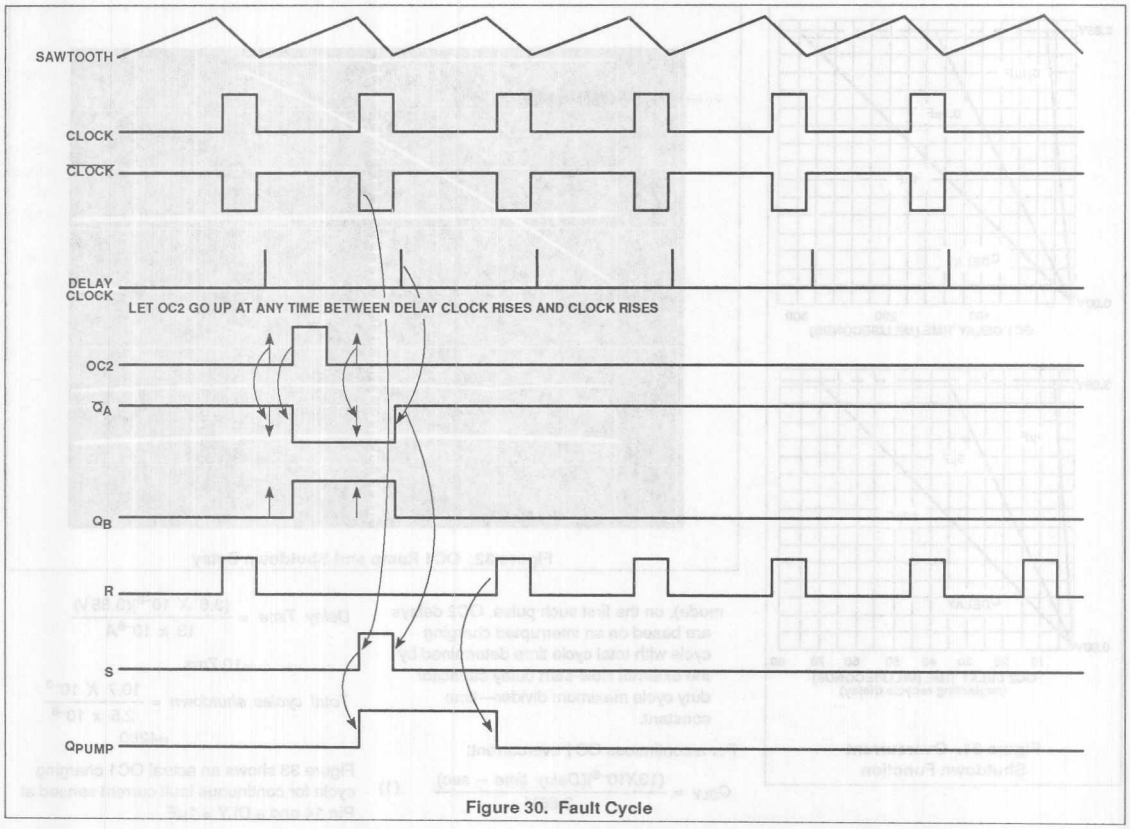


Figure 30. Fault Cycle

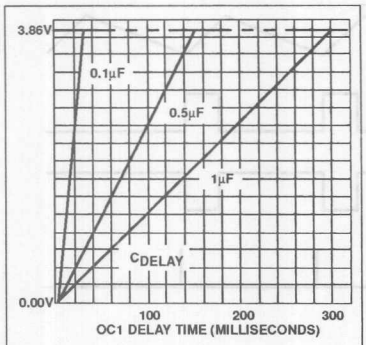


Figure 31. Overcurrent Shutdown Function

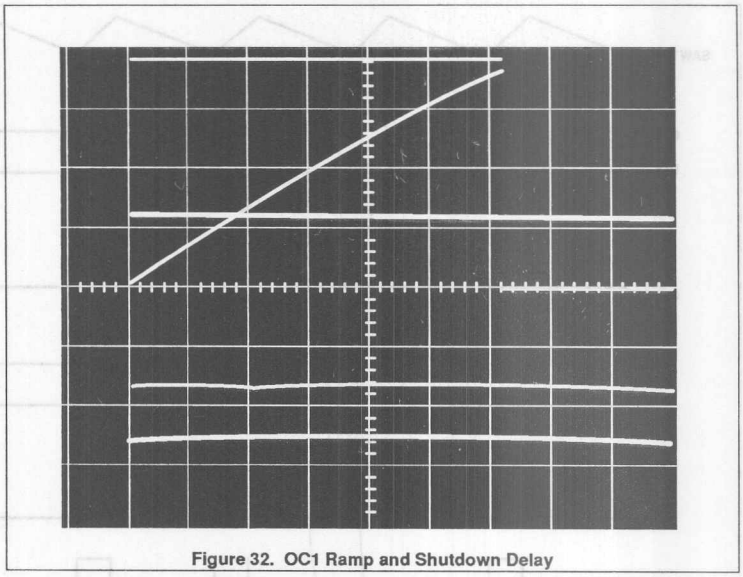


Figure 32. OC1 Ramp and Shutdown Delay

CALCULATING THE DELAY CAPACITOR

Actual delay time for a given capacitor value at Pin 16 may be estimated using the graphs in Figure 31 for OC1 and OC2. By first determining the allowable overcurrent time product for a particular power converter, a capacitor delay value may be calculated.

Note that the OC1 charge pump is typically 13μA while OC2 pumps 550μA into the capacitor. If the exact value is to be calculated for a particular delay requirement, use the following procedure:

1. Determine the level of overcurrent—OC1 or OC2.
2. Find the maximum delay time which the supply may safely sustain for this continuous overcurrent condition. Note that OC1 may be activated on every cycle if OC2 is not reached, causing continuous charging of C-Delay. However, OC2 overcurrent detection causes the supply to go into slow-start shutdown (hiccup mode), on the first such pulse. OC2 delays are based on an interrupted charging cycle with total cycle time determined by the external slow-start delay capacitor duty cycle maximum divider—time constant.

For a continuous OC1 overcurrent:

$$C_{DLY} = \frac{(13X10^{-6})(Delay\ time - sec)}{3.86V} \quad (1)$$

For a continuous OC2 overcurrent:

$$C_{DLY} = \frac{(550X10^{-6})(Delay\ cycles \times 1/f_{SW})}{3.86V} \quad (2)$$

Some downward adjustment of the OC2 capacitor value may be necessary to compensate for the 1-2μA of discharge current at Pin 16 during the delay cycles.

Example: A maximum of 100 OC2 current fault cycles is allowed.

f_{SW} =400kHz, find C_{DLY}

$$C_{DLY} = \frac{(550X10^{-6})(100 \times 1/4 \times 105)}{3.86V}$$

$$= 0.036\mu F$$

Example: OC2/C_{DLY}

Find number of OC1 cycles before shutdown with 0.036μF C_{DLY}.

$$Delay\ Time = \frac{(3.6\ X\ 10^{-8})(3.86V)}{13 \times 10^{-6}A}$$

$$= 10.7ms$$

$$Total\ cycles\ shutdown = \frac{10.7\ X\ 10^{-3}}{2.5 \times 10^{-6}}$$

$$= 4280$$

Figure 33 shows an actual OC1 charging cycle for continuous fault current sensed at Pin 14 and a DLY = 1μF.

BULK-SENSE AUXILIARY COMPARATOR WITH SHUTDOWN

This circuit is intended to act as an automatic low-line detection mechanism. As shown in Figure 33, a voltage divider is connected from the main unregulated DC supply to Pin 12. The lower divider resistor may be a potentiometer of 5-10kΩ resistance with center-tap connected to Pin 13. The comparator which senses Pin 12 voltage is referenced to 3.80V and Pin 12 divider voltage must be greater than this voltage by a sufficient margin to operate within the prescribed low-line limits. For instance, if a line voltage drop of 25% is considered the shutdown threshold, then V_{12} should be calculated for a nominal operating voltage as shown in Figure 33.

When the line voltage drops more than 25%, the output stage is disabled. With the hysteresis connected as shown and the pot adjusted near midway, the line voltage will have to exceed $V_{NOMINAL}$ before the supply will restart. The hysteresis control may then be calibrated for the desired overexcursion before restart. This prevents unstable circuit chatter.

The reset switch provides a means for resetting the shutdown latch after overcurrent faults have charged C_{DLY} to its trip threshold. This also provides a discharge path for the delay capacitor. Figure 34 shows internal circuit.

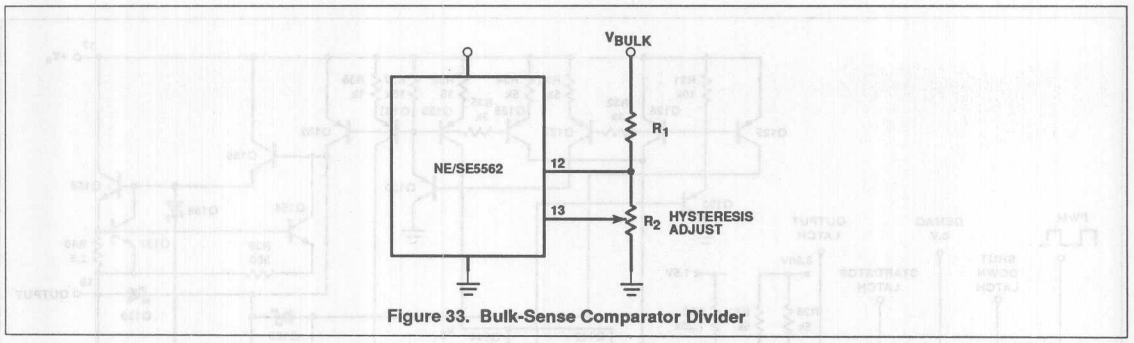


Figure 33. Bulk-Sense Comparator Divider

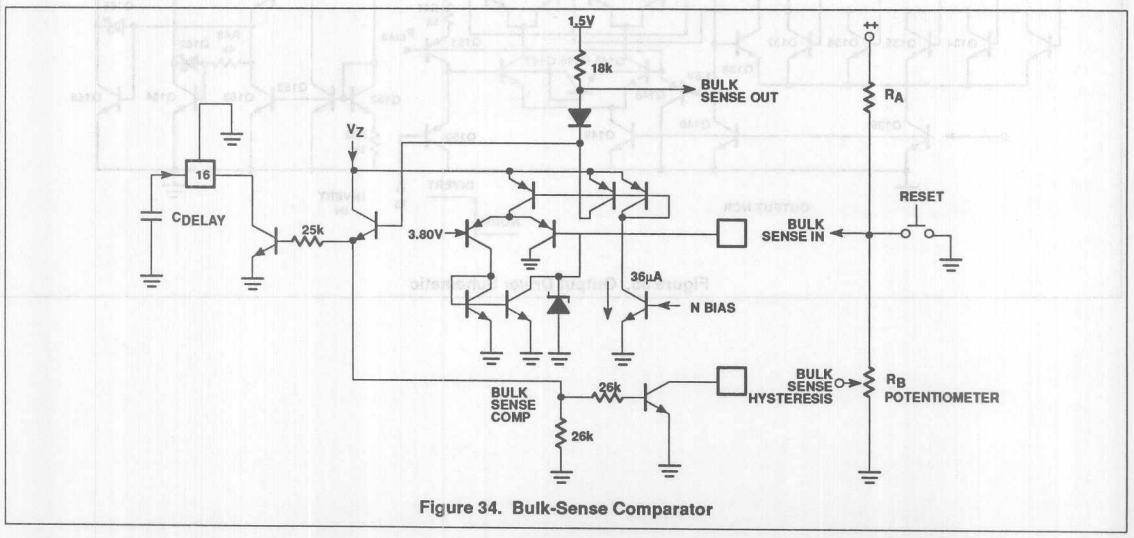


Figure 34. Bulk-Sense Comparator

THE OUTPUT DRIVE STAGE

The output stage contains the power NOR inhibit gate, invert logic function, and source-sink drivers. The driver stage is capable of sourcing and sinking 100mA at frequencies up to 600kHz. The output transistors are Schottky clamped to prevent saturation and the resultant switching delay due to stored charge. A 2.5Ω current sense resistor in the emitter of Q419 serves to drive active clamp Q427 when the output sources more than 200mA. This places a limit on the peak current available during instantaneous charging of a power MOS FET gate. This feature protects the output stage from inadvertent catastrophic overload.

When sinking current, the output is clamped to a maximum of 1.4V. Output swing for positive output is typically V_S-1.9V at 100mA sourcing. Rise time for a 2000pF load at Pin 19 is typically 160ns with a fall time of 80ns.

The power NOR gate provides a fast response inhibit function to shutdown the output in the event of a number of different fault conditions. All inputs are internal to the device and do not appear directly on the external pins as is shown on Figure 35.

The additional flexibility of an invert control allows the polarity at the output during duty cycle to be reversed. This provides a simple means of designing with P-channel power MOS FETs without adding external inverters. The invert logic is controlled by a simple logic signal at Pin 15. Grounding will cause the output to be a normal positive output and a high level gives inverted output.

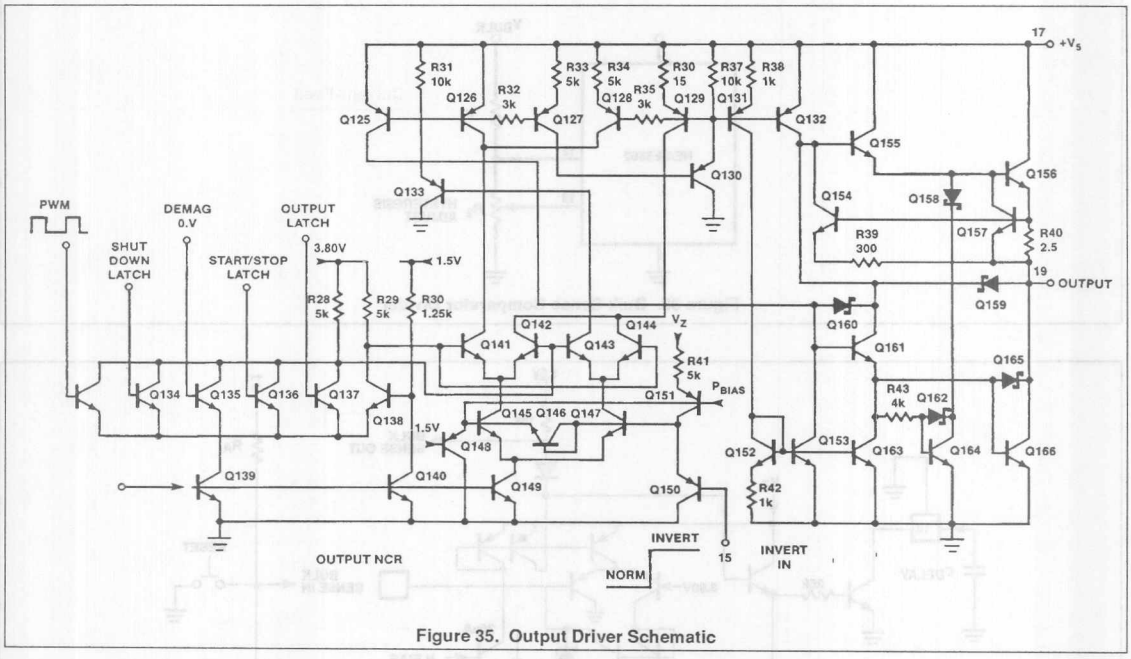


Figure 35. Output Driver Schematic

THE INTERNAL VOLTAGE REGULATOR

The internal regulator is configured to provide for external supply to the NE/SE5562 from either a voltage feed or a current feed.[1]

For the current-fed mode, a series-dropping resistor may be used to power the device from voltages greater than 18V with current supply of 15 to 25mA. Note that supply current stated in the data sheet is for the device only without load on the output or V_Z. Drive currents also are pulse-related and thus reflect frequency components onto the current-feed circuit. These must be filtered out at Pin 7 with adequately large capacitors in order to prevent motor-boating (see Figure 36 and Figure 37).

Input current to Pin 7 flows through Zeners Z_1 and Z_2, and short regulator transmitter QR. A differential amplifier with 3.80V reference provides feedback to regulate V_S to 15V.

In the voltage-fed mode using Pin 17, the Zeners prevent current flow through QR for input voltages less than 19V.

Power dissipation of the device must stay within the allowable package limits. These limits are derived from the thermal characteristics of the particular package chosen. The NE5562N plastic package is capable of operating within the temperature range (ambient) of 0 to +70°C. This rating applies to the surface-mount product NE5562D also. Obviously, the power dissipation of the "D" package is lower than the standard DIP. Thermal resistance for the various packages are:

20-Pin plastic—NE5562N/SE5562N: θ_{JA} 61°C/W

20-Pin glass/ceramic—NE5562F/SE5562F: θ_{JA} 90°C/W

20-Pin SO: -55 to +85°C/W (board-dependent)

NOTE:

1. See Figures 5 and 6 for internal Regulator Response Curves.

Design Example—An NE5562N is operated at 40°C ambient in the voltage-fed mode with V_S=15V; assume I_S=22mA average:

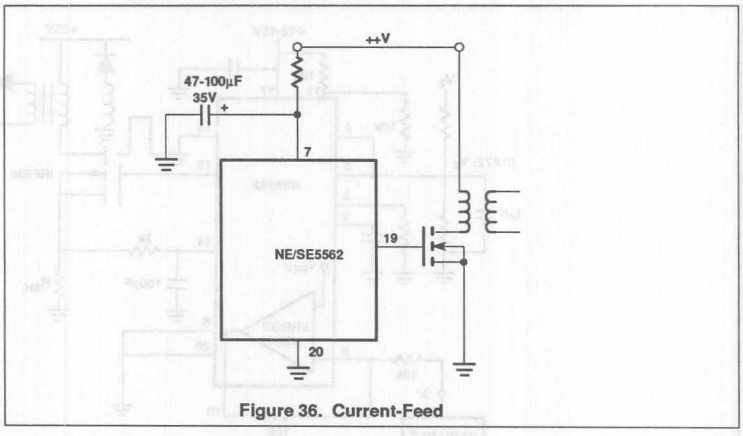


Figure 36. Current-Feed

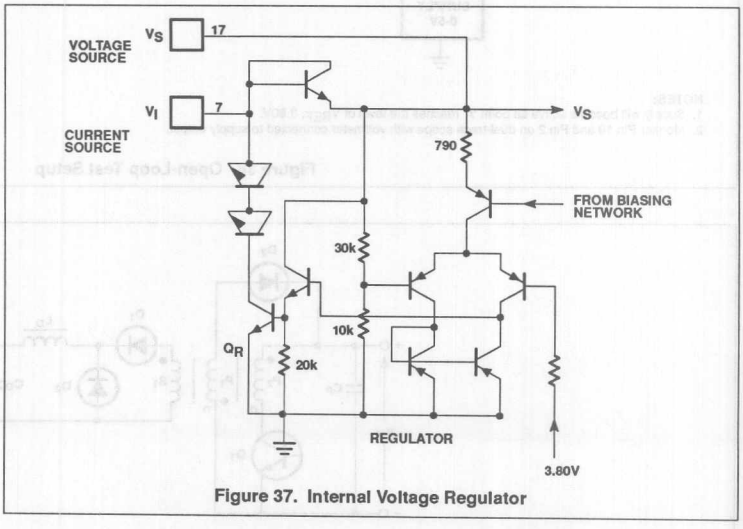


Figure 37. Internal Voltage Regulator

$\therefore P_D = (22 \times 10^{-3})\ (15)$
$= 330mW$

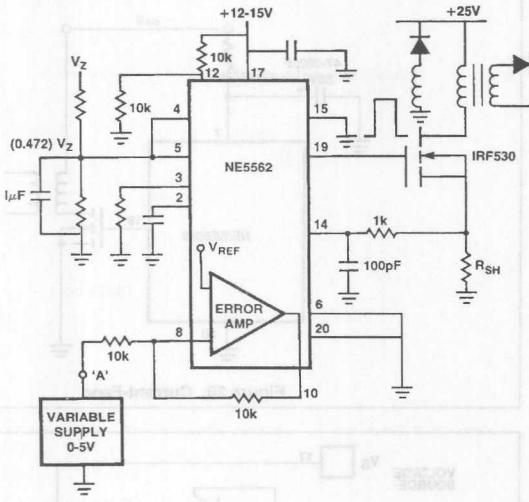
Solving for the temperature rise from ambient to the IC functions:

Temperature rise = 61°C/W×0.33W
= 20.1°C

Junction temperatures will be 20.1°C above average ambient temperatures which is 40°C

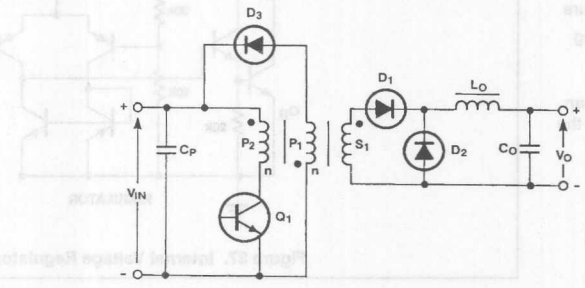
T_J=40°C 20.1°C 60.1°C

The allowable maximum junction temperature is 150°C 125°C is more conservative. The conditions of this example are safe.



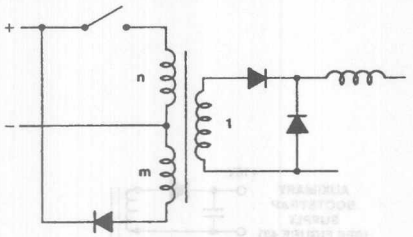
NOTES:
1. Supply will become active as point 'A' reaches the level of V_{REF}, 3.80V.
2. Monitor Pin 19 and Pin 2 on dual-trace scope with voltmeter connected to supply output.

Figure 38. Open-Loop Test Setup



NOTE:
The P_1 clamp winding prevents collector voltage from exceeding 2X VIN during off time.

Figure 39. Forward Converter



To Prevent Core Saturation Due to Flux Staircasing

$$\delta_{max} < 1 - \frac{m}{m+n} \quad \text{if } m = n \; \delta_{max} < .5$$

Demagnetization of Core

$$V_{CEmax} = V_{imax} \; X \; \frac{m+n}{m} \qquad (V)$$

Maximum Voltage Across Transistor

Figure 40. Forward Converter Design Formulas

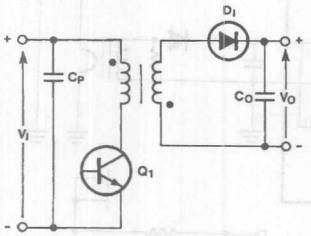


Figure 41. Isolated Secondary

Flyback Converter Design

Flyback Converter

Advantages:

- Simple circuit. Only one inductive component even with line isolation.
- Economic. Low component count, low cost.
- Work over large input voltage variations.
- Can accommodate multiple outputs.

Disadvantages:

- Large output ripple current due to discontinuous energy transfer.
- Large output capacitor; has to supply part of the load current.
- Low leakage inductance required to prevent high voltage spikes at the switching transistors.
- Relatively large core volume for the output power. Core driven in one direction only.

Design Parameters for Flyback Inductor

Input

- Minimum input voltage
- Maximum input voltage

Output

- Output voltage or voltages
- Output current or currents
- Output load

Frequency of Operation

Estimate of Overall Efficiency. (η)

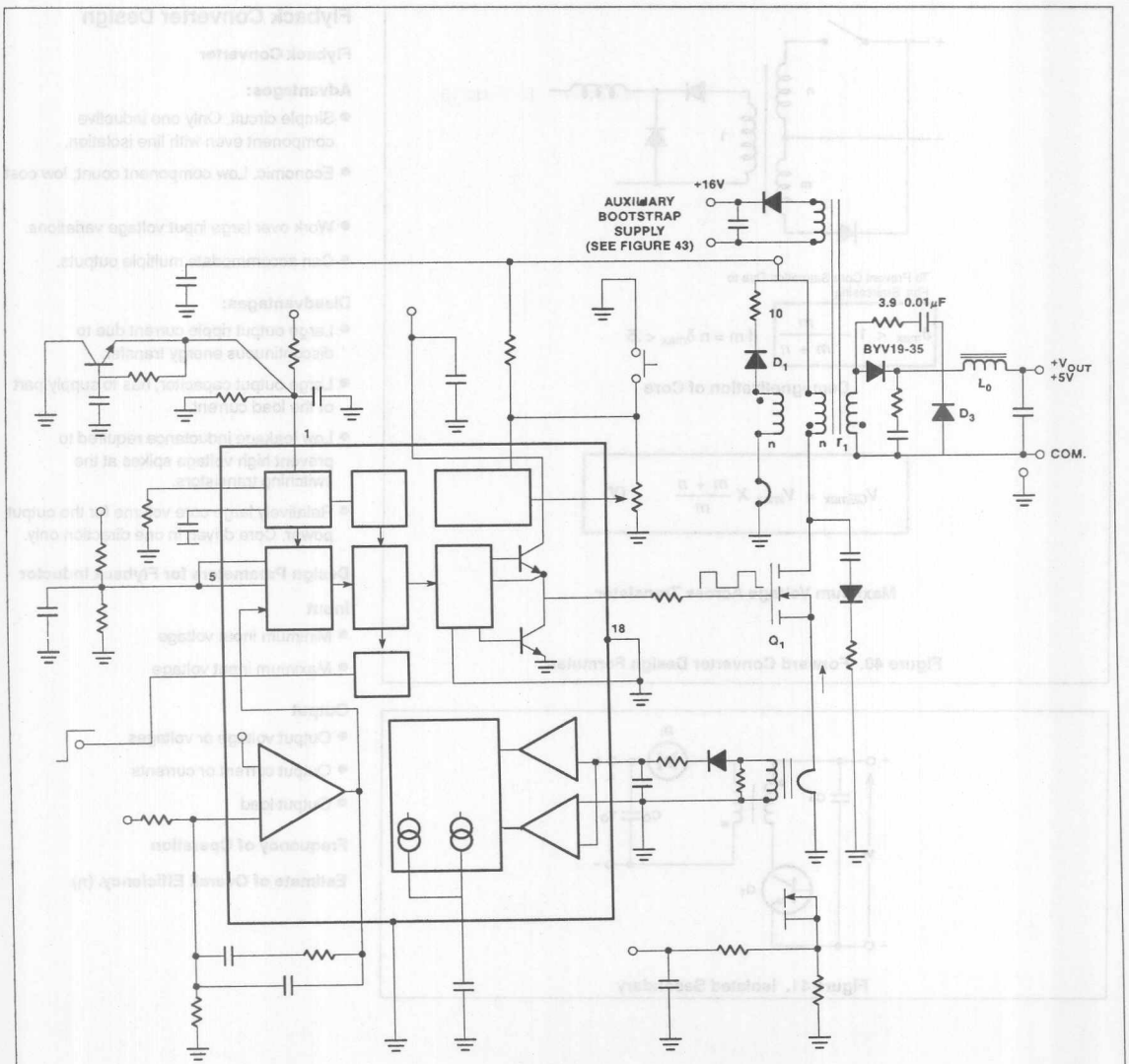


Figure 42. Forward Converter, 100W – 5V

Switched-mode power supply control circuit NE/SE5562

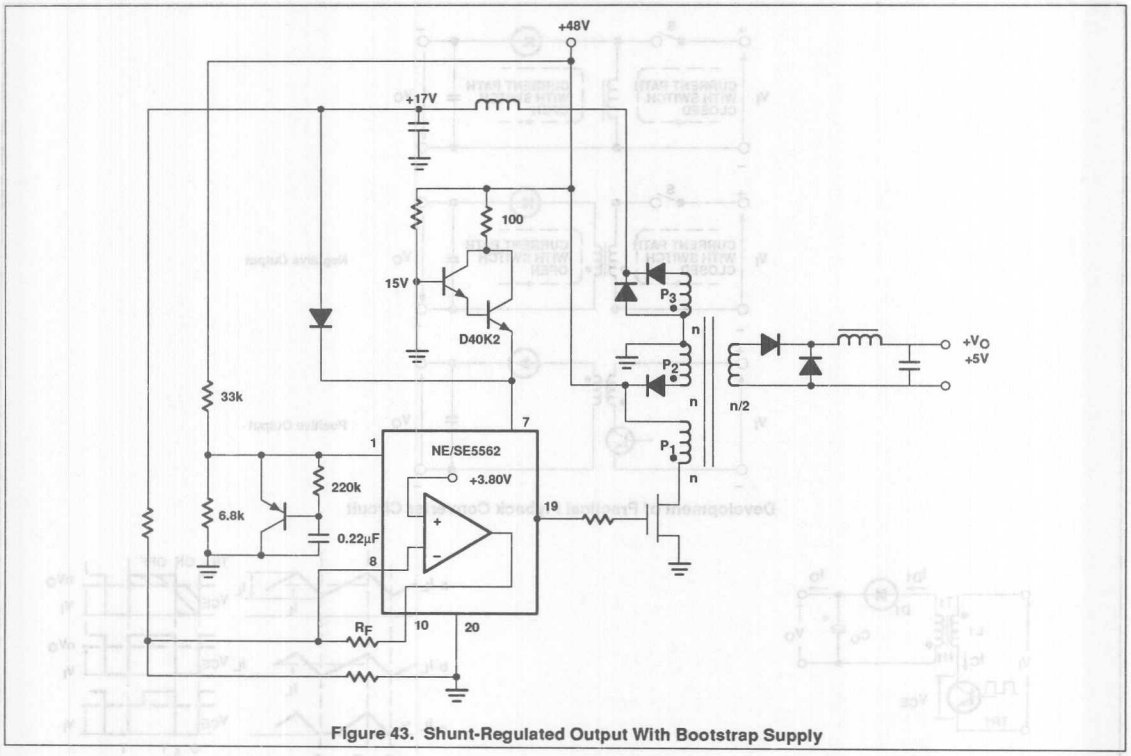
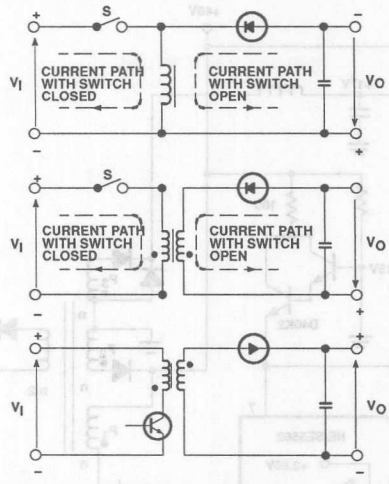
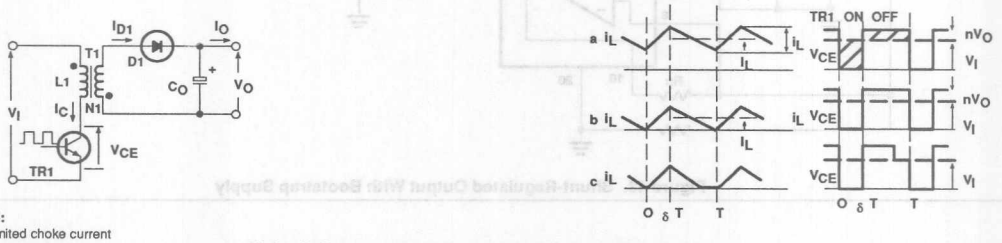


Figure 43. Shunt-Regulated Output With Bootstrap Supply



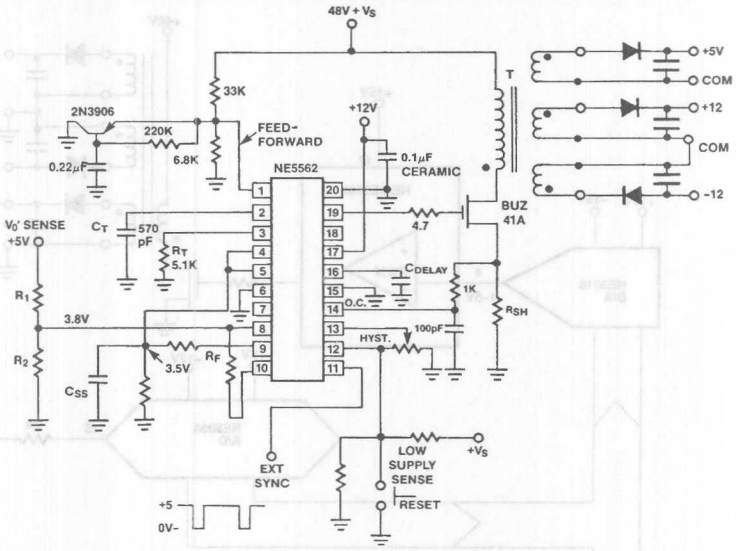
Development of Practical Flyback Converter Circuit



NOTES:
a. Unlimited choke current
b. Interrupted choke current

Flyback Converter and Current and Voltage Waveforms

Figure 44.



NOTE:
400kHz operation with feed-forward line reulation and cycle-by-cycle current timing.

Figure 45. NE5562 Flyback Converter

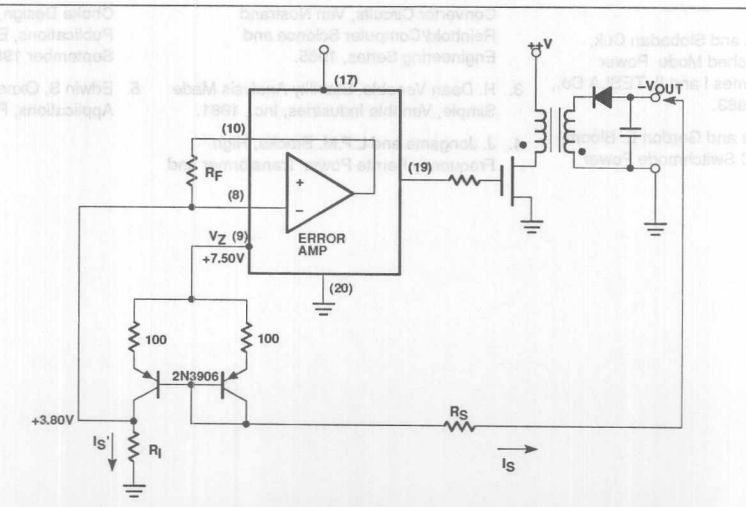


Figure 46. Negative Output Regulator Using Current Mirror

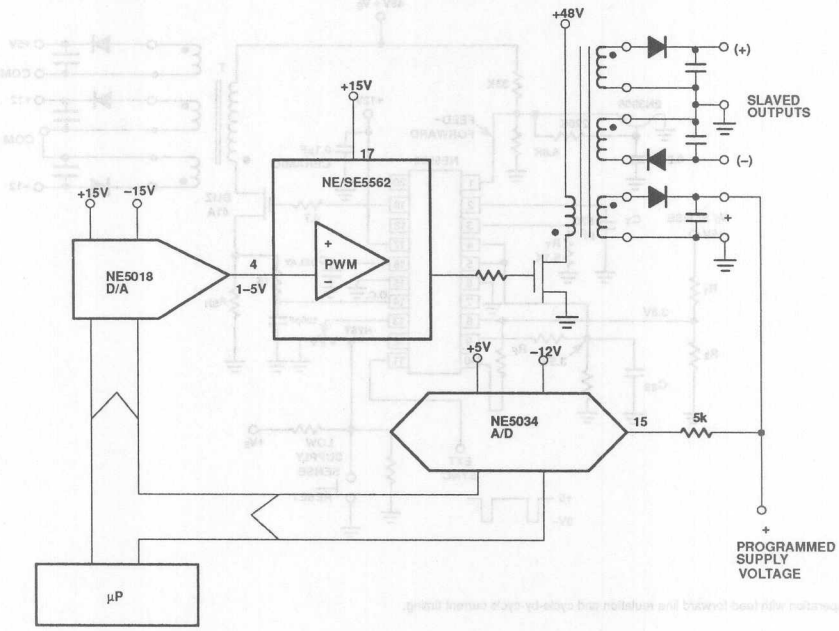


Figure 47. Microprocessor Controlled SMPS

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5. Edwin S. Oxner, Power FETs and Their Applications, Prentice-Hall, 1982.

Switched-mode power supply controller NE5568

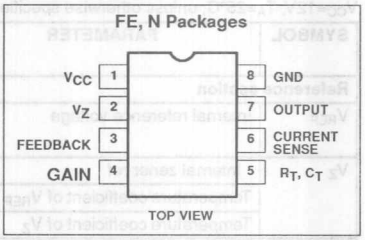
DESCRIPTION

The NE5568 is a control circuit for use in switched mode power supplies. It contains an internal temperature-compensated supply, PWM, sawtooth oscillator, over-current sense latch, and output stage. The device is intended for low cost SMPS applications where extensive housekeeping functions are not required. The NE5568 is a selected version of the NE5561.

FEATURES

- Micro-miniature (D) package
- Pulse width modulator
- Current limiting (cycle by cycle)
- Sawtooth generator
- Stabilized power supply
- Double-pulse protection
- Internal temperature-compensated reference

PIN CONFIGURATION



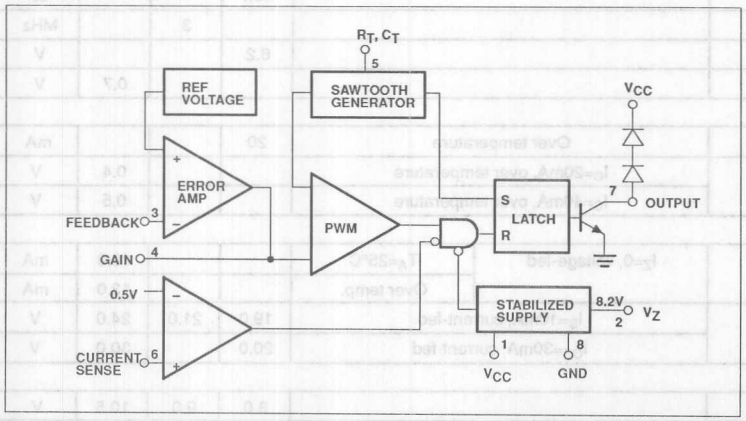
APPLICATIONS

- Switch mode power supplies
- DC motor controller inverter
- DC/DC converter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5568N
8-Pin Cerdip	0 to +70°C	NE5568FE

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	18	V
I_{OUT}	Output current	40	mA
	Output duty cycle	98	%
P_D	Max total power dissipation	0.75	W
T_A	Operating temperature range	0 to 70	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}=12V, T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		NE5568			UNIT
				Min	Typ	Max	
Reference section							
V_{REF}	Internal reference voltage	T_A=25°C		3.69	3.75	3.84	V
		Over temperature		3.66		3.87	V
V_Z	Internal zener ref	I_L=7mA		7.8	8.2	8.8	V
	Temperature coefficient of V_{REF}				± 100		ppm/°C
	Temperature coefficient of V_Z				± 200		ppm/°C
Oscillator section							
f	Frequency range	Over temperature		50		100k	Hz
	Initial accuracy	R_T and C_T Constant			5		%
	Duty cycle range	f_o=20kHz		0		98	%
Current limitng							
I_{IN}	Input current	Pin 6=250mV	T_A=25°C		-2	-10	µA
			Over temp.			-20	µA
	Single pulse inhibit delay	Inhibit delay time for 20% overdrive at	I_{OUT}=20mA		0.88	1.10	µs
			I_{OUT}=40mA		0.7	0.8	µs
	Current limit trip level			0.400	0.500	0.600	V
Error amplifier							
	Open-loop gain				60		dB
	Feedback resistor			10k			Ω
BW	Small-signal bandwidth				3		MHz
V_{OH}	Output voltage swing			6.2			V
V_{OL}	Output voltage swing					0.7	V
Output stage							
I_{OUT}	Output current	Over temperature		20			mA
V_{CE}	Saturation	I_C=20mA, over temperature				0.4	V
		I_C=40mA, over temperature				0.5	V
Supply voltage/current							
I_{CC}	Supply current	I_Z=0, voltage-fed	T_A=25°C			10.0	mA
			Over temp.			13.0	mA
V_{CC}	Supply voltage	I_S=10mA, current-fed		19.0	21.0	24.0	V
		I_{CC}=30mA, current-fed		20.0		30.0	V
Low supply protection							
	Pin 1 threshold			8.0	9.0	10.5	V

NOTES:
All curves and applications of NE5561 apply exactly

SMPS control circuit

SG3524

DESCRIPTION

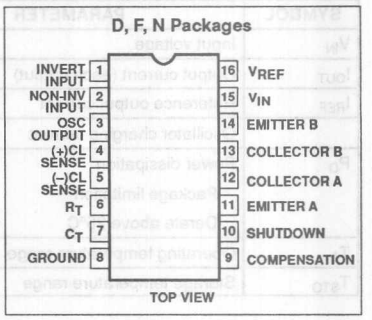
This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse-width modulator, pulse steering flip-flop, dual alternating output switches and current-limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer-coupled DC-to-DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG3524 is designed for commercial applications of 0°C to +70°C.

FEATURES

- Complete PWM power control circuitry
- Single ended or push-pull outputs
- Line and load regulation of 0.2%
- 1% maximum temperature variation
- Total supply current is less than 10mA
- Operation beyond 100kHz

PIN CONFIGURATION

D, F, N Packages

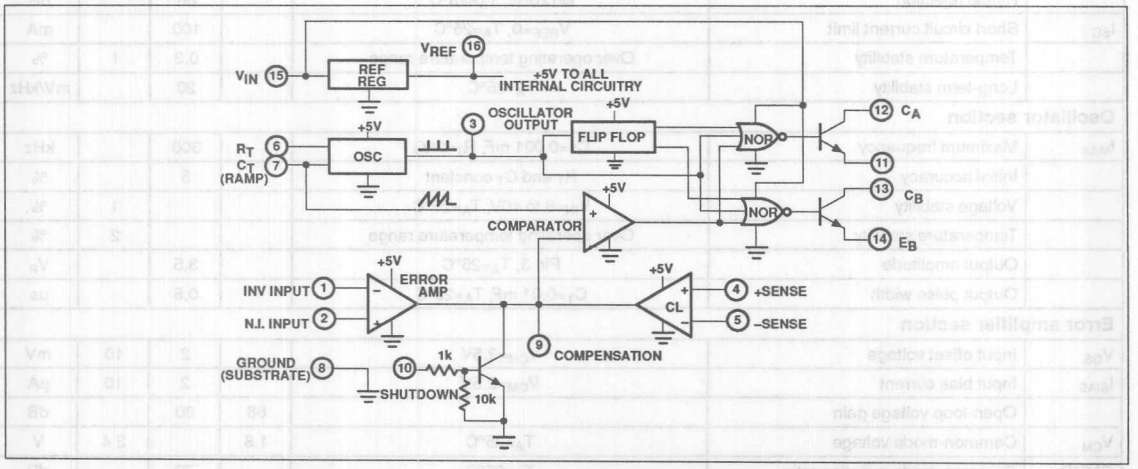


TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	SG3524N
16-Pin Cerdip	0 to +70°C	SG3524F
16-Pin SO	0 to +70°C	SG3524D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{IN}	Input voltage	40	V
I_{OUT}	Output current (each output)	100	mA
I_{REF}	Reference output current	50	mA
	Oscillator charging current	5	mA
P_D	Power dissipation		
	Package limitation	1000	mW
	Derate above 25°C	8	mW/°C
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

T_A=0°C to +70°C, V_{IN}=20V, and f=20kHz, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Reference section						
V_{OUT}	Output voltage		4.6	5.0	5.4	V
	Line regulation	V_{IN}=8 to 40V		10	30	mV
	Load regulation	I_L=0 to 20mA		20	50	mV
	Ripple rejection	f=120Hz, T_A=25°C		66		dB
I_{SC}	Short circuit current limit	V_{REF}=0, T_A=25°C		100		mA
	Temperature stability	Over operating temperature range		0.3	1	%
	Long-term stability	T_A=25°C		20		mV/kHz
Oscillator section						
f_{MAX}	Maximum frequency	C_T=0.001 mF, R_T=2kΩ		300		kHz
	Initial accuracy	R_T and C_T constant		5		%
	Voltage stability	V_{IN}=8 to 40V, T_A=25°C			1	%
	Temperature stability	Over operating temperature range			2	%
	Output amplitude	Pin 3, T_A=25°C		3.5		V_P
	Output pulse width	C_T=0.01 mF, T_A=25°C		0.5		µs
Error amplifier section						
V_{OS}	Input offset voltage	V_{CM}=2.5V		2	10	mV
I_{BIAS}	Input bias current	V_{CM}=2.5V		2	10	µA
	Open-loop voltage gain		68	80		dB
V_{CM}	Common-mode voltage	T_A=25°C	1.8		3.4	V
CMRR	Common-mode rejection ratio	T_A=25°C		70		dB
BW	Small-signal bandwidth	A_V=0dB, T_A=25°C		3		MHz
V_{OUT}	Output voltage	T_A=25°C	0.5		3.8	V
Comparator section						
	Duty cycle	% each output "ON"	0		45	%
	Input threshold	Zero duty cycle		1		V
	Input threshold	Maximum duty cycle		3.5		V
I_{BIAS}	Input bias current			1		µA

DC ELECTRICAL CHARACTERISTICS (Continued)

T_A = 0°C to +70°C, V_{IN} = 20V, and f = 20kHz, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Current limiting section						
	Sense voltage	Pin 9=2V with error amplifier set for maximum out, T_A=25°C	180	200	220	mV
	Sense voltage T.C.			0.2		mV/°C
V_{CM}	Common-mode voltage		-1		+1	V
Output section (each output)						
	Collector-emitter voltage (breakdown)		40			V
	Collector-leakage current	V_{CE}=40V		0.1	50	µA
	Saturation voltage	I_C=50mA		1	2	V
	Emitter output voltage	V_{IN}=20V	17	18		V
t_R	Rise time	R_C=2kΩ, T_A=25°C		0.2		µs
t_F	Fall time	R_C=2kΩ, T_A=25°C		0.1		µs
Total standby current						
	(excluding oscillator charging current, error and current limit dividers, and with outputs open)	V_{IN}=40V		8	10	mA

THEORY OF OPERATION

Voltage Reference

An internal series regulator provides a nominal 5V output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5V supply by connecting Pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0V.

This reference regulator may be used as a 5V source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher currents with an external PNP as shown in Figure 1.

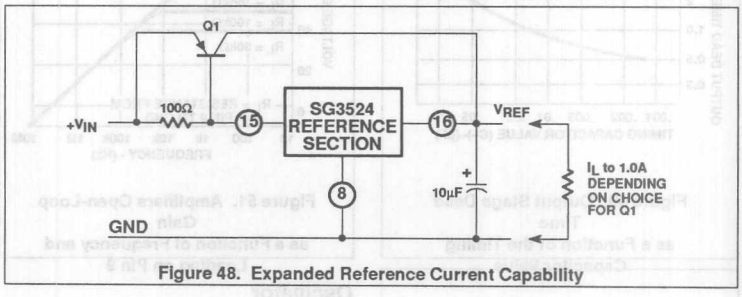
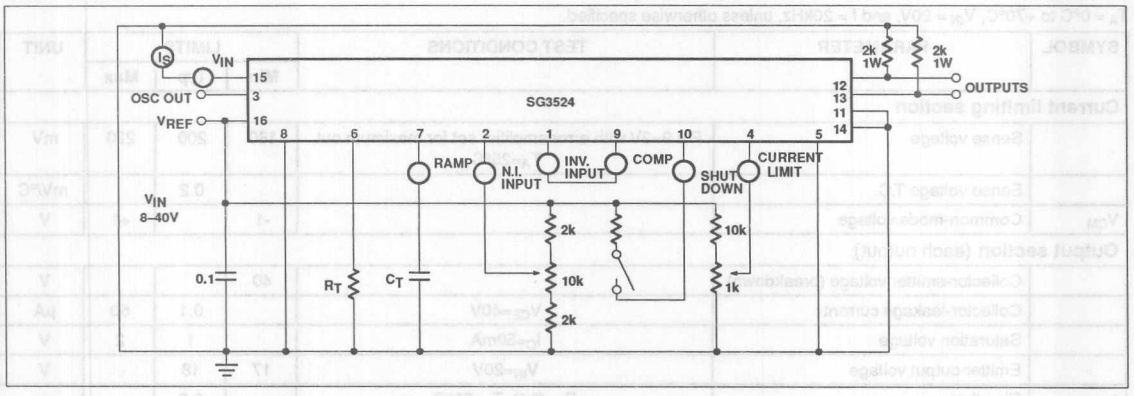


Figure 48. Expanded Reference Current Capability

TEST CIRCUIT



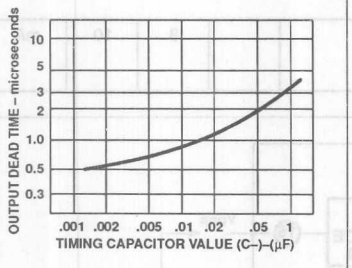


Figure 49. Output Stage Dead Time as a Function of the Timing Capacitor Value

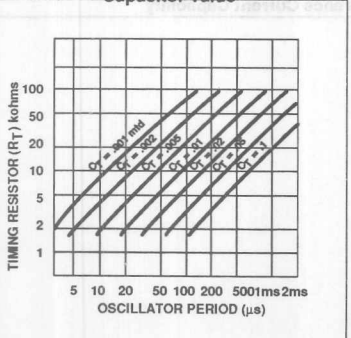


Figure 50. Oscillator Period as a Function of R_T and C_T

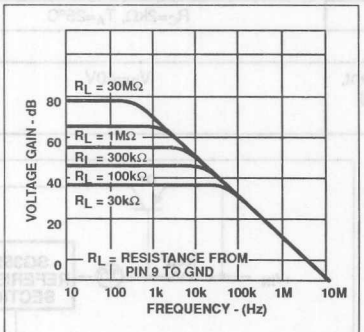


Figure 51. Amplifiers Open-Loop Gain as a Function of Frequency and Loading on Pin 9

Oscillator

The oscillator in the SG3524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series-connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to 3.6 V ÷ R_T and should be kept within the approximate range of 30μA to 2mA; i.e., 1.8k<R_T<100k.

The range of values for C_T also has limits as the discharge time of C_T determines the pulse-width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 2. A pulse width below approximately 0.5μs may allow false triggering of one output by removing the blanking pulse prior to the flip-flop's reaching a stable state. If small values of C_T must be used, the pulse-width may still be expanded by adding a shunt capacitance (≅100pF) to ground at the oscillator output. [(Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse-width slightly.)] Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between 0.001 and 0.1 μF.

The oscillator period is approximately t=R_TC_T where t is in microseconds when R_T=Ω and C_T=μF. The use of Figure 3 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each output's duty cycle is 0-45% and the overall frequency is one-half that of the oscillator.

External Synchronization

If it is desired to synchronize the SG3524 to an external clock, a pulse of ≅+3V may be applied to the oscillator output terminal with R_TC_T set slightly greater than the clock period. The same considerations of

pulse-width apply. The impedance to ground at this point is approximately 2kΩ.

If two or more SG3524s must be synchronized together, one must be designated as master with its R_TC_T set for the correct period. The slaves should each have an R_TC_T set for approximately 10% longer period than the master with the added requirement that C_T(slave)=one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse—which occurs first and has a wider pulse width—will reset the slave units.

Error Amplifier

This circuit is a simple differential input transconductance amplifier. The output is the compensation terminal, Pin 9, which is a high-impedance node ($R_L \cong 5M\Omega$). The gain is

$$A_V = g_M R_L = \frac{8\ I_C\ R_L}{2kT} \approx 0.002 R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from Pin 9 to ground, as shown in Figure 4.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 4 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain crossover at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series RC combination between Pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50kΩ plus 0.001μF.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200μA can pull this point to ground, thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5V reference voltage must be divided down as shown in Figure 5. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open-loop test circuit.

Current Limiting

The current limiting circuitry of the SG3524 is shown in Figure 6.

By matching the base-emitter voltages of Q1 and Q2, and assuming a negligible voltage drop across R_1:

$$\text{Threshold} = V_{BE}(Q1) + I_1R_2 - V_{BE}(Q2)$$

$$= I_1R_2 \cong 200mV$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ±1V common-mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300Hz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage required to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, Pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and to shorten an output pulse, should transformer saturation occur. Another application is to ground Pin 5 and use Pin 4 as an additional shutdown terminal: i.e., the output will be off with Pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 7. This circuit can reduce the short-circuit current (I_{SC}) to approximately one-third the maximum available output current (I_{MAX}).

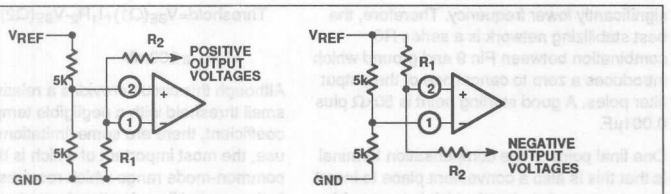


Figure 52. Error Amplifier Biasing Circuits

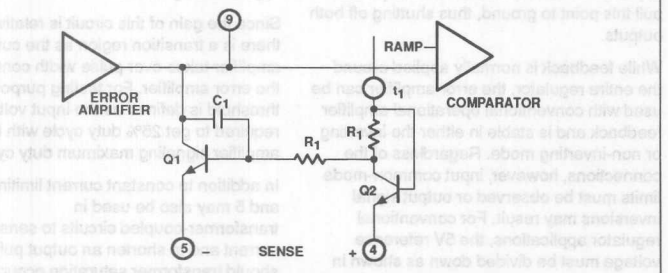
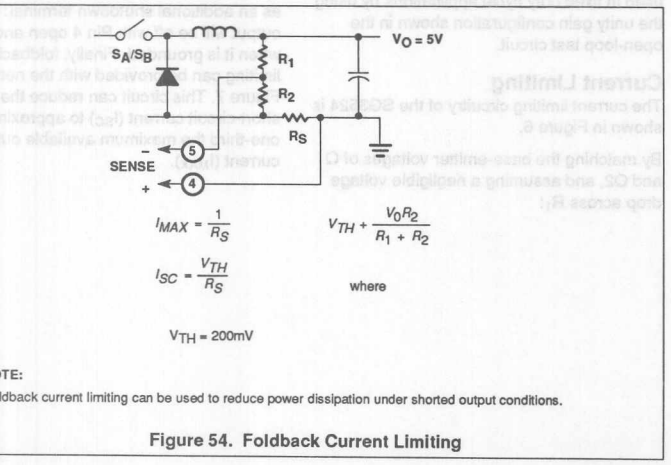


Figure 53. Current Limiting Circuitry of the SG3524



NOTE:
Foldback current limiting can be used to reduce power dissipation under shorted output conditions.

Figure 54. Foldback Current Limiting

Precision voltage regulator

µA723/723C

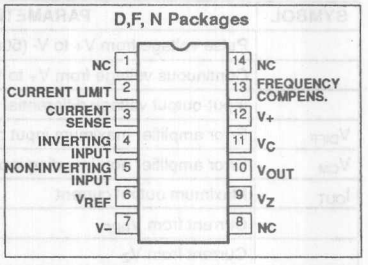
DESCRIPTION

The µA723/µA723C is a monolithic precision voltage regulator capable of operation in positive or negative supplies as a series, shunt, switching, or floating regulator. The 723 contains a temperature-compensated reference amplifier, error amplifier, series pass transistor, and current limiter, with access to remote shutdown.

FEATURES

- Positive or negative supply operation
- Series, shunt, switching, or floating operation
- 0.01% line and load regulation
- Output voltage adjustable from 2V to 37V
- Output current to 150mA without external pass transistor
- µA723 MIL-STD-883A, B, C available

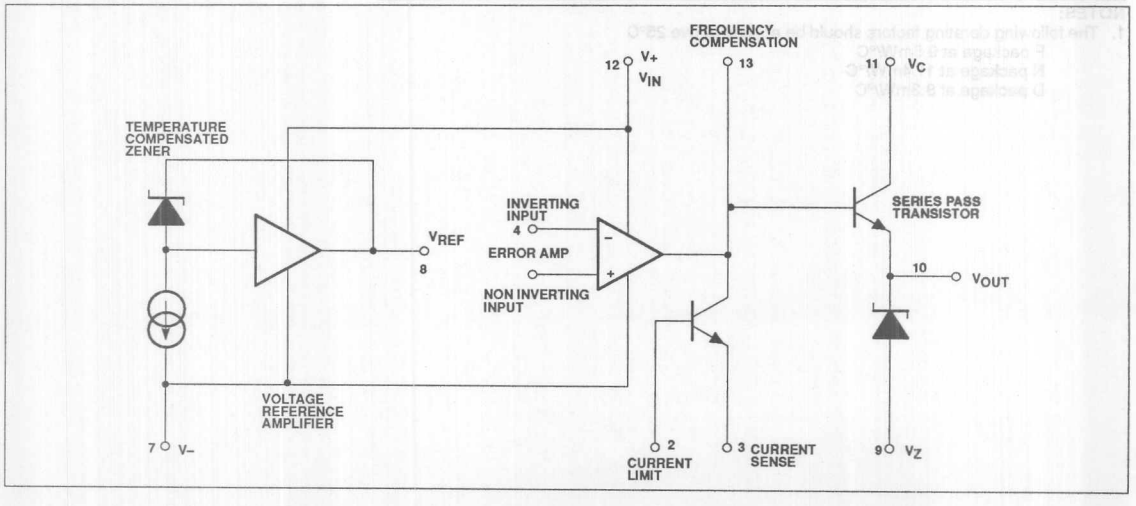
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Ceramic DIP	-55°C to 125°C	µA723F
14-Pin Plastic DIP	0 to 70°C	µA723CN
14-Pin Plastic SO	0 to 70°C	µA723CD

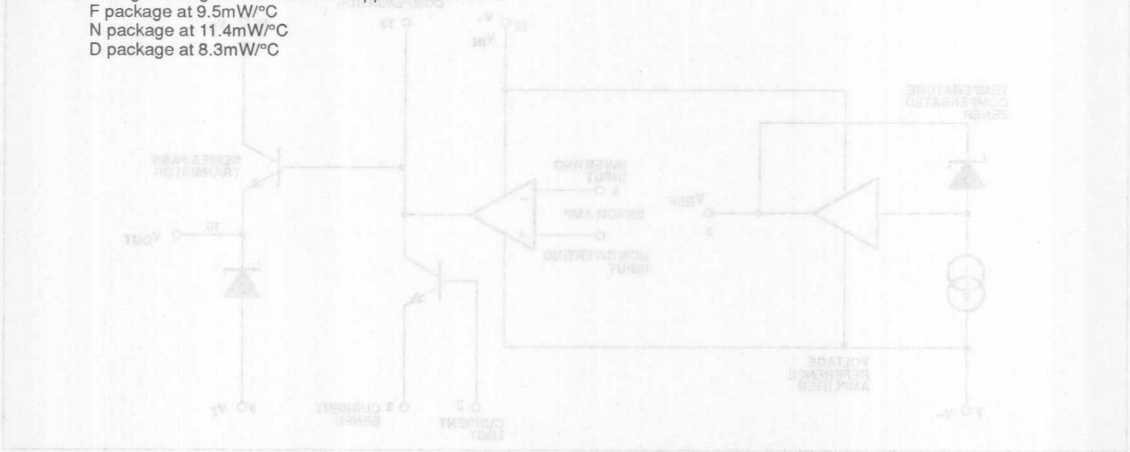
EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Pulse voltage from V+ to V- (50ms)	50	V
	Continuous voltage from V+ to V-	40	V
	Input-output voltage differential	40	V
V_{DIFF}	Error amplifier maximum input differential voltage	±5	V
V_{CM}	Error amplifier non-inverting input (Pin 5) to -V (Pin 7)	8	V
I_{OUT}	Maximum output current	150	mA
	Current from V_{REF}	15	mA
	Current from V_Z	25	mA
P_{MAX}	Maximum power dissipation T_A=25°C (still-air)[1]		
	F package	1190	mW
	N package	1420	mW
	D package	1040	mW
T_A	Operating ambient temperature range		
	µA723	-55 to +125	°C
	µA723C	0 to 70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. The following derating factors should be applied above 25°C
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C



DC ELECTRICAL CHARACTERISTICS

T_A=25°C, unless otherwise specified.[1]

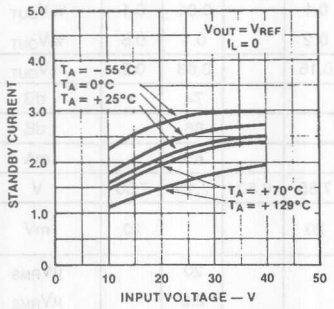
SYMBOL	PARAMETER	TEST CONDITIONS	μA723			μA723C			
			Min	Typ	Max	Min	Typ	Max	
$V_{R\ LINE}$	Line regulation[2]	V_{IN}=12V to V_{IN}=15V		0.01	0.1		0.01	0.1	$\%V_{OUT}$
		V_{IN}=12V to V_{IN}=40V		0.02	0.2		0.1	0.5	$\%V_{OUT}$
$V_{R\ LOAD}$	Load regulation[2]	I_L=1mA to I_L=50mA		0.03	0.15		0.03	0.2	$\%V_{OUT}$
ΔVIN/Δ VO	Ripple Rejection	f=50Hz to 10kHz, C_{REF}=0		74			74		dB
		f=50Hz to 10kHz, C_{REF}=5μF		86			86		dB
I_{OS}	Short-circuit current	R_{SC}=10Ω, V_{OUT}=0		65			65		mA
V_{REF}	Reference voltage	I_{REF}=0.1mA	6.95	7.15	7.35	6.80	7.15	7.50	V
$V_{REF\ (LOAD)}$	Reference voltage change with load	I_{REF}=0.1mA to 5mA			20			20	mV
V_{NOISE}	Output noise voltage	BW=100Hz to 10kHz, C_{REF}=0		20			20		μV_{RMS}
		BW=100Hz to 10kHz, C_{REF}=5μF		2.5			2.5		μV_{RMS}
S	Long-term stability	Tj=Tjmax. TA=25°C for end point measurment		0.1			0.1		%1000 hrs.
I_{SCD}	Standby current drain	I_L=0, V_{IN}=30V		2.3	3.5		2.3	4.0	mA
V_{IN}	Input voltage range		9.5		40	9.5		40	V
V_{OUT}	Output voltage range		2.0		37	2.0		37	V
V_{DIFF}	Input-output voltage differential		3.0		38	3.0		38	V
The following specifications apply over the operating temperature ranges.									
$V_{R\ LINE}$	Line regulation	V_{IN}=12V to V_{IN}=15V			0.3			0.3	$\%V_{OUT}$
$V_{R\ LOAD}$	Load regulation	I_L=1mA to I_L=50mA			0.6			0.6	$\%V_{OUT}$
TC	Average temperature coefficient of output voltage			0.002	0.015		0.003	0.015	%/°C

NOTES:

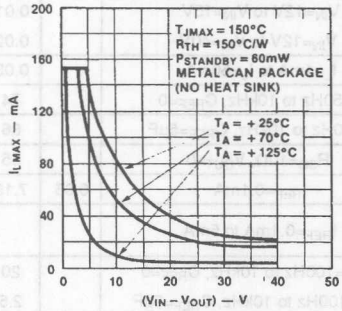
1. V_{IN}=V+=V_C=12V, V-=0V, V_{OUT}=5V, I_L=1mA, R_{SC}=0, C_1=100pF, C_{REF}=0 and divider impedance as seen by error amplifier≤10kΩ.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

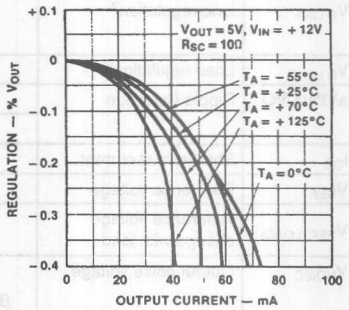
Standby Current Drain as a Function of Input Voltage



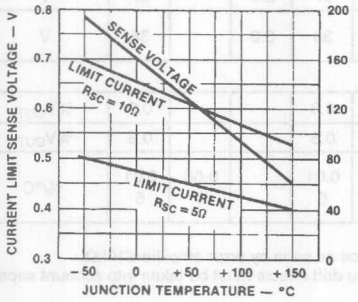
Maximum Load Current as a Function of Input-Output Voltage Differential



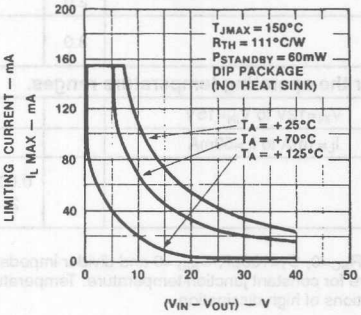
Load Regulation Characteristics with Current Limiting



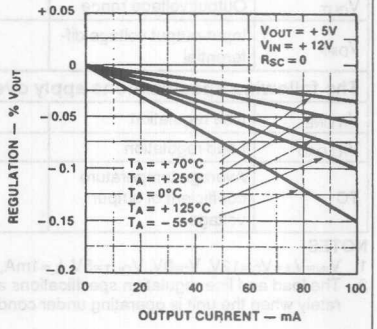
Current Limiting Characteristics as a Function of Junction Temperature



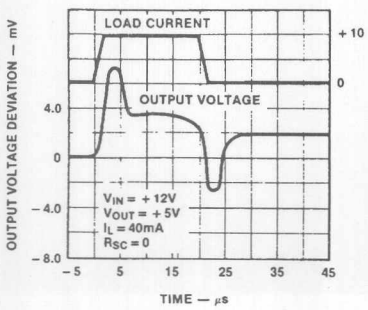
Maximum Load Current as a Function of Input-Output Voltage Differential



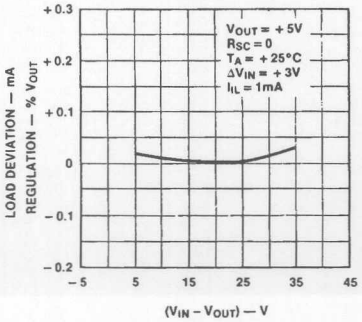
Load Regulation Characteristics Without Current Limiting



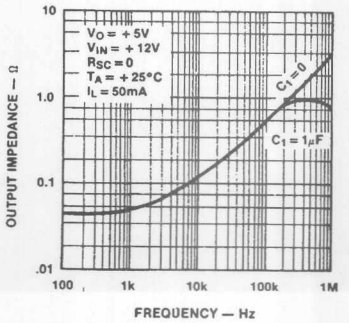
Load Transient Response



Line Regulation as a Function of Input-Output Voltage Differential

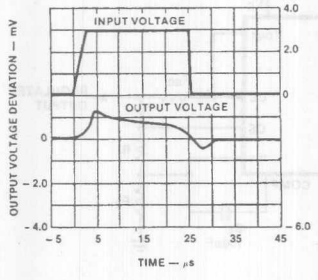


Output Impedance as a Function of Frequency

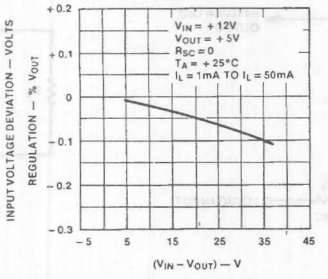


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

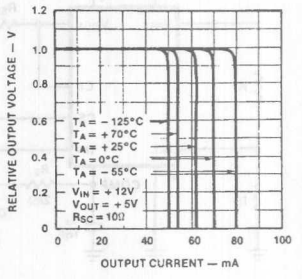
Line Transient Response



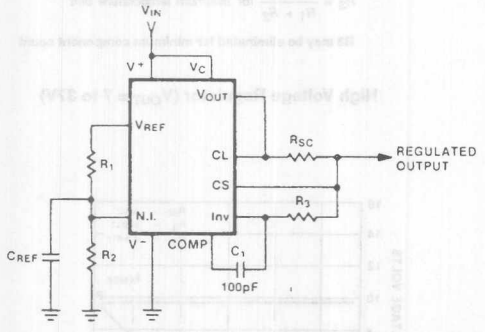
Load Regulation as a Function of Input-Output Voltage Differential



Current Limiting Characteristics



TYPICAL APPLICATIONS

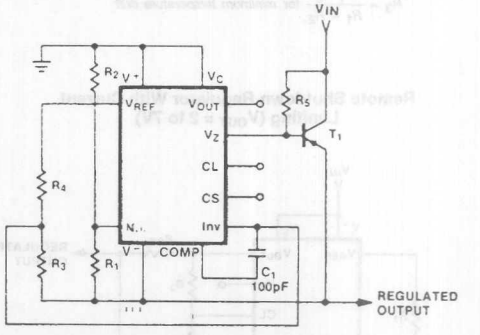


NOTES:

$$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2} \right]$$

$$R_3 = \frac{R_1 R_2}{R_1 + R_2} \text{ for minimum temperature drift}$$

Low Voltage Regulator (V_{OUT} = 2 to 7V)

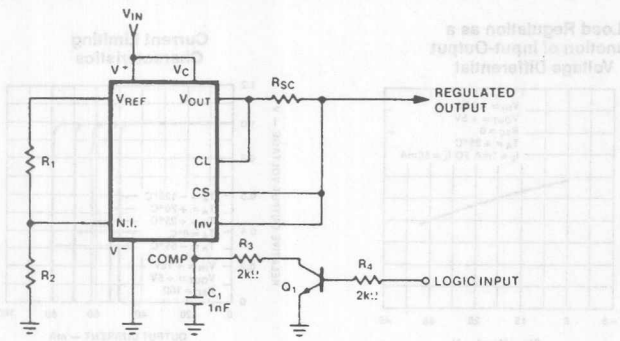


NOTE:

$$V_{OUT} = \left[\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1} \right]; \; R_3 = R_4$$

Negative Voltage Regulator

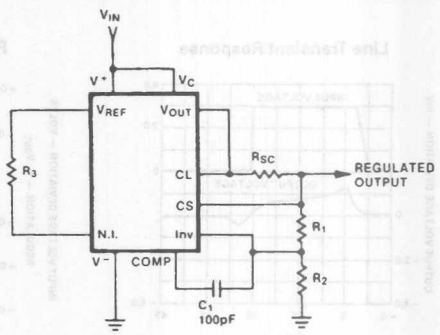
TYPICAL APPLICATIONS (Continued)



NOTE:

$$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2} \right]$$

$$R_3 = \frac{R_1 R_2}{R_1 + R_2} \text{ for minimum temperature drift}$$



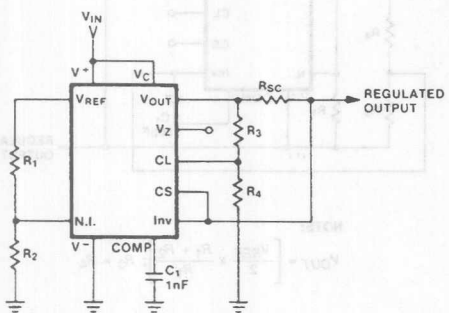
NOTE:

$$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2} \right]; \; R_3 = R_4$$

$$R_3 = \frac{R_1 R_2}{R_1 + R_2} \text{ for minimum temperature drift}$$

R3 may be eliminated for minimum component count

Remote Shutdown Regulator With Current Limiting (V_{OUT} = 2 to 7V)



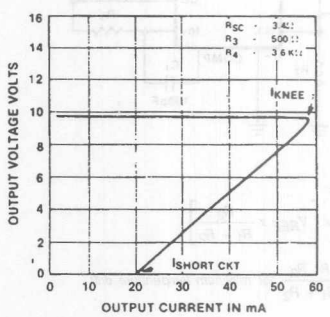
NOTES:

$$I_{KNEE} = \left[\frac{V_{OUT} R_3}{R_{SC} R_4} + \frac{V_{SENSE} (R_3 + R_4)}{R_{SC} R_4} \right]$$

$$V_{OUT} = \left[V_{REF} \times \frac{R_1 + R_2}{R_4} \right]$$

$$I_{SHORTCKT} = \left[\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4} \right]$$

High Voltage Regulator (V_{OUT} = 7 to 37V)



NOTES:

$$\frac{R_4}{R_3} = \frac{V_{OUT} I_{SC}}{V_{SENSE} (I_{KNEE} - I_{SHORTCKT})} - 1$$

$$R_{SC} = \frac{V_{SENSE}}{I_{SC}} \left[1 + \frac{R_3}{R_4} \right]$$

Foldback Current Limiting Regulator (V_{OUT} = 2 to 7V)

Current-mode PWM controller

UC3842

DESCRIPTION

The UC3842 is available in an 8-Pin mini-DIP the necessary features to implement off-line, fixed-frequency current-mode control schemes with a minimal external parts count. This technique results in improved line regulation, enhanced load response characteristics, and a simpler, easier to design control loop. Topological advantages include inherent pulse-by-pulse current limiting.

Protection circuitry includes built-in undervoltage lock-out and current limiting. Other features include fully-latched operation, a 1% trimmed bandgap reference, and start-up current less than 1mA.

These devices feature a totem-pole output designed to source and sink high peak current from a capacitive load, such as the gate of a power MOSFET. Consistent with N-channel power devices, the output is low in the OFF-state.

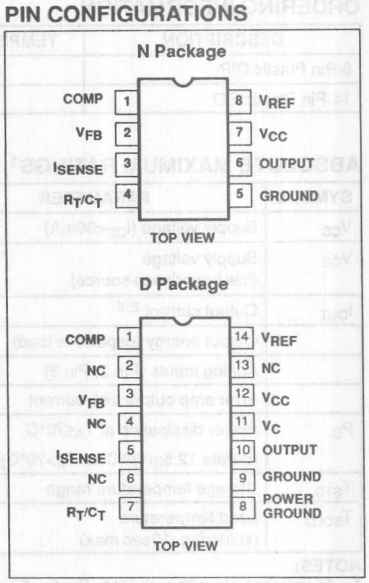
FEATURES

- Low start-up current (≤1mA)
- Automatic feed-forward compensation
- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Undervoltage lock-out with hysteresis
- Double pulse suppression
- High current totem-pole output
- Internally-trimmed bandgap reference
- 400kHz operation, guaranteed min

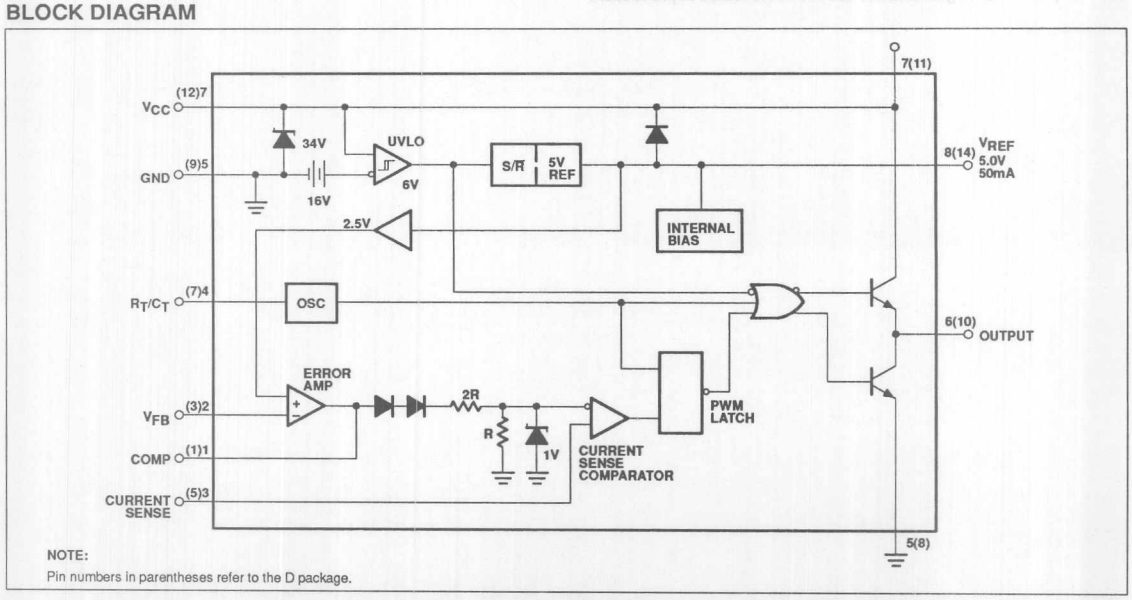
APPLICATIONS

- Off-line switched mode power supplies
- DC-to-DC converters UC3842

PIN CONFIGURATIONS



BLOCK DIAGRAM



NOTE:
Pin numbers in parentheses refer to the D package.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	UC3842N
14-Pin Plastic SO	0 to +70°C	UC3842D

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage (I_{CC}<30mA)		Self-Limiting
V_{CC}	Supply voltage (low impedance source)	30	V
I_{OUT}	Output current [2, 3]	±1	A
	Output energy (capacitive load)	5	µJ
	Analog inputs (Pin 2, Pin 3)	-0.3 to 6.3	V
	Error amp output sink current	10	mA
P_D	Power dissipation at T_A≤70°C (derate 12.5mW/°C for T_A>70°C)[2]	1	W
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 10sec max)	300	°C

NOTES:
1. All voltages are with respect to Pin 5; all currents are positive into the specified terminal.
2. See section in application note on "Power Dissipation Calculation".
3. This parameter is guaranteed, but not 100% tested in production.

DC AND AC ELECTRICAL CHARACTERISTICS

$0 \le T_J \le 70°C$ for UC3842; V_{CC}=154; R_T=10kW; C_T=3.3nF, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	UC3842			UNIT
			Min	Typ	Max	
Reference section						
V_{OUT}	Output voltage	T_J=25°C, I_O=1mA	4.90	5.00	5.10	V
	Line regulation	$12 \le V_{IN} \le 25V$		6	20	mV
	Load regulation	$1 \le I_O \le 20mA$		6	25	mV
	Temp. stability[1]			0.2	0.4	mV/°C
	Total output variation[1]	Line, load, temp.	4.82		5.18	V
V_{NOISE}	Output noise voltage[1]	$10Hz \le f \le 10kHz$, T_J=25°C		50		µV
	Long-term stability[1]	T_J=125°C, 1000 Hrs.		5	25	mV
	Output short-circuit	T_J=25	-30	-100	-130	mA
	Output short-circuit	$-55 < T_J \le 0°C$	-30	-100	-180	mA
Oscillator section						
	Initial accuracy	T_J=25°C	47	52	57	kHz
	Voltage stability	$12 \le V_{CC} \le 25V$		0.2	1	%
	Temp. stability[1]	$T_{MIN} \le T_J \le T_{MAX}$		5		%
	Amplitude	$V_{PIN\ 4}$ peak-to-peak		1.7		V
Error amp section						
	Input voltage	V Pin 1=2.5V	2.42	2.50	2.58	V
I_{BIAS}	Input bias current			-0.3	-2	µA
A_{VOL}		$2 \le V_O \le 4V$	65	90		dB
	Unity gain bandwidth[1]	T_J=25°C	0.7	1		MHz
	Unity gain bandwidth	$T_{MIN} < T_J < T_{MAX}$	0.5			MHz
PSRR	Power supply rejection ratio	$12 \le V_{CC} \le 25V$	60	70		dB
I_{SINK}	Output sink current	$V_{PIN\ 2}$=2.7V, $V_{PIN\ 1}$=1.1V	2	6		mA
I_{SOURCE}	Output source current	$V_{PIN\ 2}$=2.3V, $V_{PIN\ 1}$=5V	-0.5	-0.8		mA
	V_{OUT} High	$V_{PIN\ 2}$=2.3V, R_L=15k to ground	5	6		V
	V_{OUT} Low	$V_{PIN\ 2}$=2.7V, R_L=15k to Pin 8		0.7	1.1	V
Current sense section						
	Gain [2, 3]		2.85	3	3.15	V/V
	Maximum input signal[2]	$V_{PIN\ 1}$=5V	0.9	1	1.1	V
PSRR	Power supply rejection ratio[2]	$12 \le V_{CC} \le 25V$		70		dB
I_{BIAS}	Input bias current			-2	-10	µA
	Delay to output[1]			150	300	ns

DC AND AC ELECTRICAL CHARACTERISTICS

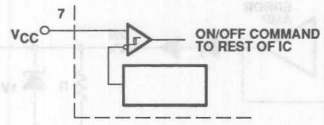
$0 \leq T_J \leq 70°C$ for UC3842; V_{CC}=15[4]; R_T=10kΩ; C_T=3.3nF, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	UC3842			UNIT
			Min	Typ	Max	
Output section						
I_{OL}	Output Low-Level	I_{SINK}=20mA		0.1	0.4	V
		I_{SINK}=200mA		1.5	2.2	V
I_{OH}	Output High-Level	I_{SOURCE}=20mA	13	13.5		V
		I_{SOURCE}=200mA	12	13.5		V
t_R	Rise time	C_L=1nF		50	150	ns
t_F	Fall time	C_L=1nF		50	150	ns
Undervoltage lockout section						
	Start threshold	X842	14.5	16	17.5	V
		X843	7.8	8.4	9.0	V
	Min. operating voltage after turn on	X842	8.5	10	11.5	V
		X843	7.0	7.6	8.2	V
PWM section						
	Maximum duty cycle	X842/43	93	97	100	%
	Minimum duty cycle				0	%
Total standby current						
	Start-up current			0.5	1	mA
I_{CC}	Operating supply current	$V_{PIN\ 2}$=$V_{PIN\ 3}$=0V		11	17	mA
	V_{CC} zener voltage	I_{CC}=25mA		34		V
Maximum operating frequency section						
	Maximum operating frequency for all functions operating cycle-by-cycle		400			kHz

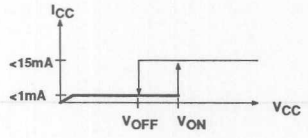
NOTES:

1. These parameters, although guaranteed, are not 100% tested in production.
2. Parameter measured at trip point of latch with $V_{PIN\ 2}$=0.
3. Gain defined as: $A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}$; $0 \leq V_{PIN\ 3} \leq 0.8V$

UNDERVOLTAGE LOCKOUT

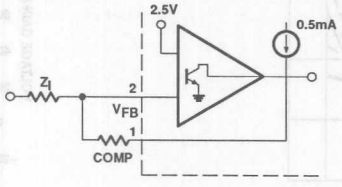


	UC3842
V_{ON}	16V
V_{OFF}	10V



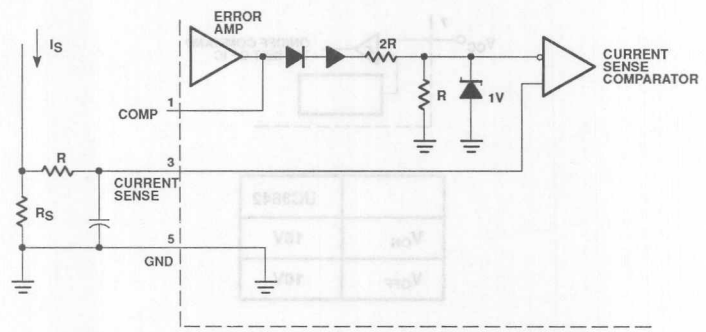
NOTE:
During Undervoltage Lock-Out, the output driver is biased to a high impedance state. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with output leakage current.

ERROR AMP CONFIGURATION



NOTE:
Error AMP can source or sink up to 0.5mA.

CURRENT SENSE CIRCUIT



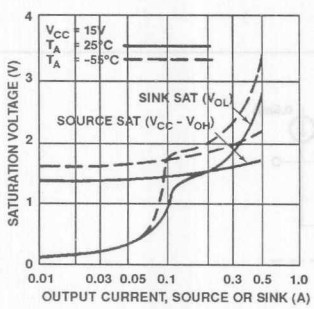
NOTE:
Peak current (I_S) is determined by the formula:

$$I_{S\ MAX} = \frac{1.0V}{R_S}$$

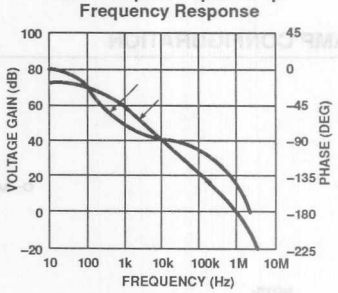
A small RC filter may be required to suppress switch transients.

TYPICAL PERFORMANCE CHARACTERISTICS

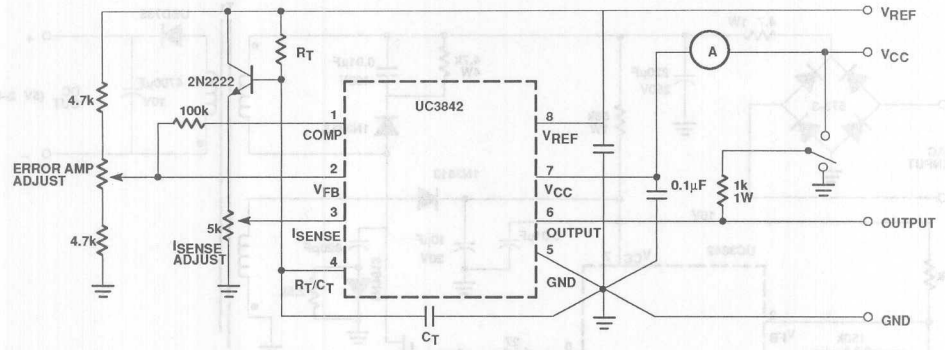
Output Saturation Characteristics



Error Amplifier Open-Loop Frequency Response

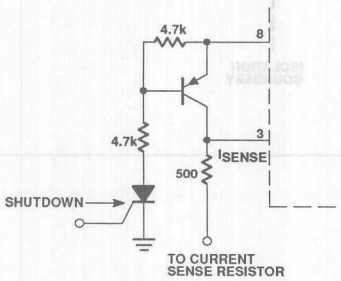


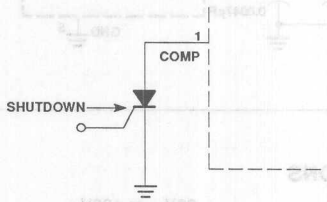
OPEN-LOOP LABORATORY TEST FIXTURE



NOTE:
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to Pin 3.

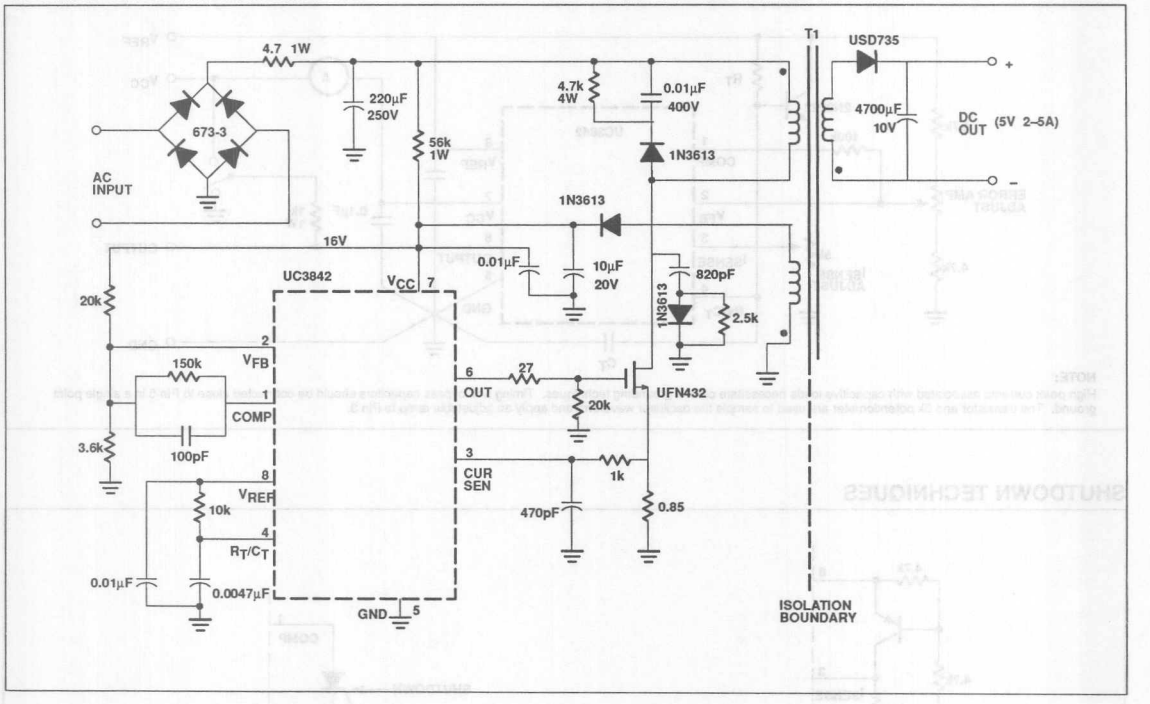
SHUTDOWN TECHNIQUES





NOTE:
Shutdown of the UC3842 can be accomplished by two methods; either raise Pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground. Either method causes the output of thw PWM comparator to be high (refer to Block Diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at Pins 1 and/or 3 is removed. In the examples shown, an externally-latched shutdown may be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower UVLO threshold (10V). At this point all internal bias is removed, allowing the SCR to reset.

OFF-LINE FLYBACK REGULATOR

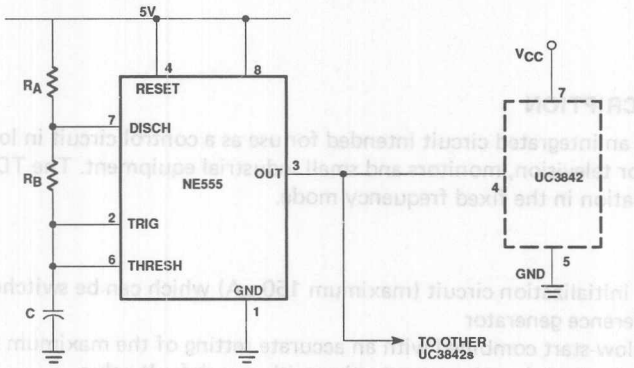


SPECIFICATIONS

Input line voltage:	$90V_{AC}$ to $130V_{AC}$
Input frequency:	50 or 60Hz
Switching frequency:	40kHz±10%
Output power:	25W maximum
Output voltage:	5V±5%
Output current:	2 to 5A
Line regulation:	0.01%/V
Load regulation:	8%/A*
Efficiency @ 25 W,	
$V_{IN}=90V_{AC}$:	70%
$V_{IN}=130V_{AC}$:	65%
Output short-circuit current:	2.5A average

NOTE:
This circuit uses a low-cost feedback scheme in which the DC voltage developed from the primary-side control winding is sensed by the UC3842 error amplifier. Load regulation is therefore dependent on the coupling between secondary and control windings, and on transformer leakage inductance. For applications requiring better load regulation, a UC1901 Isolated Feedback Generator can be used to directly sense the output voltage.

SYNCHRONIZATION AND MAXIMUM DUTY CYCLE CLAMP



NOTES:

$$f = \frac{1.44}{(R_A + 2R_B)\,C}$$

$$D_{MAX} = \frac{R_B}{R_A + 2R_B}$$

Control circuit for switched-mode power supplies TDA8380

GENERAL DESCRIPTION

The TDA8380 is an integrated circuit intended for use as a control circuit in low-cost switched mode power supplies for television, monitors and small industrial equipment. The TDA8380 operates using duty factor regulation in the fixed frequency mode.

Features

- A low-current initialization circuit (maximum 150 μA) which can be switched off
- A bandgap reference generator
- Circuitry for slow-start combined with an accurate setting of the maximum duty factor (D_{max})
- Programmable low supply voltage protection with one default value
- High supply protection circuitry
- Error amplifier with a transfer characteristic generator (TCG)
- Protection against open- and short-circuited feedback loop
- An overload voltage foldback
- Primary current protection circuitry for both cycle-by-cycle and trip mode
- Protection against transformer saturation
- A direct drive output stage (sink current 2.5 A, source current 0.75 A)
- Anti-double pulse logic
- Protected against damage as a result of a short-circuited high-voltage transistor
- RC oscillator with synchronization input

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{CC}	–	14	–	V
Supply current	I_{CC}	–	–	15	mA
Output pulse repetition frequency range	f_o	10	–	100	kHz
Operating ambient temperature range	T_{amb}	–25	–	+ 70	°C

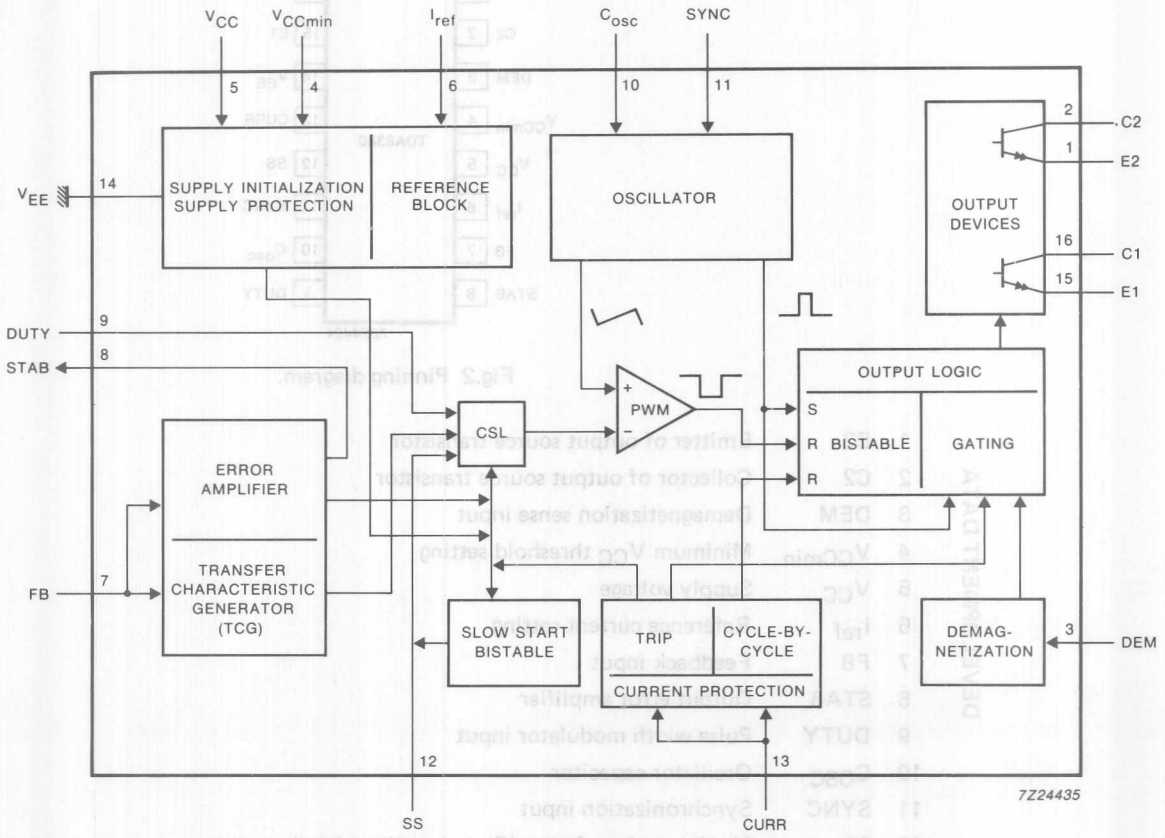


Fig.1 Block diagram.

PINNING

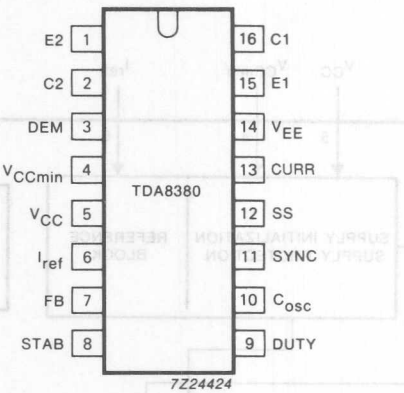


Fig.2 Pinning diagram.

DEVELOPMENT DATA

1	E2	Emitter of output source transistor
2	C2	Collector of output source transistor
3	DEM	Demagnetization sense input
4	V_{CCmin}	Minimum V_{CC} threshold setting
5	V_{CC}	Supply voltage
6	I_{ref}	Reference current setting
7	FB	Feedback input
8	STAB	Output error amplifier
9	DUTY	Pulse width modulator input
10	C_{OSC}	Oscillator capacitor
11	SYNC	Synchronization input
12	SS	Maximum duty factor (D_{max}) setting plus slow-start
13	CURR	Input current protection
14	V_{EE}	Ground
15	E1	Emitter of output sink transistor
16	C1	Collector of output sink transistor

FUNCTIONAL DESCRIPTION

The TDA8380 is a control circuit which generates the pulses required to drive the switching transistor in a switched mode power supply (SMPS).

Supply

This device is intended to be used on the primary side of the power supply and can be supplied via a take-over (auxiliary) winding on the transformer.

The device is initialized via a high value resistor connected between the rectified mains voltage and the device's supply pin (pin 5), which causes the capacitor connected to this pin to charge slowly. When the voltage exceeds the initialization level (typically 17 V) the device will start up and the duty cycle will be slowly increased by the slow-start circuit. After a short period the take-over winding will supply the device. The value of the resistor is normally defined by the time taken to charge the capacitor. A one second delay between switching on and operation of the power supply is acceptable in most cases.

The operating voltage range is from 9 to 20 V. The supply pin is protected by a 23 V Zener diode. The supply protection circuit is activated once the Zener diode is conducting. The slow-start procedure begins after initialization, until then the output is off. The current drawn by the device during the initialization period is less than 150 μA.

When the supply voltage falls below the minimum trip level, the device switches off and the start-up procedure is repeated. The minimum voltage supply threshold setting (V_{CCmin}) can be set externally with a resistor connected between the V_{CCmin} pin (pin 4) and ground (pin 14) (see Fig.3).

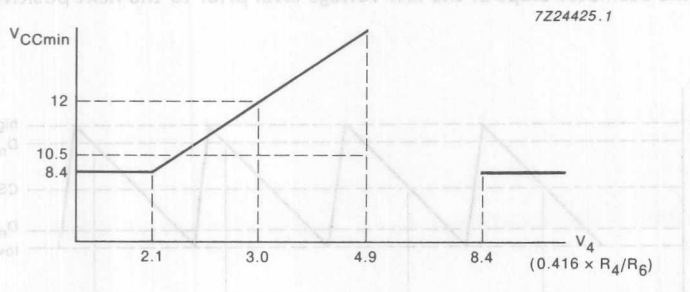


Fig.3 Trip level setting of minimum V_{CC} protection level.

V_{CCmin} can be set between 8.4 V (an internally fixed overriding protection level) and 17 V by means of an external resistor connected to pin 4.

When choosing the initialization and minimum supply voltages the following should be taken into account:

- The difference between the two voltages should be large enough to enable a supply voltage dip during start-up.
- The value of the minimum supply voltage should be high enough to ensure that the high-voltage transistor is correctly driven. A high protection level makes it possible to have a large resistor value in series with the base drive.

For battery line input operation, the V_{CCmin} pin is connected to V_{CC}, the start-up circuit is then inhibited and the device starts operating when V_{CC} exceeds the 8.4 V protection level (this level has a hysteresis of approximately 50 mV). The device draws current continuously under these conditions.

Reference block

A bandgap based reference generates a stabilized voltage of 7 V to supply most of the device's internal circuits, this decreases chip size and increases reliability. The only circuits connected to V_{CC} are:

- The initialization circuit
- The output circuitry
- The series transistor of the stabilized voltage

By means of a resistor (R_6) connected to the I_{ref} input a reference current is defined which determines six other device settings.

Part of the reference current is used to charge the oscillator capacitor (C_{10}), therefore, the charging time is proportional to $R_6 \times C_{10}$. The maximum duty factor (D_{max}) is set by the resistor connected to pin 12 (R_{12}) and is defined by the ratio R_6/R_{12}. The minimum supply voltage (pin 5) set by the resistor (R_4) at input V_{CCmin} is defined by: $4/6 \times V_6 \times R_4/R_6$.

Oscillator

The oscillator capacitor is charged and discharged between the high and low voltage levels as defined by the bandgap reference (high voltage typically 5 V and low voltage typically 1.4 V). The charge current is 1/6 of the reference current, the discharge current having the same value as the reference current. The period is therefore defined by $10 \times R_6 \times C_{10}$.

The oscillator flyback pulse is used to set the bistable in the output logic, however the output remains low until the positive ramp starts (see Fig.4). The oscillator can be synchronized by means of the SYNC pin. When this pin is connected to V_{CC}, the oscillator is free running. When it is between 0.85 and 5.6 V, the oscillator stops at the low voltage level prior to the next positive ramp.

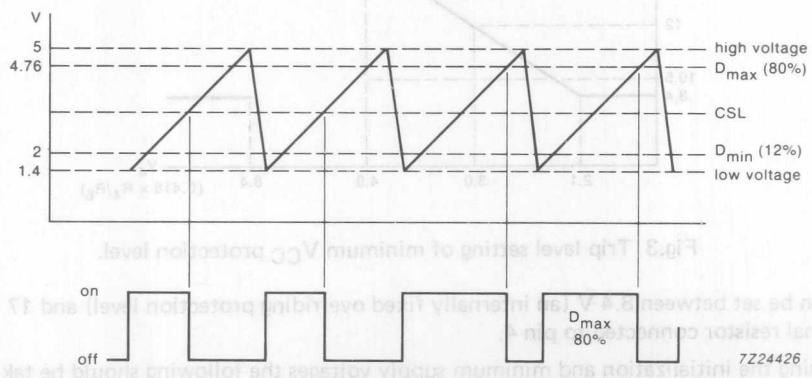


Fig.4 Oscillator levels.

FUNCTIONAL DESCRIPTION (continued)

Synchronization

The synchronization input (pin 11) can be driven by either an optocoupler or a loosely coupled pulse transformer.

Figure 5(a) illustrates synchronization using the 0.85 V threshold and a digital signal connected to the SYNC input (for example, an optocoupler between pin 11 and V_{CC}); the duty factor of the pulse is not very important. The oscillator starts at the first negative going edge of the sync. signal after the low voltage level has been reached. The synchronization frequency must be lower than the free running frequency. Synchronization must never affect the period time as this will corrupt the setting of the maximum duty factor.

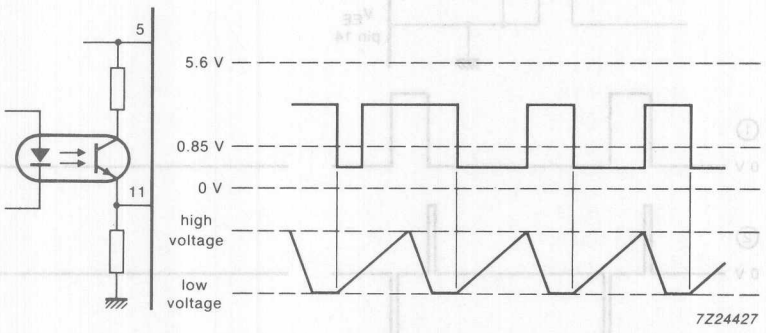


Fig. 5(a) DC coupled synchronization using the 0.85 V level.

In Fig.5(b) the disabling threshold (5.6 V) is used for synchronization. In this case the oscillator starts at the positive going edge of the sync. signal.

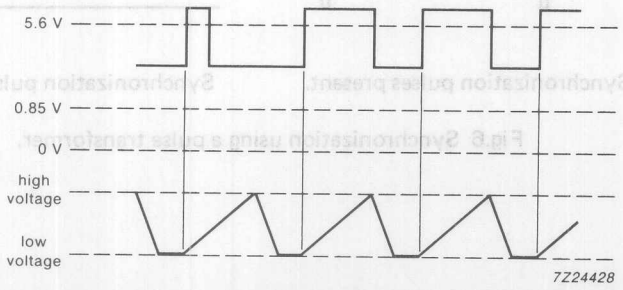
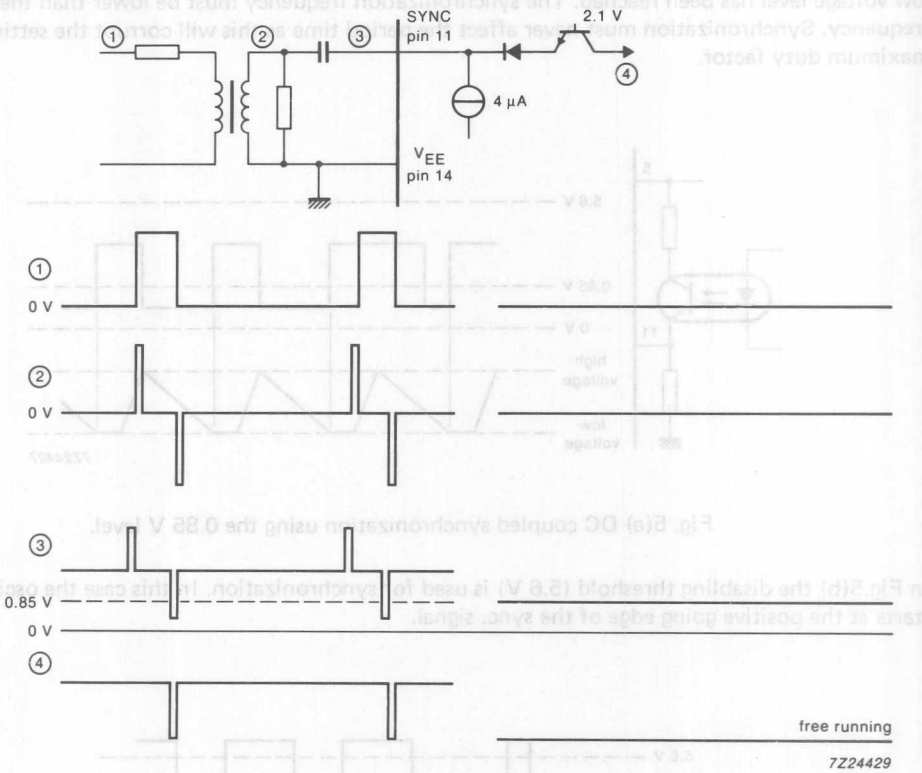


Fig.5(b) DC coupled synchronization using the 5.6 V level.

Figure 6 illustrates synchronization using a pulse transformer. Internal circuitry causes a DC shift which informs the device that synchronization pulses are present (spikes around 0 V at the output of the pulse transformer) or not present (DC 0 V at the output of the pulse transformer). When synchronization is not used the SYNC pin must be connected to V_{CC}, it must not be connected directly to ground or left open.



Synchronization pulses present. Synchronization pulses not present.

Fig.6 Synchronization using a pulse transformer.

FUNCTIONAL DESCRIPTION (continued)

Error amplifier

The error amplifier compares the feedback voltage of the SMPS with a reference voltage (nominally 2.5 V). The amplifier output at pin 8 enables gain setting. The amplifier is stable for a gain greater than 20 dB.

The output of the error amplifier is not internally connected to the Pulse Width Modulator (PWM). One input to the PWM is available at the DUTY input (pin 9) via the Control Slicing Level (CSL) circuit. Normally the STAB and DUTY pins are connected together, but direct driving of pin 9 via an optocoupler from the secondary side is also possible. A type of current mode control can be achieved by mixing the STAB signal with the primary current signal before applying it to the DUTY input.

The feedback (FB) input (pin 7) is used as the input to the Transfer Characteristic Generator (TCG) circuit which ensures well defined duty factors at low FB voltages; a voltage foldback is an inherent characteristic. In Fig.7, the duty factor is shown as a function of the voltages at the FB, DUTY and SS inputs. The input which gives the lowest duty factor overrides the others.

The left hand curve is passed through during a slow-start (via the slow-start input pin 12) when the duty cycle slowly increases linearly with respect to V_{12}. The right-hand curve is passed through at start-up. The FB voltage slowly increases from zero and the duty factor, starting at 12%, increases until the maximum duty factor (D_{max}) is reached. A few hundred millivolts later, the FB voltage reaches the start of the regulation curve which is at approximately 2.5 V. The plateau area between reaching D_{max} and starting the regulation curve is kept as small as possible (typically 200 mV).

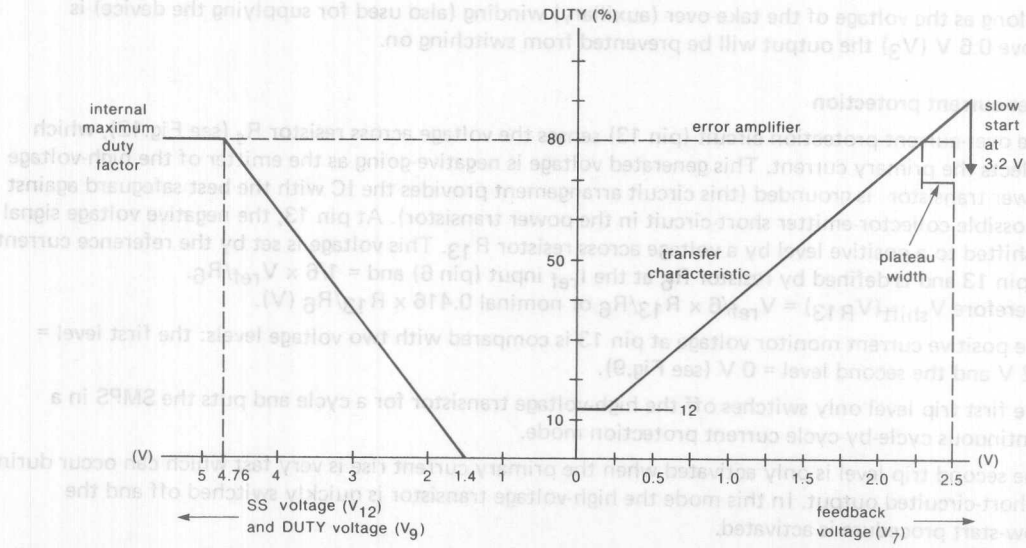


Fig.7 The duty factor as a function of the FB, SS and DUTY voltages.

Due to the characteristics of the TCG, and the fact that an open FB input results in a low voltage at the FB input, open- and short-circuit feedback loops will result in low duty factors. When DC feedback is used across the error amplifier, the current capability of the error amplifier must be considered when determining the feedback resistor value.

When the input to the PWM (pin 9) is driven by an optocoupler, the TCG can be used when a rough primary voltage is applied to the FB input. In this situation an open feedback loop will cause an increase in the FB voltage as the duty factor rises to its maximum. As soon as the FB voltage exceeds the reference by 0.7 V, the slow-start is triggered.

Demagnetization sense circuit

To enable the SMPS to be kept in the non-continuous mode, an input is available which delays switch-on of the high-voltage transistor until the transformer currents have decayed to zero. This is an effective way of avoiding transformer saturation. The waveforms illustrated by Fig.8 show demagnetization with respect to the application diagram of Fig.12.

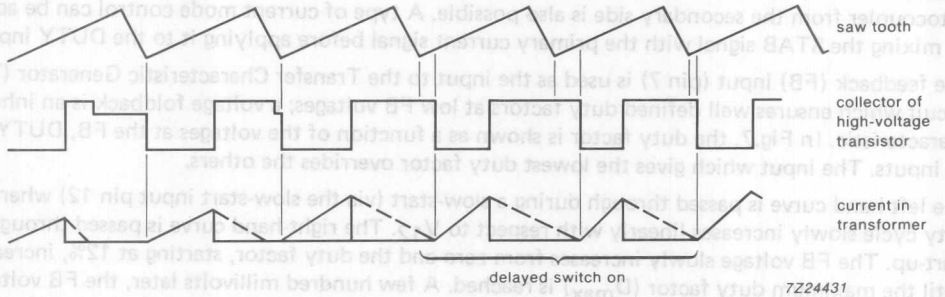


Fig.8 Demagnetization function.

As long as the voltage of the take-over (auxiliary) winding (also used for supplying the device) is above 0.6 V (V_3) the output will be prevented from switching on.

Over-current protection

The over-current protection circuit (pin 13) senses the voltage across resistor R_s (see Fig.12), which reflects the primary current. This generated voltage is negative-going as the emitter of the high-voltage power transistor is grounded (this circuit arrangement provides the IC with the best safeguard against a possible collector-emitter short-circuit in the power transistor). At pin 13, the negative voltage signal is shifted to a positive level by a voltage across resistor R_{13}. This voltage is set by the reference current at pin 13 and is defined by resistor R_6 at the I_{ref} input (pin 6) and = $1/6 \times V_{ref}/R_6$.
Therefore $V_{shift}(V_{R13}) = V_{ref}/6 \times R_{13}/R_6$ or nominal $0.416 \times R_{13}/R_6$ (V).

The positive current monitor voltage at pin 13 is compared with two voltage levels: the first level = 0.2 V and the second level = 0 V (see Fig.9).

The first trip level only switches off the high-voltage transistor for a cycle and puts the SMPS in a continuous cycle-by-cycle current protection mode.

The second trip level is only activated when the primary current rise is very fast which can occur during a short-circuited output. In this mode the high-voltage transistor is quickly switched off and the slow-start procedure is activated.

The difference between the first and second primary current peak levels is set by R_s:

$I_2 - I_1 = 0.2/R_s$.

The absolute peak values are set by R_6 and R_{13}:

$I_2 \times R_s = 0.416 \times R_{13}/R_6$ or

$I_1 \times R_s = (0.416 \times R_{13}/R_6) - 0.2$

FUNCTIONAL DESCRIPTION (continued)

Over-current protection (continued)

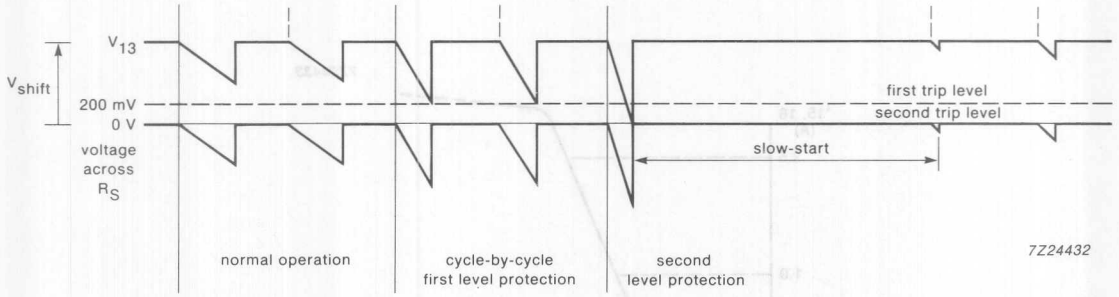


Fig.9 Current protection.

Slow-start circuit

A slow-start occurs:

- At Switch-on of the SMPS
- After a current trip as described in the section **Over-current protection**
- After a low or high V_{CC} trip.

The capacitor at the SS input is discharged and the slow-start bistable is reset when the voltage at the SS input falls below 0.5 V after which the circuit is ready for a slow-start. The dead time (during which the capacitor at the SS input is being charged to the 1.4 V lower level of the sawtooth) before duty cycle regulation starts is minimal. The SS input can also be used for D_{max} setting by connecting a resistor to ground. The voltage across this resistor is then limited to $1/6 \times V_{ref} \times R_{12}/R_6$.

Output stages

The output stage consists of two NPN darlington transistors, their collector and emitter connected to separate pins (see Fig.12). The top transistor is capable of sourcing a maximum of 0.75 A to the high-voltage transistor while the bottom transistor can sink peak currents up to 2.5 A.

For low currents up to 10 mA, the saturation voltage of the sink darlington transistor is similar to that of a single transistor (see Fig.10). During switching of this transistor dV/dt is internally limited to reduce interference.

Care should be taken with the external wiring of the output pins to avoid oscillation or interference due to parasitic inductance and wire resistance.

During start-up a small current flows from V_{CC} to E2 to precharge the series capacitor at the output (see Fig.12).

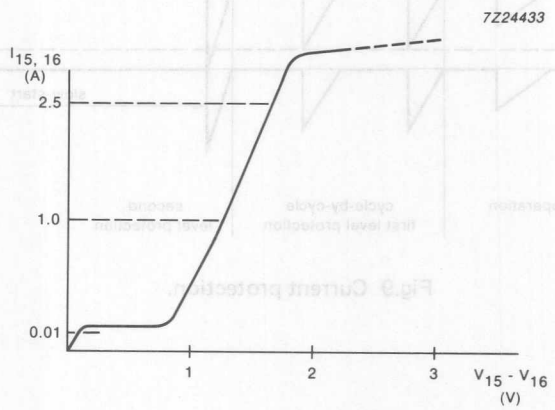


Fig.10 Saturation curve.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Voltage					
pin 5 (V_{CC})		−0.5	–	20	V
pins 1, 2, 4 and 16		−0.5	–	V_{CC}	V
pins 3 and 13		−0.5	–	0.5	V
pins 7 and 9		−0.5	–	6.5	V
pin 11		0.6	–	V_{CC}	V
Currents					
pin 5 (V_{CC})		0	–	20	mA
pin 1		−0.75	–	0	A
pin 2		0	–	0.75	A
pins 3, 4, 6 to 8 and 10 to 12		−10	–	10	mA
pin 13		−200	–	10	mA
pin 15		−2.5	–	0	A
pin 16		0	–	2.5	A
Total power dissipation	P_{tot}	see Fig.11			
Operating ambient temperature range (for dissipation $\leqslant$ 1 W)	T_{amb}	−25	–	+ 70	°C
Storage temperature range	T_{stg}	−55	–	+ 150	°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}a(max)}$ = 55 K/W

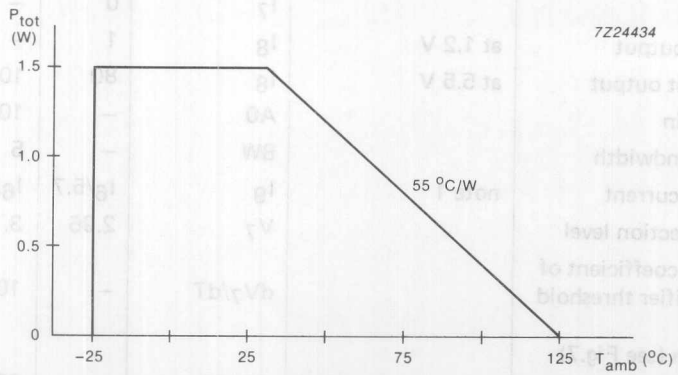


Fig.11 Power derating curve.

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C; reference resistor = 5 kΩ unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{CC}	9	–	20	V
Supply initialization level		V_5	15	17	18	V
High voltage protection		V_5	21	23	25	V
Internal fixed minimum protection level		V_5	7.9	8.4	8.9	V
Hysteresis		dV_{CC}	–	50	–	mV
Supply current operational		I_{CC}	–	–	15	mA
before initialization		I_{CC}	–	100	150	μA
Reference current (pin 4)	note 1	I_4	I_6/5.7	I_6/6	I_6/6.4	mA
Trigger level V_{CCmin} setting		V_5	$3.6V_4$	$3.8V_4$	$4.2V_4$	V
Clamp voltage	at 20 mA		21.5	23.5	25.5	V
Reference (pin 6)						
Reference voltage		V_{ref}	2.4	2.5	2.6	V
Current range		I_{ref}	200	–	800	μA
Reference voltage over I_6 range		dV_{ref}	–20	–	+ 20	mV
Error amplifier						
Error amplifier threshold	V_{CC} = 8.5 to 20 V	V_7	2.4	2.5	2.6	V
Input current		I_7	0	–	5	μA
Sink current output	at 1.2 V	I_8	1	–	–	mA
Source current output	at 5.5 V	I_8	80	100	130	μA
Open loop gain		A0	–	100	–	dB
Unity gain bandwidth		BW	–	5	–	MHz
Input DUTY current	note 1	I_9	I_6/5.7	I_6/6	I_6/6.3	mA
High FB protection level		V_7	2.95	3.1	3.25	V
Temperature coefficient of error amplifier threshold		dV_7/dT	–	100	–	10^{-6}/K
TCG function (see Fig.7)						
Transfer characteristic		dD/dV_7	–	32	–	%/V
Minimum duty factor		D_{min}	–	12	–	%
Plateau width		V_7	–	200	–	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Slow-start function						
Transfer characteristic		dD/dV_{12}	–	23.8	–	%/V
Input current	note 1	I_{12}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
Sink current during faults	at 0.5 V	I_{12}	8	–	–	mA
Internally fixed maximum duty factor		D_{max}	75	80	85	%
Clamp current	at V_{12} = 0.5 V	I_{12}	–	–2	–	mA
Output stage						
Source transistor						
Voltage drop with respect to V_{CC}	at 0.75 A	$V_{CC}-V_1$	–	2	–	V
Pull-up current	$V_{CC} - V_1$ = 15 V	$-I_1$	25	–	100	μA
Operating current range		$-I_1$	0	–	0.75	A
Sink transistor (see Fig.10)						
Saturation voltage						
at 2.5 A		$V_{16} - V_{15}$	–	2	–	V
at 1 A		$V_{16} - V_{15}$	–	1.5	–	V
at 10 mA		$V_{16} - V_{15}$	–	0.3	–	V
Leakage current	$V_{16} - V_{15}$ = 20 V	I_{16}	–	–	1	μA
Falling edge		$dV_{16\text{-}15}/dt$	–	0.2	–	V/ns
Operating current range						
Peak		I_{16}	0	–	2.5	A
Average		I_{16}	–	–	250	mA
Oscillator						
High level voltage		V_{10}	–	5	–	V
Low level voltage		V_{10}	–	1.4	–	V
Charge current	note 1	I_{10}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
Frequency range		f_o	10	–	100	kHz
Frequency	R_6 = 5 kΩ C_{10} = 680 pF	f_o	27	28.5	30	kHz
Temperature coefficient of the frequency		df/dT	–	100	–	10^{-6}/K

parameter	conditions	symbol	min.	typ.	max.	unit
Synchronization						
Minimum synchronization pulse width		t_{11}	–	–	0.5	μs
Switching threshold		V_{11}	0.7	0.85	0.9	V
Input current		I_{11}	2.5	5.0	7.5	μA
Disabling threshold		V_{11}	4.2	5.6	6.0	V
Input voltage	at −700 μA	V_{11}	390	–	550	mV
Demagnetization input						
Pin voltage	at 0 A	V_3	–	690	–	mV
Input current	at 0 V	I_3	−30	−40	−55	μA
Current range of clamp circuits		I_3	−10	–	+ 10	mA
Clamp level positive	at 10 mA	V_3	–	950	–	mV
Clamp level negative	at −10 mA	V_3	–	−800	–	mV
Current protection						
Input current	note 1	I_{13}	$I_6/5.7$	$I_6/6$	$I_6/6.3$	mA
First threshold		V_{13}	190	200	210	mV
Second threshold		V_{13}	−10	0	10	mV
Delay to switch output via level 1	pulse at pin 13 from 300 mV to 100 mV; I_O = 500 mA	–	–	350	–	ns
Delay to switch output via level 2	pulse at pin 13 from 300 mV to −200 mV; I_O = 500 mA	–	–	300	500	ns
First threshold including R_{13} (12 kΩ)	R_6 = 5 kΩ	–	–	−800	–	mV
Threshold for open pin detection		V_{13}	–	3.5	–	V

Note to the characteristics

1. Over the current range of I_6; 200 to 800 μA.

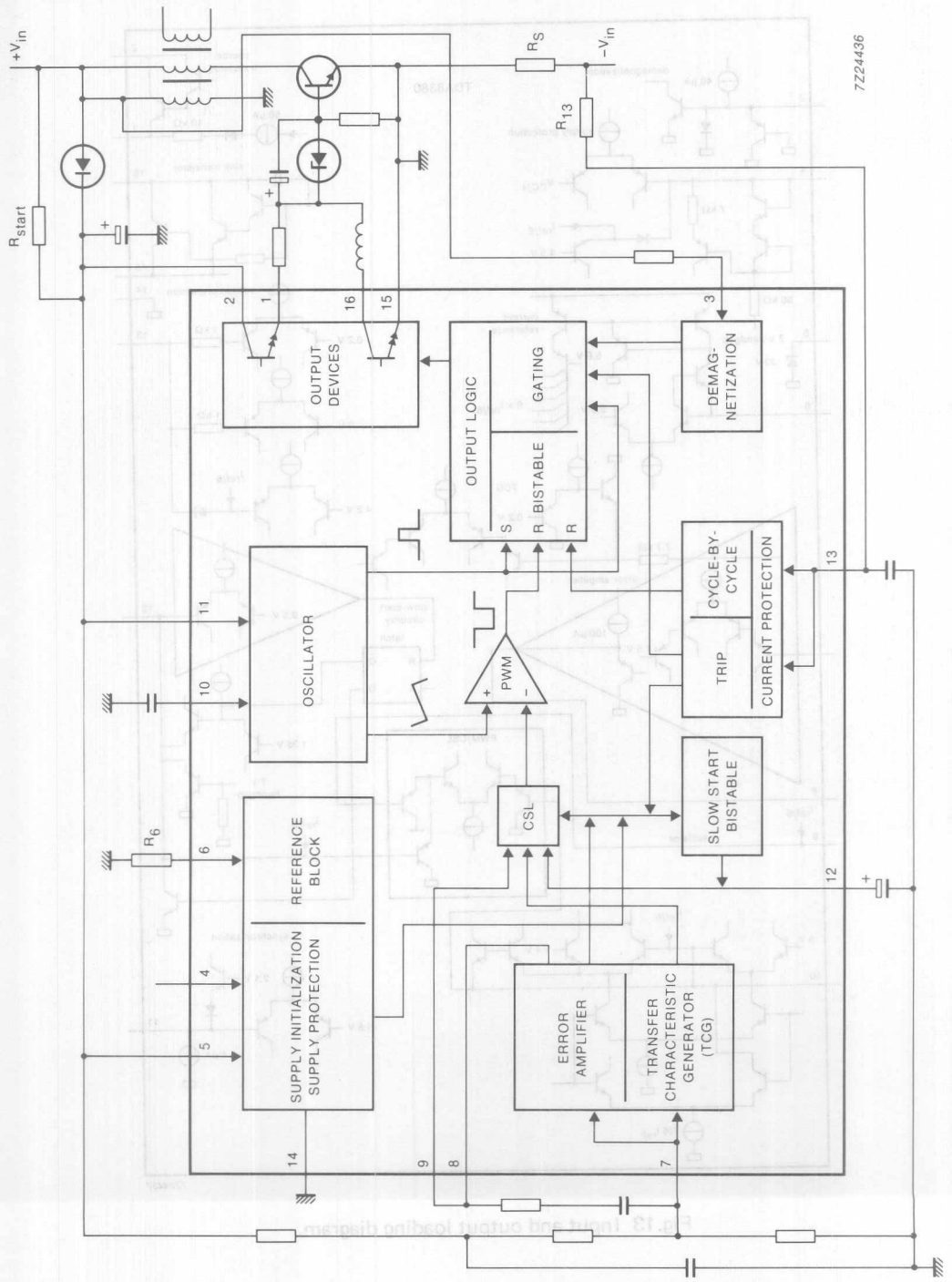


Fig.12 Simplified application diagram.

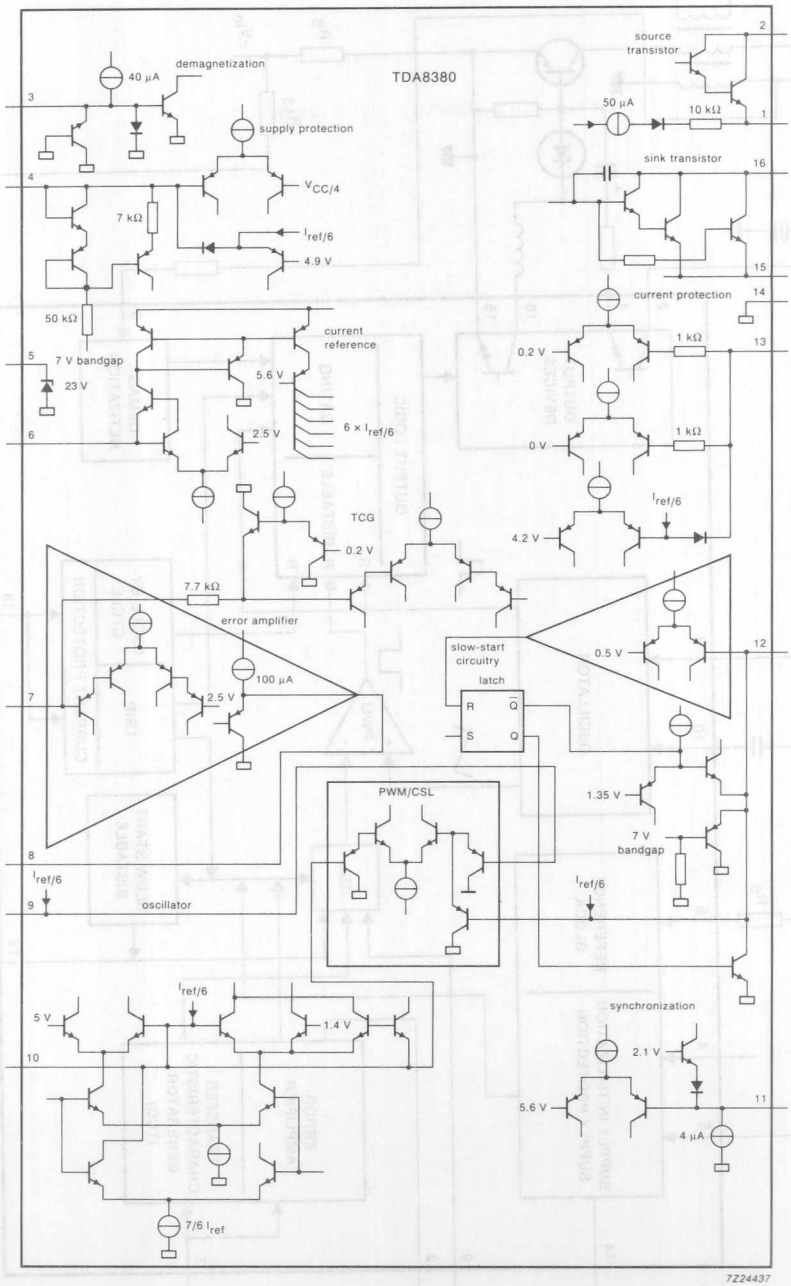


Fig.13 Input and output loading diagram.

Control circuit for switched-mode power supply TEA1039

GENERAL DESCRIPTION

The TEA1039 is a bipolar integrated circuit intended for the control of a switched-mode power supply. Together with an external error amplifier and a voltage regulator (e.g. a regulator diode) it forms a complete control system. The circuit is capable of directly driving the SMPS power transistor in small SMPS systems.

It has the following features:

- Suited for frequency and duty factor regulation.
- Suited for flyback converters and forward converters.
- Wide frequency range.
- Adjustable input sensitivity.
- Adjustable minimum frequency or maximum duty factor limit.
- Adjustable overcurrent protection limit.
- Supply voltage out-of-range protection.
- Slow-start facility.

QUICK REFERENCE DATA

Supply voltage	V_{CC}	nom.	14	V
Supply current	I_{CC}	max.	13	mA
Output pulse repetition frequency range	f_o	1 Hz to	100	kHz
Output current LOW	I_{OL}	max.	1	A
Operating ambient temperature range	T_{amb}	−25 to +	125	°C

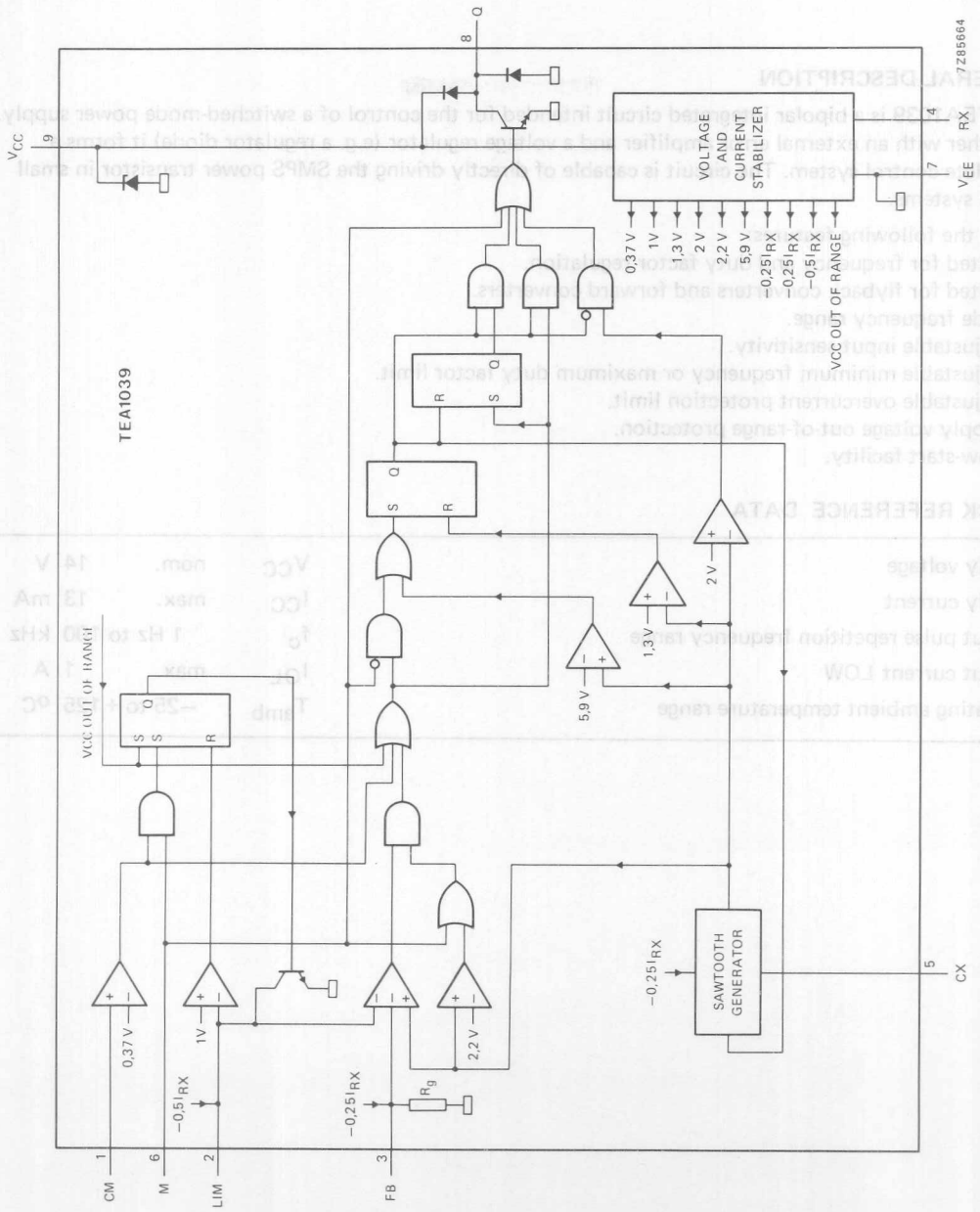


Fig. 1 Block diagram.

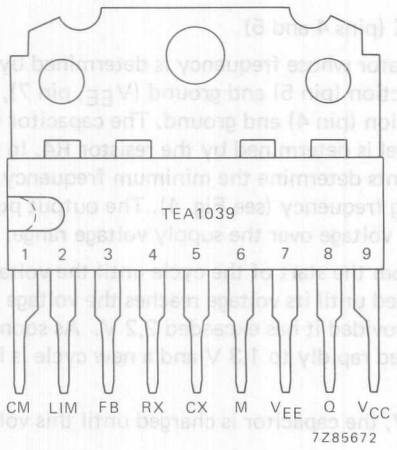


Fig. 2 Pinning diagram.

PINNING

1	CM	overcurrent protection input
2	LIM	limit setting input
3	FB	feedback input
4	RX	external resistor connection
5	CX	external capacitor connection
6	M	mode input
7	V_{EE}	common
8	Q	output
9	V_{CC}	positive supply connection

FUNCTIONAL DESCRIPTION

The TEA1039 produces pulses to drive the transistor in a switched-mode power supply. These pulses may be varied either in frequency (frequency regulation mode) or in width (duty factor regulation mode).

The usual arrangement is such that the transistor in the SMPS is ON when the output of the TEA1039 is HIGH, i.e. when the open-collector output transistor is OFF. The duty factor of the SMPS is the time that the output of the TEA1039 is HIGH divided by the pulse repetition time.

Supply V_{CC} (pin 9)

The circuit is usually supplied from the SMPS that it regulates. It may be supplied either from its primary d.c. voltage or from its output voltage. In the latter case an auxiliary starting supply is necessary.

The circuit has an internal V_{CC} out-of-range protection. In the frequency regulation mode the oscillator is stopped; in the duty factor regulation mode the duty factor is made zero. When the supply voltage returns within its range, the circuit is started with the slow-start procedure.

When the circuit is supplied from the SMPS itself, the out-of-range protection also provides an effective protection against any interruption in the feedback loop.

Mode input M (pin 6)

The circuit works in the frequency regulation mode when the mode input M is connected to ground (V_{EE}, pin 7). In this mode the circuit produces output pulses of a constant width but with a variable pulse repetition time.

The circuit works in the duty factor regulation mode when the mode input M is left open. In this mode the circuit produces output pulses with a variable width but with a constant pulse repetition time.

FUNCTIONAL DESCRIPTION (continued)

Oscillator resistor and capacitor connections RX and CX (pins 4 and 5)

The output pulse repetition frequency is set by an oscillator whose frequency is determined by an external capacitor C5 connected between the CX connection (pin 5) and ground (V_{EE}, pin 7), and an external resistor R_4 connected between the RX connection (pin 4) and ground. The capacitor C5 is charged by an internal current source, whose current level is determined by the resistor R4. In the frequency regulation mode these two external components determine the minimum frequency; in the duty factor regulation mode they determine the working frequency (see Fig. 4). The output pulse repetition frequency varies less than 1% with the supply voltage over the supply voltage range.

In the frequency regulation mode the output is LOW from the start of the cycle until the voltage on the capacitor reaches 2 V. The capacitor is further charged until its voltage reaches the voltage on either the feedback input FB or the limit setting input LIM, provided it has exceeded 2,2 V. As soon as the capacitor voltage reaches 5,9 V the capacitor is discharged rapidly to 1,3 V and a new cycle is initiated (see Figs 5 and 6).

For voltages on the FB and LIM inputs lower than 2,2 V, the capacitor is charged until this voltage is reached; this sets an internal maximum frequency limit.

In the duty factor regulation mode the capacitor is charged from 1,3 V to 5,9 V and discharged again at a constant rate. The output is HIGH until the voltage on the capacitor exceeds the voltage on the feedback input FB; it becomes HIGH again after discharge of the capacitor (see Figs 7 and 8). An internal maximum limit is set to the duty factor of the SMPS by the discharging time of the capacitor.

Feedback input FB (pin 3)

The feedback input compares the input current with an internal current source whose current level is set by the external resistor R4. In the frequency regulation mode, the higher the voltage on the FB input, the longer the external capacitor C5 is charged, and the lower the frequency will be. In the duty factor regulation mode external capacitor C5 is charged and discharged at a constant rate, the voltage on the FB input now determines the moment that the output will become LOW. The higher the voltage on the FB input, the longer the output remains HIGH, and the higher the duty factor of the SMPS.

Limit setting input LIM (pin 2)

In the frequency regulation mode this input sets the minimum frequency, in the duty factor regulation mode it sets the maximum duty factor of the SMPS. The limit is set by an external resistor R2 connected from the LIM input to ground (pin 7) and by an internal current source, whose current level is determined by external resistor R4.

A slow-start procedure is obtained by connecting a capacitor between the LIM input and ground. In the frequency regulation mode the frequency slowly decreases from f_{max} to the working frequency. In the duty factor regulation mode the duty factor slowly increases from zero to the working duty factor.

Overcurrent protection input CM (pin 1)

A voltage on the CM input exceeding 0,37 V causes an immediate termination of the output pulse. In the duty factor regulation mode the circuit starts again with the slow-start procedure.

Output Q (pin 8)

The output is an open-collector n-p-n transistor, only capable of sinking current. It requires an external resistor to drive an n-p-n transistor in the SMPS (see Figs 9 and 10).

The output is protected by two diodes, one to ground and one to the supply.

At high output currents the dissipation in the output transistor may necessitate a heatsink. See the power derating curve (Fig. 3).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range, voltage source	V_{CC}	−0,3 to	+20	V
Supply current range, current source	I_{CC}	−30 to	+30	mA
Input voltage range, all inputs	V_I	−0,3 to	+6	V
Input current range, all inputs	I_I	−5 to	+5	mA
Output voltage range	V_{8-7}	−0,3 to	+20	V
Output current range				
output transistor ON	I_8	0 to	1	A
output transistor OFF	I_8	−100 to	+ 50	mA
Storage temperature range	T_{stg}	−55 to	+150	°C
Operating ambient temperature range (see Fig. 3)	T_{amb}	−25 to	+125	°C
Power dissipation (see Fig. 3)	P_{tot}	max.	2	W

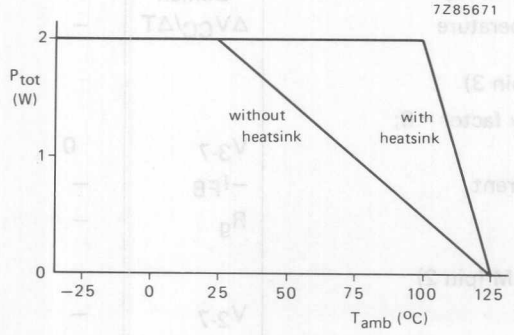


Fig. 3 Power derating curve.

CHARACTERISTICS

V_{CC} = 14 V; T_{amb} = 25 °C unless otherwise specified

	symbol	min.	typ.	max.	unit
Supply V_{CC} (pin 9)					
Supply voltage, operating	V_{CC}	11	14	20	V
Supply current					
at V_{CC} = 11 V	I_{CC}	–	7,5	11	mA
at V_{CC} = 20 V	I_{CC}	–	9	12	mA
variation with temperature	$\frac{\Delta I_{CC}/I_{CC}}{\Delta T}$	–	−0,3	–	%/K
Supply voltage, internally limited					
at I_{CC} = 30 mA	V_{CC}	23,5	–	28,5	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	18	–	mV/K
Low supply threshold voltage	V_{CCmin}	9	10	11	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	−5	–	mV/K
High supply threshold voltage	V_{CCmax}	21	23	24,6	V
variation with temperature	$\Delta V_{CC}/\Delta T$	–	10	–	mV/K
Feedback input FB (pin 3)					
Input voltage for duty factor = 0; M input open	V_{3-7}	0	–	0,3	V
Internal reference current	$-I_{FB}$	–	0,5 I_{RX}	–	mA
Internal resistor R_g	R_g	–	130	–	kΩ
Limit setting input LIM (pin 2)					
Threshold voltage	V_{2-7}	–	1	–	V
Internal reference current	$-I_{LIM}$	–	0,25 I_{RX}	–	mA
Overcurrent protection input CM (pin 1)					
Threshold voltage	V_{1-7}	300	370	420	mV
variation with temperature	$\Delta V_{1-7}/\Delta T$	–	0,2	–	mV/K
Propagation delay, CM input to output	t_{PHL}	–	500	–	ns

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.	unit
Oscillator connections RX and CX (pins 4 and 5)					
Voltage at RX connection at $-I_4$ = 0,15 to 1 mA	V_{4-7}	6,2	7,2	8,1	V
variation with temperature	$\Delta V_{4-7}/\Delta T$	–	2,1	–	mV/K
Lower sawtooth level	V_{LS}	–	1,3	–	V
Threshold voltage for output H to L transition in F mode	V_{FT}	–	2	–	V
Threshold voltage for maximum frequency in F mode	V_{FM}	–	2,2	–	V
Higher sawtooth level	V_{HS}	–	5,9	–	V
Internal capacitor charging current, CX connection	$-I_{CX}$	–	0,25 I_{RX}	–	mA
Oscillator frequency (output pulse repetition frequency)	f_o	1	–	10^5	Hz
Minimum frequency in F mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Maximum frequency in F mode, initial deviation	$\Delta f/f$	−20	–	+20	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	−0,16	–	%/K
Output LOW time in F mode, initial deviation	$\Delta t/t$	−25	–	+25	%
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Pulse repetition frequency in D mode, initial deviation	$\Delta f/f$	−10	–	10	%
variation with temperature	$\frac{\Delta f/f}{\Delta T}$	–	0,034	–	%/K
Minimum output LOW time in D mode at C_5 = 3,6 nF	t_{OLmin}	–	1	–	μs
variation with temperature	$\frac{\Delta t/t}{\Delta T}$	–	0,2	–	%/K
Output Q (pin 8)					
Output voltage LOW at I_8 = 100 mA	V_{8-7}	–	0,8	1,2	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	1,5	–	mV/K
Output voltage LOW at I_8 = 1 A	V_{8-7}	–	1,7	2,1	V
variation with temperature	$\Delta V_{8-7}/\Delta T$	–	−1,4	–	mV/K

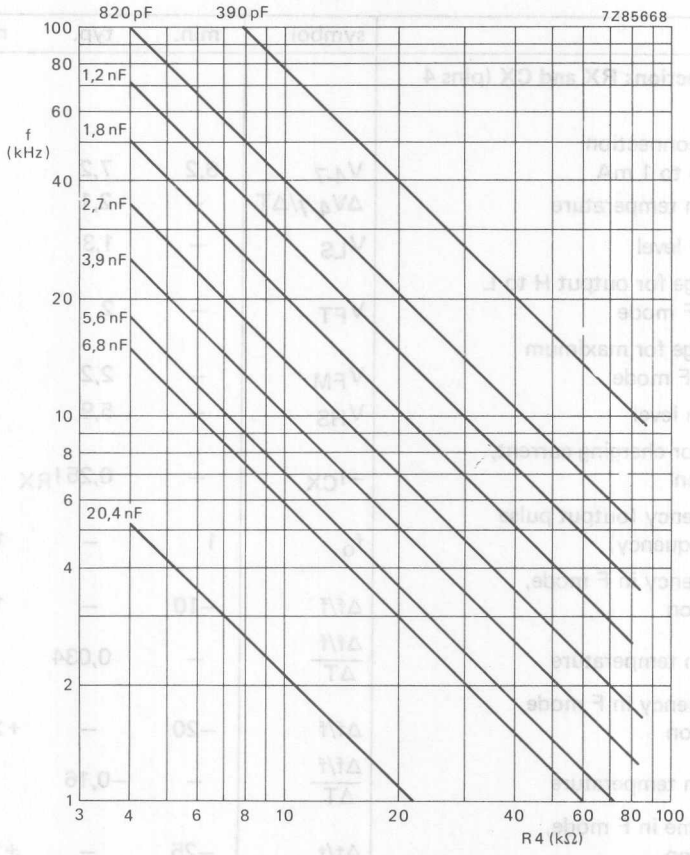


Fig. 4 Minimum pulse repetition frequency in the frequency regulation mode, and working pulse repetition frequency in the duty factor regulation mode, as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

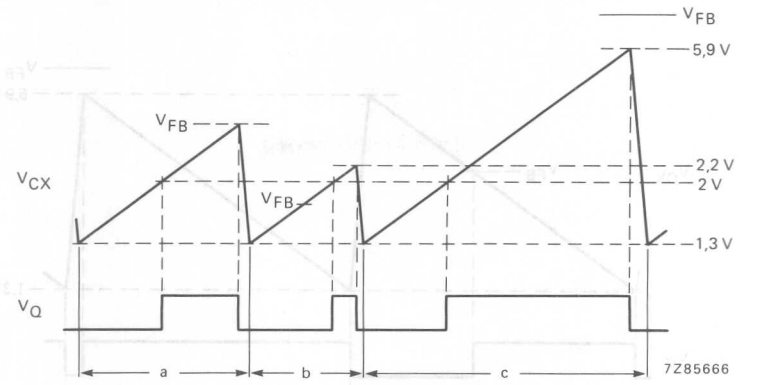


Fig. 5 Timing diagram for the frequency regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for three combinations of input signals. *a:* The voltages on inputs FB or LIM are between 2,2 V and 5,9 V. The circuit is in its normal regulation mode. *b:* The voltage on input FB or input LIM is lower than 2,2 V. The circuit works at its maximum frequency. *c:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit works at its minimum frequency.

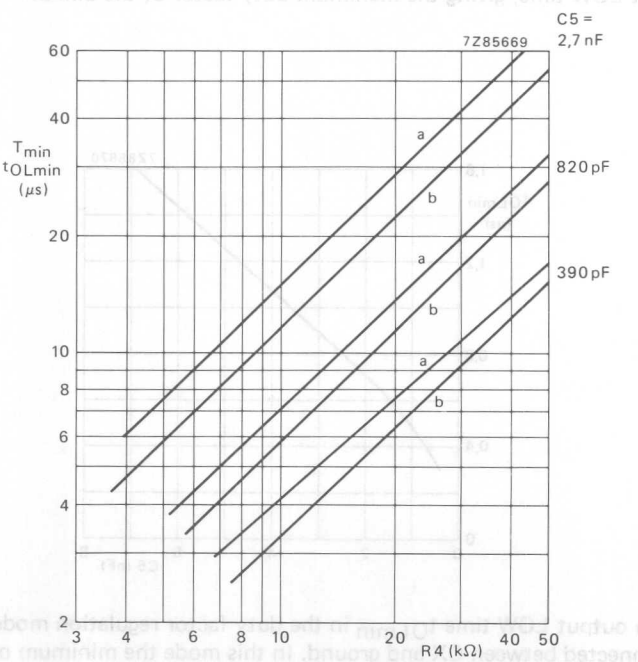


Fig. 6 Minimum output pulse repetition time T_{min} (curves a) and minimum output LOW time t_{OLmin} (curves b) in the frequency regulation mode as a function of external resistor R4 connected between RX and ground with external capacitor C5 connected between CX and ground as a parameter.

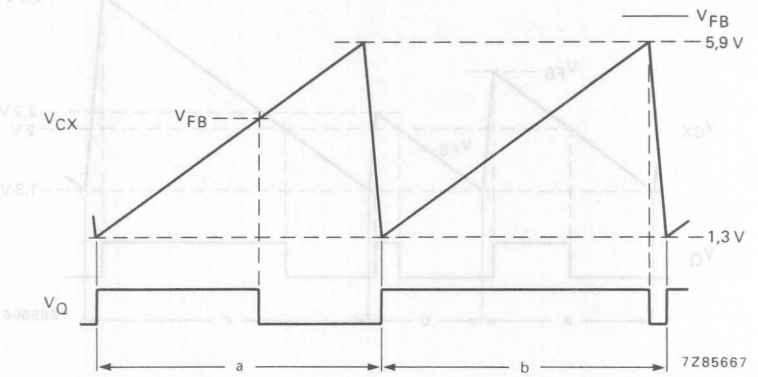


Fig. 7 Timing diagram for the duty factor regulation mode showing the voltage on external capacitor C5 connected between CX and ground and the output voltage as a function of time for two combinations of input signals. *a:* The voltages on inputs FB or LIM are below 5,9 V. The circuit is in its normal regulation range. *b:* The voltages on inputs FB and LIM are higher than 5,9 V. The circuit produces its minimum output LOW time, giving the maximum duty factor of the SMPS.

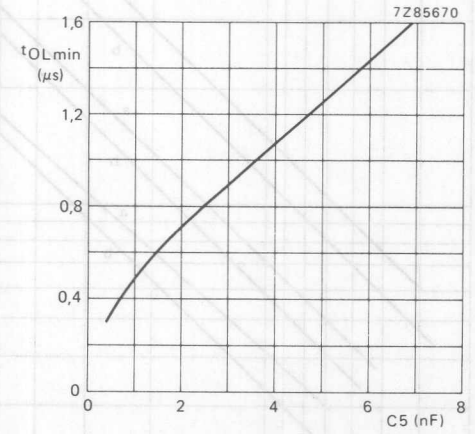


Fig. 8 Minimum output LOW time t_{OLmin} in the duty factor regulation mode as a function of external capacitor C5 connected between CX and ground. In this mode the minimum output LOW time is independent of R4 for values of R4 between 4 kΩ and 80 kΩ.

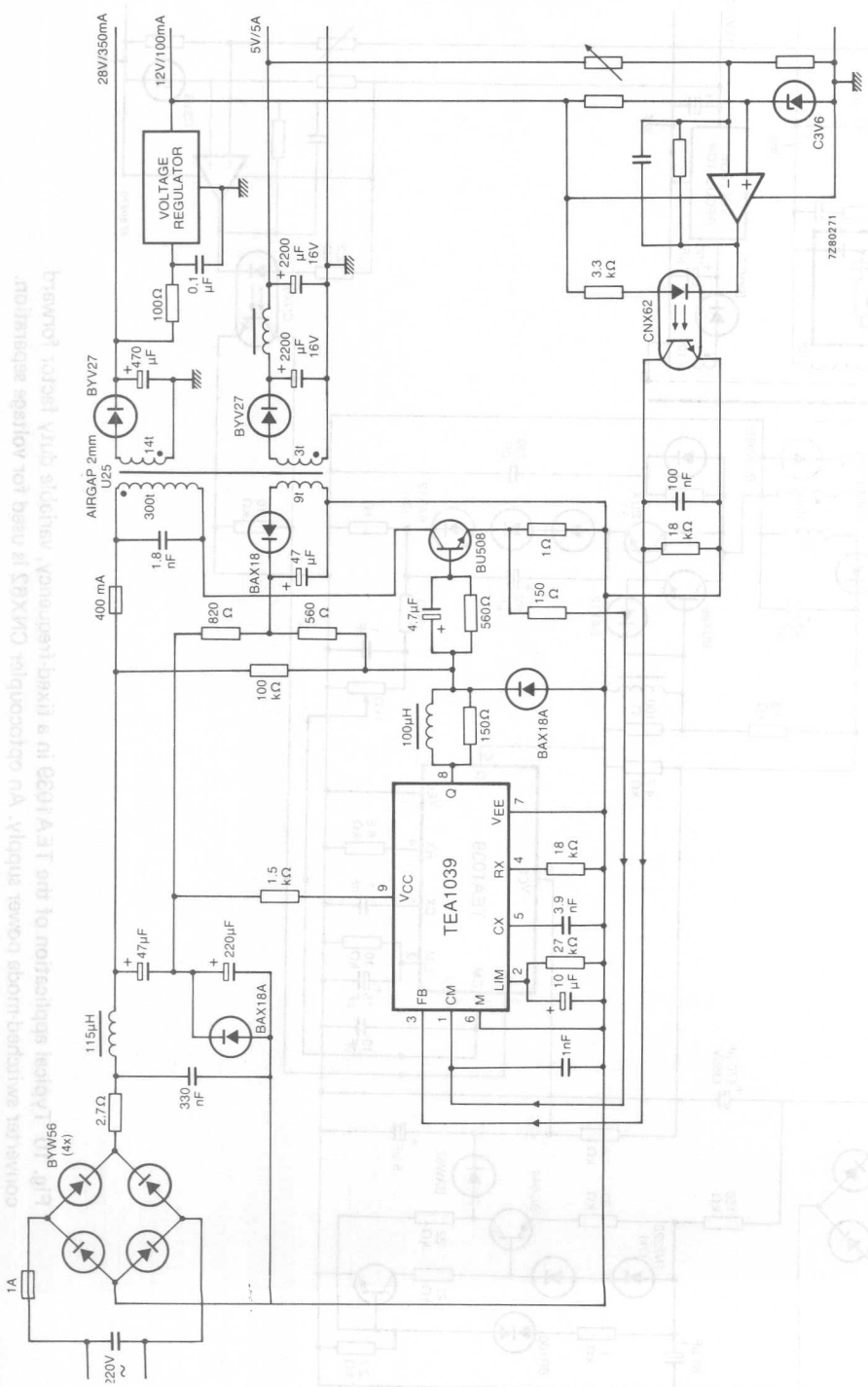


Fig. 9 Typical application of the TEA1039 in a variable-frequency flyback converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

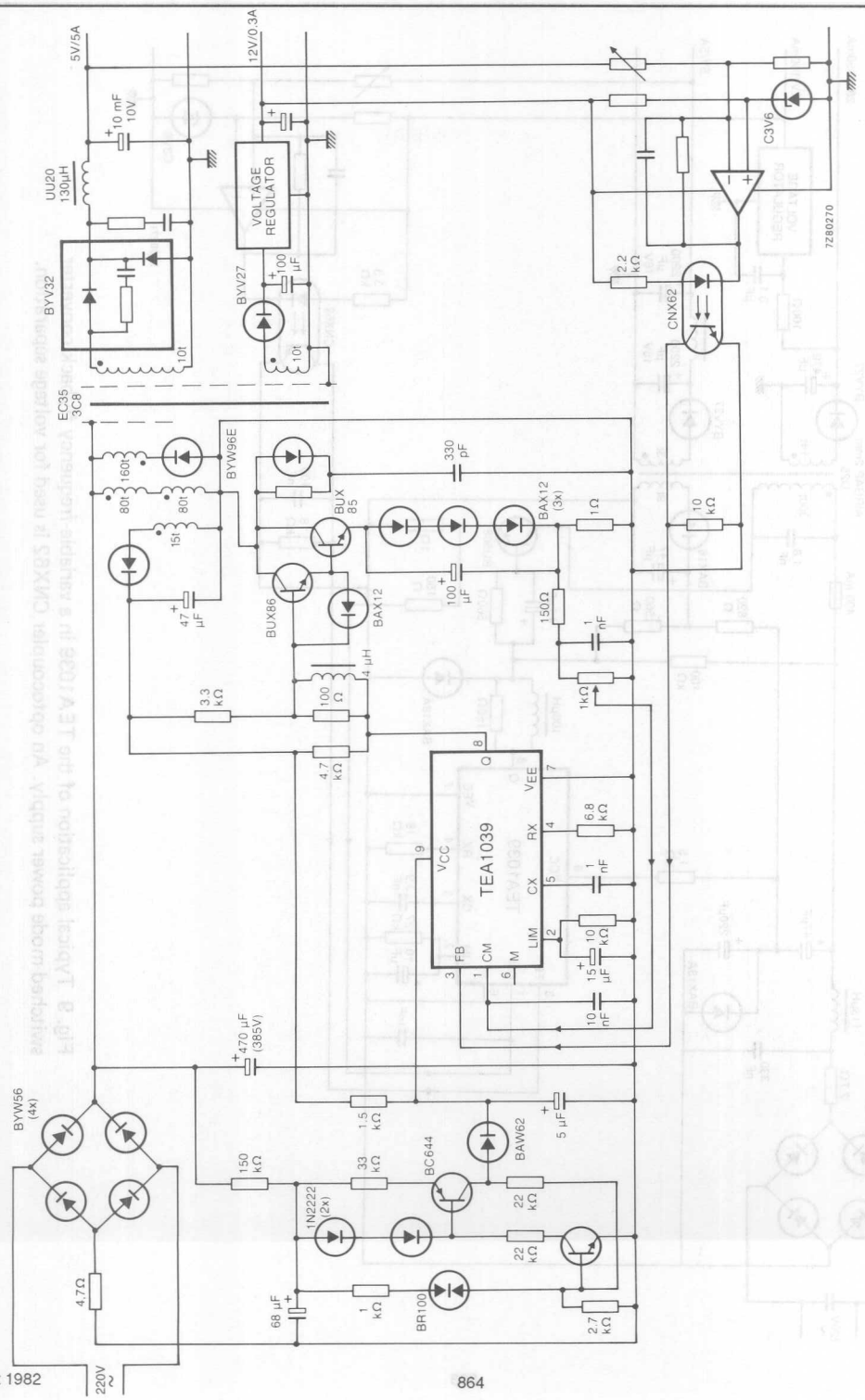


Fig. 10 Typical application of the TEA1039 in a fixed-frequency, variable duty factor forward converter switched-mode power supply. An optocoupler CNX62 is used for voltage separation.

APPLICATION INFORMATION SUPPLIED ON REQUEST

Section 15
Motor control circuits

INDEX

NE/SA5570	Brushless DC motor controller	867
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Section 15
Motor control circuits

Brushless DC motor controller

NE/SA5570

DESCRIPTION

The NE/SA/SE5570 is a three-phase brushless DC motor controller with a microprocessor-compatible serial input data port; 8-bit monotonic digital-to-analog converter; PWM comparator; oscillator; three Hall sensor inputs and six source/sink phase pre-drivers.

FEATURES

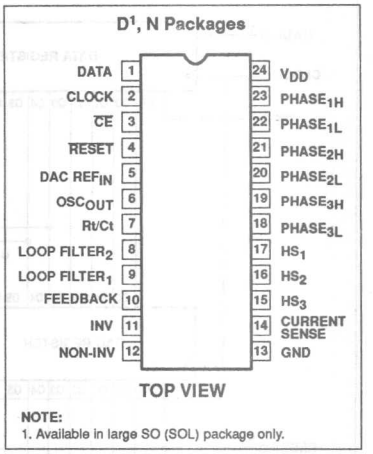
- 8-bit DAC
- Serial-to-parallel converter
- Output pre-drivers
- Entire switch mode conversion
- Adaptable to 60° or 120° commutation
- Overcurrent protection

APPLICATIONS

- Motor controller for three-phase brushless DC motor
- Robotics
- Computer peripherals

PIN CONFIGURATION

D[1], N Packages



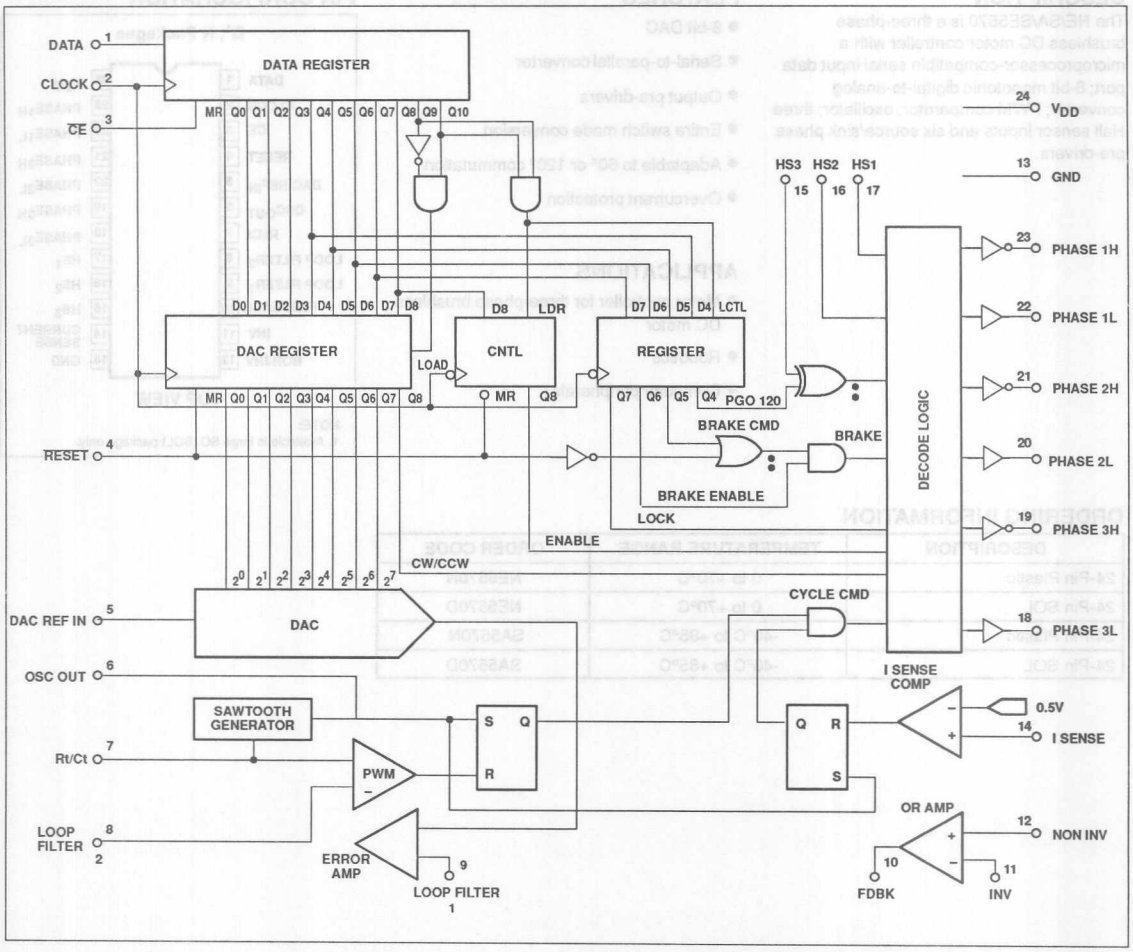
TOP VIEW

NOTE:
1. Available in large SO (SOL) package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic	0 to +70°C	NE5570N
24-Pin SOL	0 to +70°C	NE5570D
24-Pin Plastic	-40°C to +85°C	SA5570N
24-Pin SOL	-40°C to +85°C	SA5570D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING			UNIT
		NE5570	SA5570	SE5570	
	Temperature range				
T_A	Operating ambient	0 to 70	-40 to 85	-55 to 125	°C
T_J	Operating junction	-55 to 150	-55 to 150	-55 to 150	°C
T_{STG}	Storage	-65 to 150	-65 to 150	-65 to 150	°C
V_{DD}	Power supply	16	16	16	V
	Logic inputs, all	-0.3 to 15	-0.3 to 15	-0.3 to 15	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient temperature range		
	NE Grade	0 to 70	°C
	SA Grade	-40 to 85	°C
	SE Grade	-55 to 125	°C
T_J	Junction temperature range		
	NE Grade	0 to 90	°C
	SA Grade	-40 to 105	°C
	SE Grade	-55 to 145	°C
V_{DD}	Supply voltage	9.6 to 14.4	V

DC ELECTRICAL CHARACTERISTICS

Limits apply at V_{DD}=12V ±10%, V_{REF}=5V and over operating temperature range unless otherwise specified. Typical data applies at T_A=25°C

SYMBOL	PARAMETER	TEST CONDITIONS	SA/NE5570			SE5570			UNIT
			Min	Typ	Max	Min	Typ	Max	
Oscillator									
f_O	Frequency initial accuracy	T_A=25°C, R_T=2.49kΩ, C_T=22nF	18.5	20	21	18.5	20	21	kHz
f_C	Frequency drift over temp	R_T=2.49kΩ, C_T=22nF	18		22	18		22	kHz
	Supply voltage sensitivity	T_A=25°C		±2			±2		%/V
	Output pulse width	T_A=25°C, R_T=2.49kΩ, C_T=22nF		500	1000		500	1000	ns
Motor Phase Pre-Drivers									
t_R	Rise time	R_L=2kΩ to Gnd, C_L=2nF [1V to 11V]			500			500	ns
t_F	Fall time	R_L=2kΩ to V_{CC}, C_L=2nF [1V to 11V]			500			500	ns
I_{OUT}	I_{SOURCE} I_{SINK}	V_{OH}=8V	80			80			mA
		V_{OL}=3.1V	80			80			mA
V_{OUT}	V_{OH}	I_{SOURCE}=5mA	11	11.8		11	11.8		V
		I_{SOURCE}=80mA (over temp)	8	10		8	10		V
	V_{OL}	I_{SINK}=5mA		0.4	1		0.4	1	V
		I_{SINK}=80mA (over temp)		2	3.1		2	3.1	V
PWM Comparator									
I_{BIAS}	Input bias current				1			1	µA
Current Sense Comparator									
I_{BIAS}	Input bias current				1			1	µA
V_{TH}	Current sense trip level		350	500	600	350	500	600	mV
t_{PD}	Propagation delay to output drivers	C_L=2nF		250			250		ns
Error Amplifier									
I_{BIAS}	Input bias current				1			1	µA
V_{CM}	Input common-mode voltage range		0		5	0		5	V
V_{OL}	Large-signal voltage gain	V_{OUT}=1V to 11V	70	90		70	90		dB
PSRR	Power supply rejection ratio		60			60			dB
V_O	Output voltage swing	V_{IN}=+50mV, I_L=-150µA V_{IN}=-50mV, I_L=+150µA	11.5	11.7 0.2	0.5	11.5	11.7 0.2	0.5	V V

DC ELECTRICAL CHARACTERISTICS

(Continued) Limits apply at V_{DD}=12V +10%, V_{REF}=5V and over operating temperature range unless otherwise specified. Typical data applies at T_A=25°C.

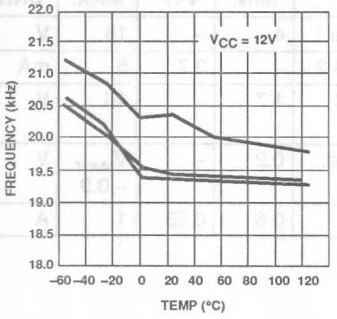
SYMBOL	PARAMETER	TEST CONDITIONS	SA/NE5570			SE5570			UNIT
			Min	Typ	Max	Min	Typ	Max	
Operational Amplifier									
V_{OS}	Offset voltage		-20	3	+20	-20	3	+20	mV
I_{BIAS}	Input bias current				1			1	µA
V_{CM}	80Input common-mode voltage range	T_A=25°C Over temp.	-0.3 0		5 5	-0.3 0		5 5	V
V_{OL}	Large signal voltage gain	V_{OUT}=1V to 11V	70	90		70	90		dB
PSRR	Power supply rejection ratio		60	90		60	90		dB
V_O	Output voltage swing	V_{IN}=+50mV, I_L=-150µA V_{IN}=-50mV, I_L=+150µA	11.5	11.7 0.2	0.5	11.5	11.7 0.2	0.5	V V
CMRR	<80>Common-mode rejection ratio	R_S=10kΩ	60	80		60	80		dB
GBW	Gain bandwidth	R_F=100kΩ		250			250		kHz
V_{NN}	Input noise voltage	F=1kHz							nV/√Hz
Digital-to-Analog Converter									
	Resolution				8			8	bits
INL	Integral non-linearity error			±1	±2		±1	±2	LSB
DNL	<80>Differential non-linearity error[1]			±0.5	±1		±0.5	±1	LSB
V_{FS}	Full-scale gain error	Error amp. A_V=1		±0.2	±0.8		±0.2	±0.8	%FS
	Full-scale temperature drift	$V_{REF}T_C$=0ppm/°C		20			20		ppm/°C
V_{ZS}	Zero-scale offset error	Error amp. A_V=1		±1	±2		±1	±2	LSB
Z_{IN}	Input impedance (DAC ref. in)		30	45	60	30	45	60	kΩ
t_S	Settling time to ±0.5 LSB			5			5		µs
t_{PLH}	80Propagation delay time (high)	Through DAC		200			200		ns
t_{PHL}	80Propagation delay time (low)	Through DAC		200			200		ns
Logic Inputs									
V_{IH}	Input voltage: TTL high		2.0		12	2.0		12	V
V_{IL}	Input voltage: TTL low		0		0.8	0		0.8	V
I_{IH}	Input current: TTL high				±1			±1	µA
I_{IL}	Input current: TTL low				±1			±1	µA
Supply Current									
I_{DD}				1.8	5.0		1.8	5.0	mA

NOTES:

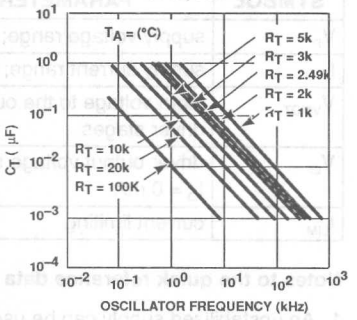
1. Monotonicity guaranteed over operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

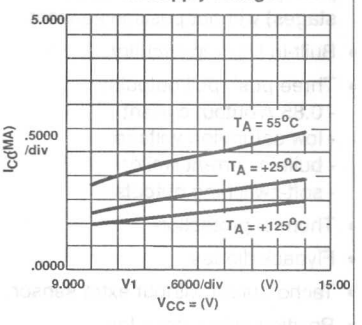
NE5570 Oscillator Frequency vs Temperature



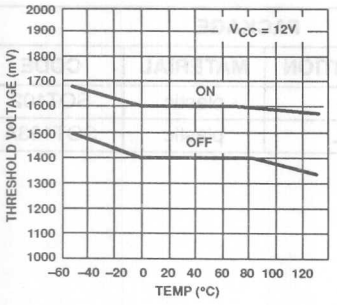
Oscillator Frequency vs R_T and C_T



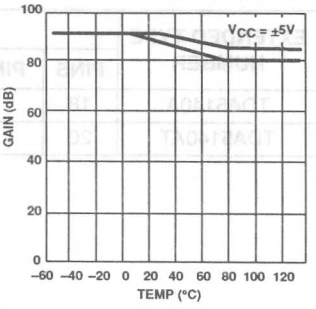
NE5570 Oscillator Frequency vs Supply Voltage



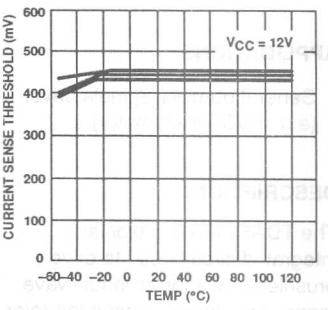
NE5570 Oscillator Output Pulse Width



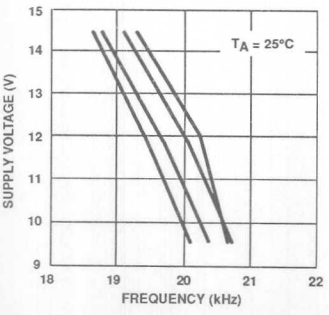
NE5570 Op Amp Gain vs Temperature



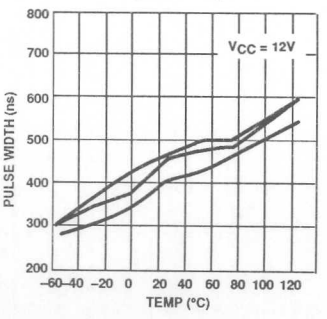
NE5570 Current Sense Comparator Threshold vs Temperature



I_{CC} vs V_{CC}



NE5570 Logic Threshold Voltage vs Temperature



Brushless DC motor drive circuit TDA5140A/AT

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - 0.85 A output current
  - low saturation voltage
  - built-in current limiter
  - soft-switching outputs
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Position pulse stage for phase-locked-loop control
- Transconductance amplifier for an external control transistor

APPLICATIONS

- General purpose spindle driver (e.g. HDD, drum motor)

DESCRIPTION

The TDA5140A is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for a hard disk drive motor.

QUICK REFERENCE DATA

Measured over full voltage and temperature range

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range; note 1	4	–	18	V
I_P	supply current range; note 2	–	3.7	5	mA
V_{VMOT}	input voltage to the output driver stages	1.7	–	16	V
V_O	driver output voltage range; I_O = 0 mA	0.2	–	V_{VMOT} – 0.9	V
I_{LIM}	current limiting	0.6	0.85	1	A

Notes to the quick reference data

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN and –AMP IN at 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5140A	18	DIL	plastic	SOT102
TDA5140AT	20	SOL	plastic	SOT163A

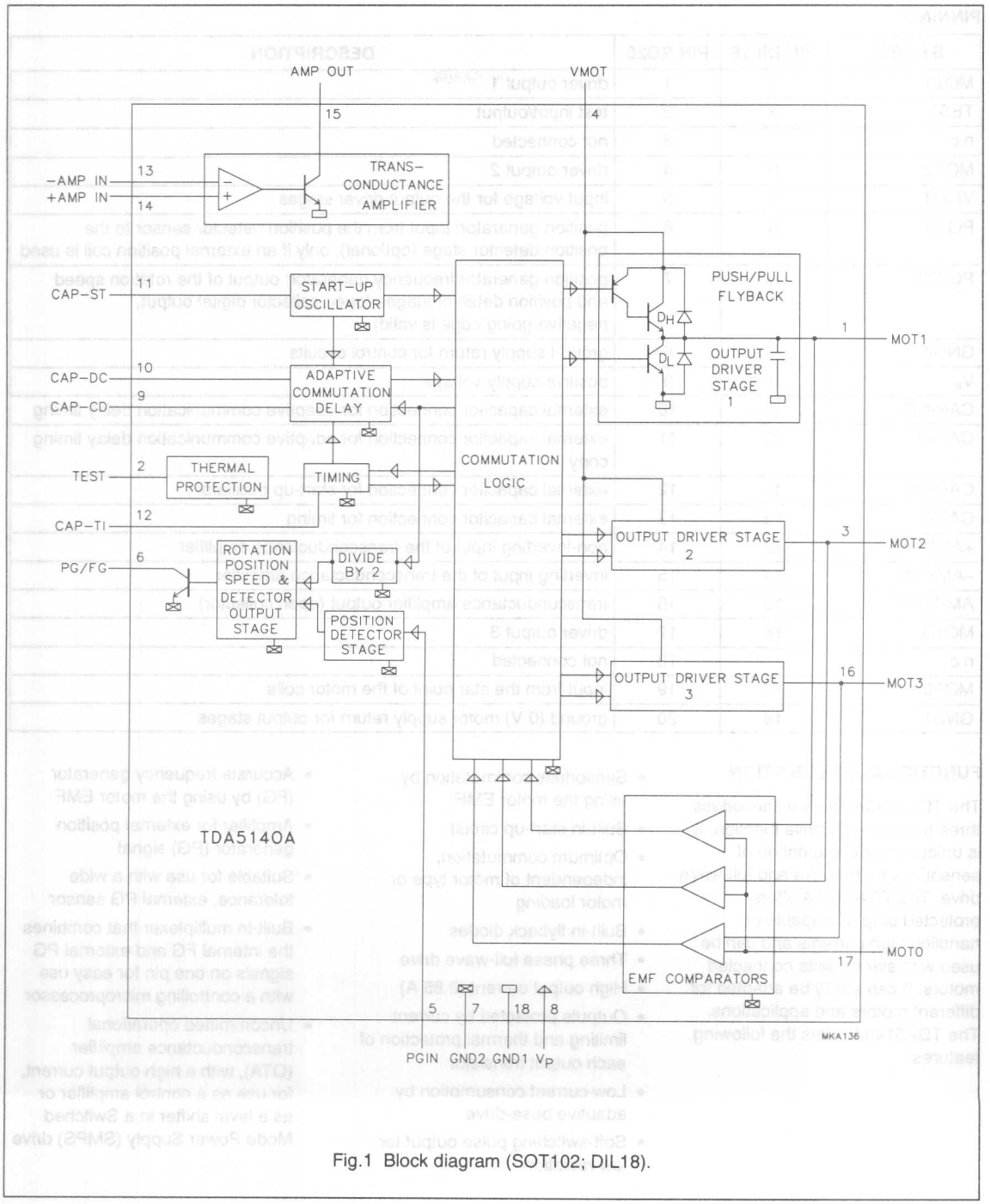


Fig.1 Block diagram (SOT102; DIL18).

PINNING

SYMBOL	PIN DIL18	PIN SO20	DESCRIPTION
MOT1	1	1	driver output 1
TEST	2	2	test input/output
n.c.		3	not connected
MOT2	3	4	driver output 2
VMOT	4	5	input voltage for the output driver stages
PG IN	5	6	position generator: input from the position detector sensor to the position detector stage (optional); only if an external position coil is used
PG/FG	6	7	position generator/frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
GND2	7	8	ground supply return for control circuits
V_P	8	9	positive supply voltage
CAP-CD	9	10	external capacitor connection for adaptive communication delay timing
CAP-DC	10	11	external capacitor connection for adaptive communication delay timing copy
CAP-ST	11	12	external capacitor connection for start-up oscillator
CAP-TI	12	13	external capacitor connection for timing
+AMP IN	13	14	non-inverting input of the transconductance amplifier
–AMP IN	14	15	inverting input of the transconductance amplifier
AMP OUT	15	16	transconductance amplifier output (open collector)
MOT3	16	17	driver output 3
n.c.		18	not connected
MOT0	17	19	input from the star point of the motor coils
GND1	18	20	ground (0 V) motor supply return for output stages

FUNCTIONAL DESCRIPTION

The TDA5140A offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5140A offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5140A offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Built-in flyback diodes
- Three phase full-wave drive
- High output current (0.85 A)
- Outputs protected by current limiting and thermal protection of each output transistor
- Low current consumption by adaptive base-drive
- Soft-switching pulse output for low radiation
- Accurate frequency generator (FG) by using the motor EMF
- Amplifier for external position generator (PG) signal
- Suitable for use with a wide tolerance, external PG sensor
- Built-in multiplexer that combines the internal FG and external PG signals on one pin for easy use with a controlling microprocessor
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive

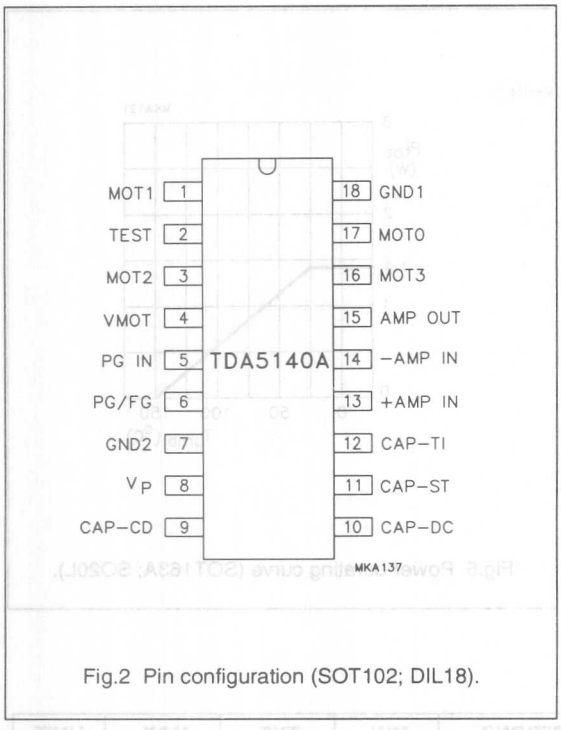


Fig.2 Pin configuration (SOT102; DIL18).

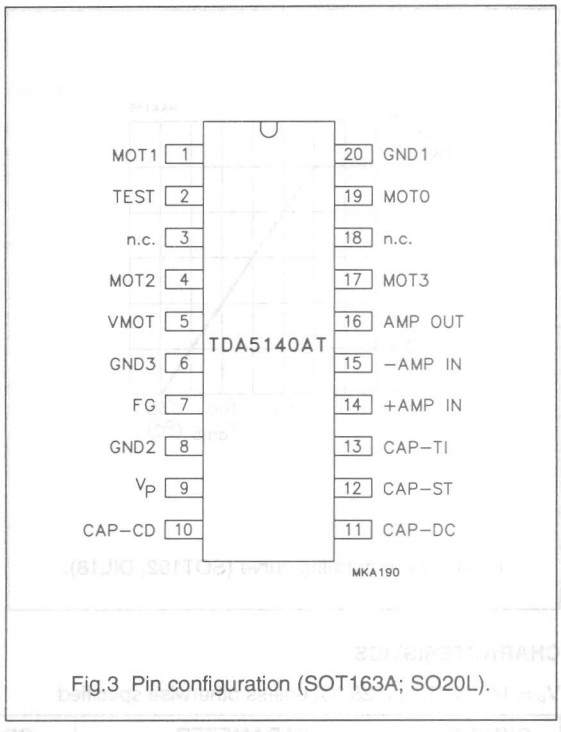


Fig.3 Pin configuration (SOT163A; SO20L).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	–	18	V
V_I	input voltage; all pins except VMOT: $V_I < 18$ V	–0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage	–0.5	17	V
V_O	output voltage AMP OUT and PG/FG	GND	V_P	V
V_O	output voltage MOT0, MOT1, MOT2 and MOT3	–1	$V_{VMOT} + V_D$	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC	–	2.5	V
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
P_{tot}	total power dissipation	–	see Figs 4 and 5	
V_{es}	electrostatic voltage; see also handling	–	500	V

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 2. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses – on each pin referenced to ground.

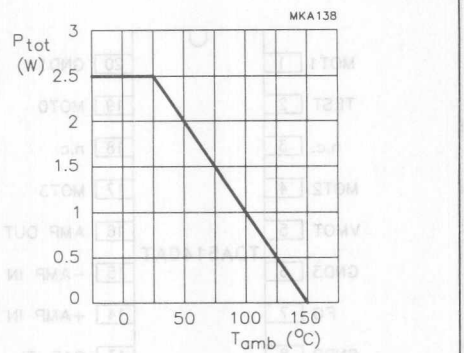


Fig.4 Power derating curve (SOT102; DIL18).

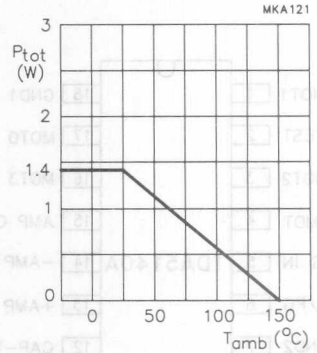


Fig.5 Power derating curve (SOT163A; SO20L).

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range	note 1	4	–	18	V
I_P	supply current range	note 2	–	3.7	5	mA
V_{VMOT}	input voltage to the driver output stages	see Fig.1	1.7	–	16	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
MOT0 - centre tape						
V_I	input voltage range		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	0	µA
V_{CSW}	comparator switching level	note 3	±20	±30	±40	mV
ΔV_{CSW}	variation in comparator switching levels		–3	0	+3	mV
V_H	comparator input hysteresis		–	75	–	µV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MOT1, MOT2 and MOT3						
V_O	driver output voltage range	I_O = 100 mA	0.4	–	V_{VMOT} – 1.2	V
V_{DO}	drop-out voltage	I_O = 500 mA	–	2.1	–	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA	–	–	180	mV
I_{LIM}	current limiting	lower transistor; V_{CE} = 6 V	0.6	0.85	1	A
t_{tr}	transition time switching output	V_{VMOT} = 14.5 V; see Fig.6	5	9	15	µs
V_{DHF}	diode forward voltage (diode D_H)	I_O = –500 mA; notes 4 and 5; see Fig.1	–	–	1.5	V
V_{DLF}	diode forward voltage (diode D_L)	I_O = 500 mA; notes 4 and 5; see Fig.1	–1.5	–	–	V
I_{DM}	peak diode current	note 5	–	–	1	A
+AMP IN and -AMP IN						
V_{IAMP}	input voltage range		–0.3	–	V_P – 1.7	V
V_{IAMP}	differential mode voltage without 'latch-up'		–	–	$\pm V_P$	V
I_B	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{OFFSET}	input offset voltage		–	–	10	mV
I_I	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_{Omax}	maximum output voltage		18	–	–	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	–	60	–	mA/µs
G_{tr}	transfer gain		0.3	–	–	S
PG IN						
V_I	input voltage		–0.3	–	5	V
I_B	input bias current		–	–	650	nA
R_I	input resistance		5	–	30	kΩ
V_{CWS}	comparator switching level		86	–	107	mV
V_H	comparator input hysteresis		–	±8	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PG/FG						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
V_{OHmax}	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	µs
	ratio of PG/FG frequency and commutation frequency		–	1 : 2	–	
δ	duty factor		–	50	–	%
t_{PL}	pulse width LOW	after a PG IN pulse	5	7	18	µs
CAP-ST						
I_I	output sink current		1.5	2.0	2.5	µA
I_O	output source current		–2.5	–2.0	–1.5	µA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_I	output sink current		–	28	–	µA
I_{OH}	HIGH level output source current		–	–57	–	µA
I_{OL}	LOW level output source current		–	–5	–	µA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-CD						
I_I	ouput sink current		10.6	16.2	22	µA
I_O	output source current		–5.3	–8.1	–11	µA
I_I/I_O	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		850	875	900	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V
CAP-DC						
I_I	output sink current		10.1	15.5	20.9	µA
I_O	output source current		–20.9	–15.5	–10.1	µA
I_I/I_O	ratio of sink to source current		0.9	1.025	1.15	

Notes to the characteristics

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P and I_O = 0 mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in the high-impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

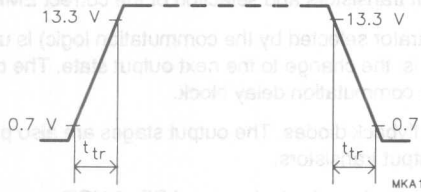
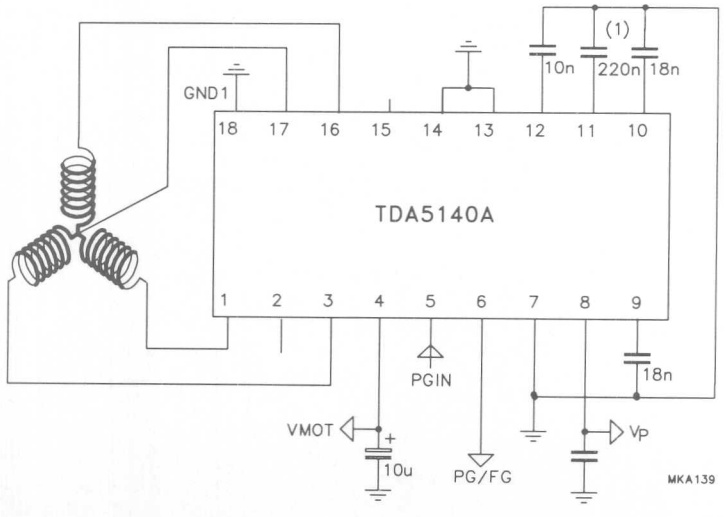


Fig.6 Output transition time measurement.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency

Fig.7 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction (see Fig.8)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The zero-crossings can be used to provide speed information such as the tacho signal FG. A VCR scanner also requires a PG phase sensor. This circuit has an interface for a simple pick-up coil. A multiplexer circuit is also provided to combine the FG and PG signals in time. This digital signal, FGPG, is available at an open-collector output.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5140A also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5140A is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented), possibility of using a pick-up coil without bias current.

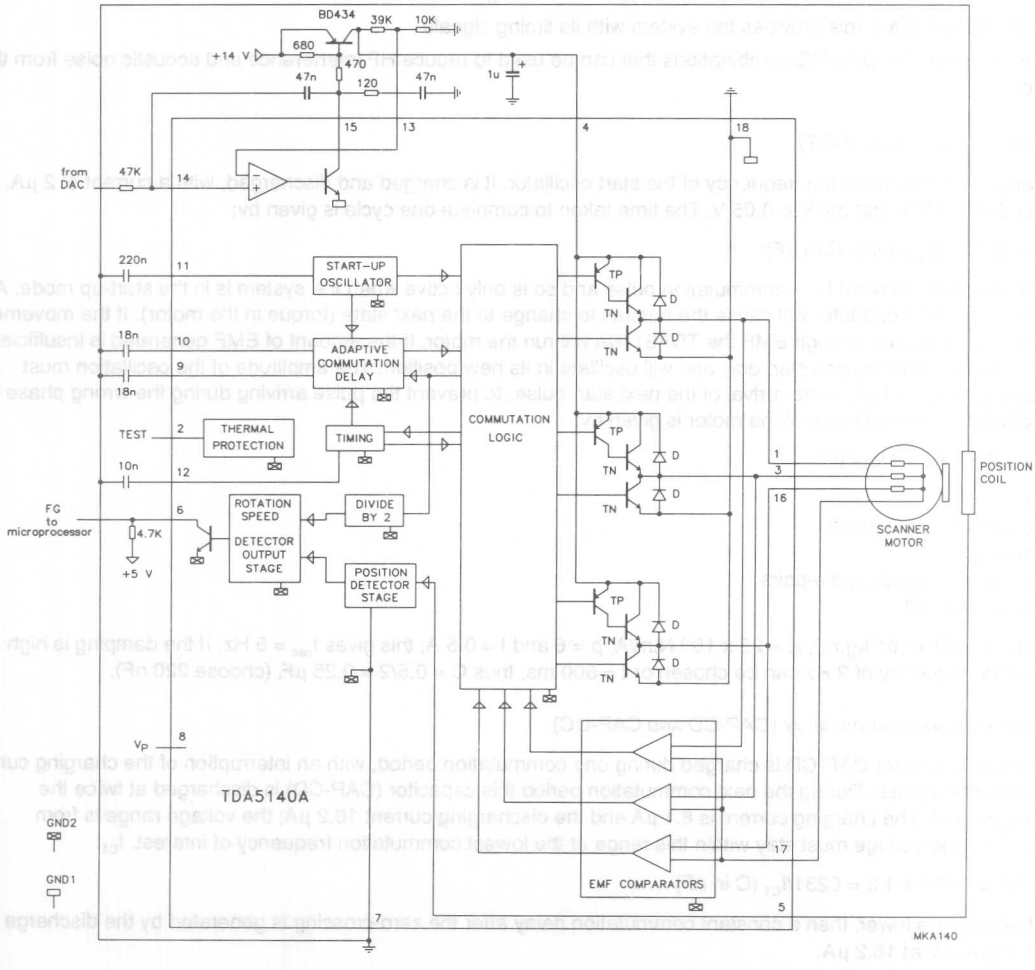


Fig.8 Typical application of the TDA5140A as a scanner driver, with use of OTA.

ADJUSTMENTS

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals
- Three external, damping RC-combinations that can be used to reduce HF interference and acoustic noise from the motor

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 V to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

t_{start} = (2.15 x C) s (with C in μF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5140A will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$f_{osc} = 0.5/\pi \times (K_t \times I \times p/J)^{1/2}$

where:
K_t = torque constant (N.m/A)
I = current (A)
p = number of magnetic pole-pairs
J = inertia J ($kg.m^2$)

Example: J = 72 x 10^{-6} $kg.m^2$, K = 25 x 10^{-3} N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF, (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

$C = 8.1 \times 10^{-6}/ f \times 1.3 = 6231/f_{C1}$ (C in nF)

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 μA.

maximum delay = (0.076 x C) ms (witch C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

CAP-CD = 6231/400 = 15.6 (choose 18 nF)

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 20 μA. The same value can be chosen as for CAP-CD. Figure 9 illustrates typical voltage waveforms.

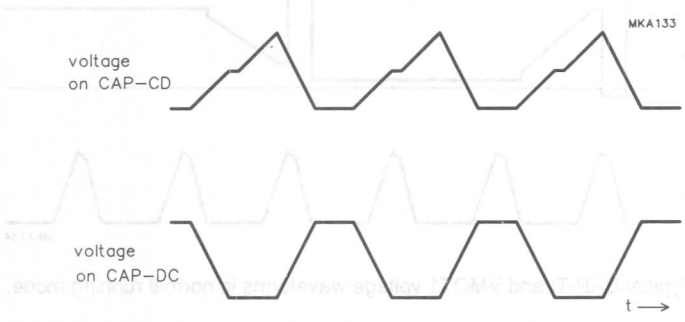


Fig.9 CAP-CD and CAP-DC voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 µA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 µA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 µA. The watchdog time is the time taken to charge the capacitor, with a current of 5 µA, from 0.3 to 2.2 V. The value of CAP-TI is given by:

$$C = 5 \times 10^{-6} \times t_m/1.9 = 2.63\, t_m \text{(C in nF; t in ms)}$$

Example: If after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 20 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$$C = 2.63 \times 3.5 = 9.2 \text{ (choose 10 nF)}$$

Typical voltage waveforms are illustrated by Fig.10.

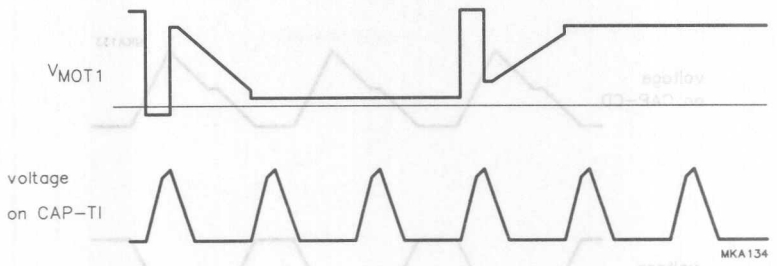


Fig.10 Typical CAP-TI and VMOT1 voltage waveforms in normal running mode.

Note to Fig.10

If the chosen value of CAP-TI is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

THE EXTERNAL DAMPING COMPONENTS

Flyback pulses from the motor windings may cause HF interference and acoustic noise. The flyback pulses can be damped by RC-combinations in parallel with the motor windings. This reduces the HF interference; it also reduces the acoustic noise by several dB, depending on the motor construction.

These damping components also have negative effects. They not only dissipate energy from the flyback pulses, but also contribute to the overall energy consumption. Other negative effects are discussed below.

One negative effect is the distortion of the motor EMF sensed by the comparators in the TDA5140A. This distortion may influence the correct functioning of the TDA5140A, for example, an (damped) oscillation occurring after the winding has been switched off. This oscillation must be critically (or over critically) damped, so that:

$R^2 \times C = 4 \times L$ (L = inductance of one coil, R and C for damping)

A second requirement is that the effect of the damping components must be negligible by the time that the zero-crossing of the EMF is expected. This is because the remainder of the step (due to RC components) causes shifting of the zero-crossing. For a critically damped combination the voltage can be calculated as a negative exponential with $\omega_o \times t$.

Example: Commutation frequency = 900 Hz, so t = 1100 µs, the time taken from the end of the diode pulse to the zero-crossing of the EMF will be approximately t = 440 µs. If a damping voltage from 9 V to 3 mV is required, then the reduction is 3000-fold, or e exp–8 = e exp $-\omega_o \times t$. This gives ω_o = 18180 rad/s. With L = 3 mH, C is found to be 1.01 µF (use 1 µF) and R is found to be 109.1 Ω (use 100 Ω).

A motor voltage of 7 V (peak-to-peak) at 150 Hz gives 3300 V/s, thus a 3 mV remainder shifts the zero-crossing 1 µs. Eddy currents will also contribue to this phase shift. A shift of 20 µs corresponds with 0.18 degrees (mechanically) for a 1500 rpm motor, or 0.1 mm on a VHS scanner drum.

OTHER DESIGN ASPECTS

There are other design aspects concerning the application of the TDA5140A besides the commutation function. They are:

- Generation of the tacho signal FG
- A built-in interface for a PG sensor
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability

FG SIGNAL

The FG signal is generated in the TDA5140A by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing (except for PG). The negative-going edges are called FG pulses because they generate an interrupt in a controlling microprocessor.

The accuracy of the FG output signal (jitter) is very good. This accuracy depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: A three phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 450 Hz.

PG SIGNAL

The accuracy of the PG signal in applications such as VCR must be high (phase information). This accuracy is obtained by combining the accurate FG signal with the PG signal by using a wide tolerance external PG sensor. The external PG signal (PG IN) is only used as an indicator to select a particular FG pulse. This pulse differs from the other FG pulses in that a short LOW-time of 15 µs after a HIGH-to-LOW transition. All other FG pulses have a 50% duty factor (see Fig.11).

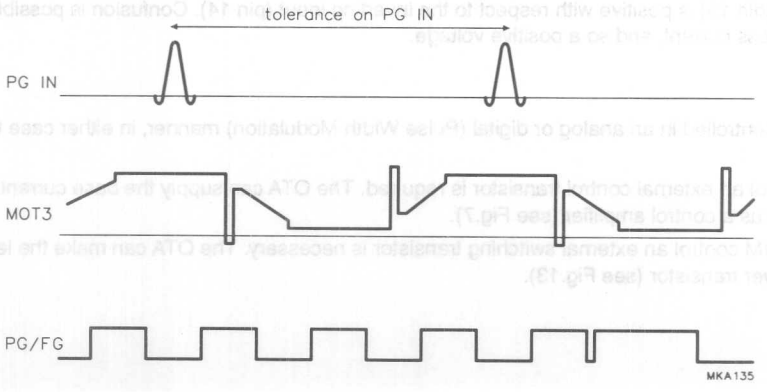


Fig.11 Timing and the FG and PGIN signals.

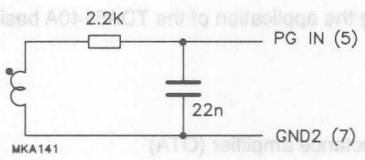


Fig.12 Pick-up coil as PG sensor.

The special PG pulse is derived from the negative-going zero-crossing from the MOT3 output (pin 16). The external PG signal (PG IN on pin 5) must sense a positive going (>80 mV) within 1.5 to 7.5 commutation periods before the negative-going zero-crossing in MOT3 (see Fig.11).

The voltage requirements of the PG IN input are shut that a cheap pick-up coil can be used as a sensor (see Fig.12).

Example: If p = 6, then one revolution contains 6 x 6 = 36 commutations. The tolerance is 6 periods, that is 60 degrees (mechanically) or 6.67 ms at 1500 rpm.

If a PG sensor is not used, the PG IN input must be grounded, this will result in a 50% duty factor FG signal.

The Operational Transconductance Amplifier (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier or as a level converter in a Switched Mode Power Supply (SMPS). The common mode input range includes ground (GND) and rises to V_P – 1.7 V. The high sinking current enables the OTA to drive a power transistor directly in an analog control amplifier or in a SMPS drive.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (pin 15) to the positive supply, a positive-going voltage is found when the non-inverting input (pin 13) is positive with respect to the inverting input (pin 14). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

Motor Control

DC motors can be controlled in an analog or digital (Pulse Width Modulation) manner, in either case the OTA may be used as follows:

- With analog control an external control transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.7).
- With digital or PWM control an external switching transistor is necessary. The OTA can make the level translation and drive the power transistor (see Fig.13).

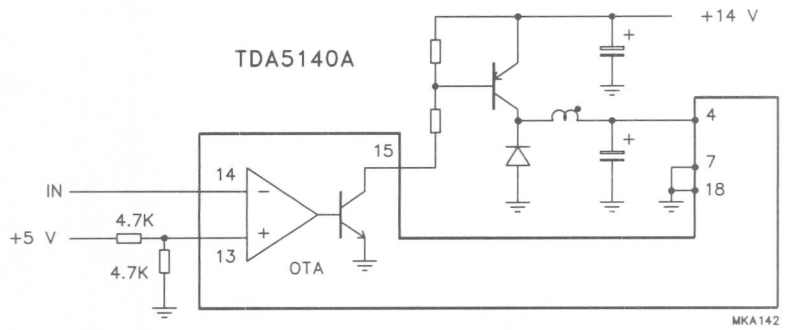


Fig.13 PWM drive of the output stages, OTA used as level converter.

A further aspect of motor control is current or voltage control; the TDA5140A is intended for voltage control applications. Both ground pins (7 and 18) must be connected externally. However the current from pin 7 can be considered as small and constant with respect to the current in the output stages. A resistor connected between pins 7, 18 and ground can be used for current control. Care must be taken that the voltage on pins 7, 18 does not disturb the (digital) FGPG signal too much (this signal is added to the digital signal).

An alternative method of voltage control is to increase the output impedance for a certain frequency, such as the commutation frequency; the circuit illustrated by Fig.7 uses this method. The low output impedance increases to approximately 10 Ω at 900 Hz. This circuit diagram is an example of the application of the TDA5140A with a VTR scanner for a PAL recorder running at 1500 rpm. The input signal is a PWM 5 V signal. The FGPG signal is read by a microprocessor that runs the servo control program.

A final aspect of motor control is braking; decreasing the speed to zero. No provisions have been made for this function. However, the generated voltage of the motor is rectified by the flyback diodes. If the voltage is loaded by a current drain on pin 5 then the motor will generate a braking torque that is proportional to the current.

Reliability

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high.

It is possible, that when braking (see previous section), the motor voltage (via the flyback diodes and the impedance on pin 5) may cause higher currents than allowed (>0.6 A). These currents must be limited externally.

Fig.13 PWM drive of the output stages. OTA used as level converter.

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Brushless DC motor drive circuit TDA5141/T/AT

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - 1.8 A output current
  - low saturation voltage
  - built-in current limiter
  - soft-switching outputs
- Thermal protection
- Flyback diodes
- Tacho output without extra sensor
- Position pulse stage for phase-locked-loop control
- Transconductance amplifier for an external control transistor

APPLICATIONS

- General purpose spindle driver (e.g. HDD, drum motor)

DESCRIPTION

The TDA5141 is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for a hard disk drive motor.

QUICK REFERENCE DATA

Measured over full voltage and temperature range

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range; note 1	4	–	18	V
I_P	supply current range; note 2	–	4.9	6.8	mA
V_{VMOT}	input voltage to the output driver stages	1.7	–	16	V
V_O	driver output voltage range; I_O = 0 mA	0.2	–	V_{VMOT} – 0.9	V
I_{LIM}	current limiting	1.3	1.8	2.3	A

Notes to the quick reference data

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN and –AMP IN at 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5141	18	DIL	plastic	SOT102
TDA5141T	28	SOL	plastic	SOT136A
TDA5141AT	20	SOL	plastic	SOT163A

Brushless DC motor drive circuit TDA5141/T/AT

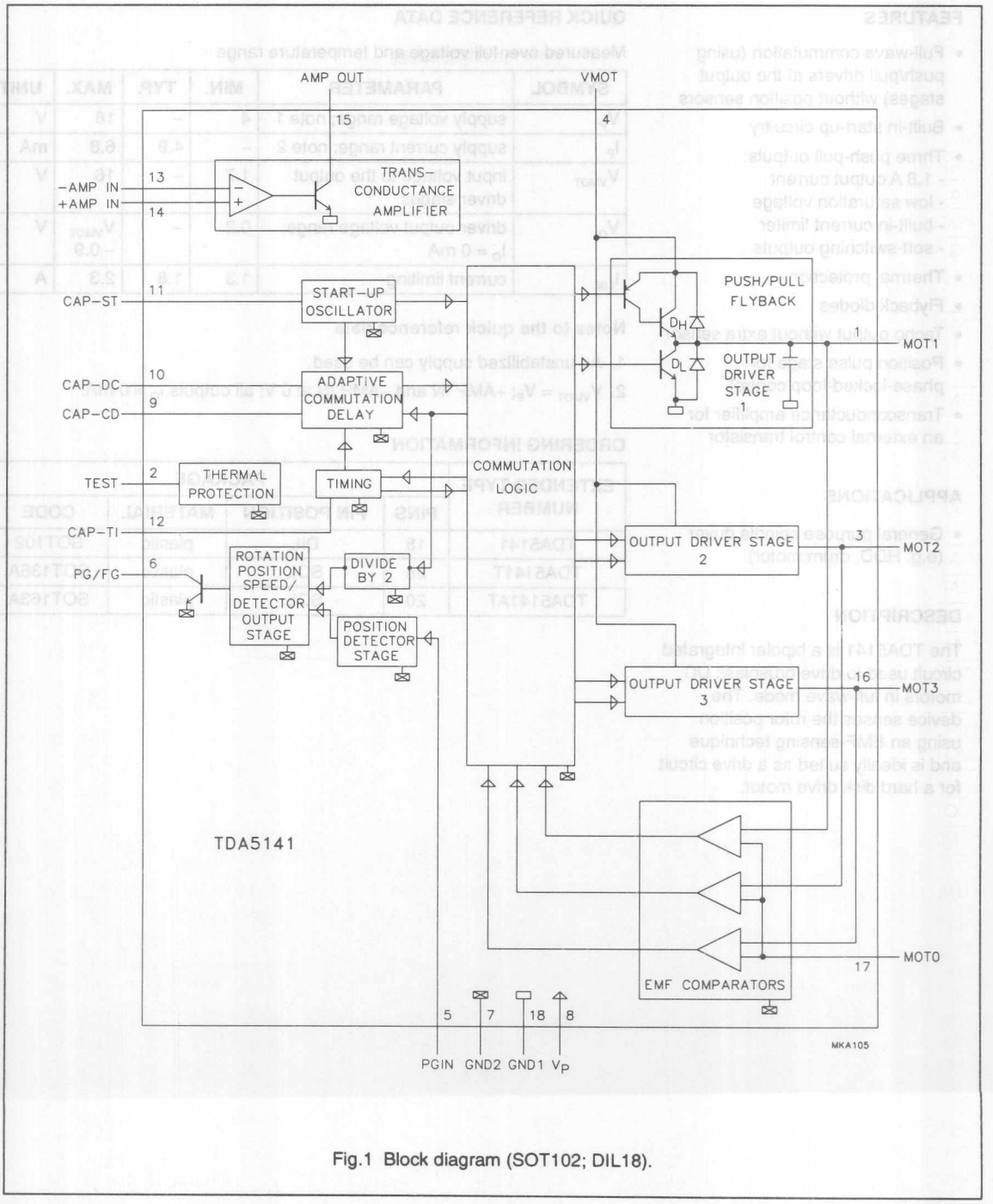


Fig.1 Block diagram (SOT102; DIL18).

Brushless DC motor drive circuit TDA5141/T/AT

PINNING

SYMBOL	PIN DIL18	PIN SO20	PIN SO28	DESCRIPTION
MOT1	1	1	1, 2	driver output 1
TEST	2	2	3	test input/output
n.c.		3	4	not connected
MOT2	3	4	5, 6	driver output 2
n.c.			7	not connected
VMOT	4	5	8, 9	input voltage for the output driver stages
PG IN	5	6	10	position generator: input from the position detector sensor to the position detector stage (optional); only if an external position coil is used
PG/FG	6	7	11	position generator/frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
GND2	7	8	12	ground supply return for control circuits
V_P	8	9	13	positive supply voltage
CAP-CD	9	10	14	external capacitor connection for adaptive communication delay timing
CAP-DC	10	11	15	external capacitor connection for adaptive communication delay timing copy
CAP-ST	11	12	16	external capacitor connection for start-up oscillator
CAP-TI	12	13	17	external capacitor connection for timing
+AMP IN	13	14	18	non-inverting input of the transconductance amplifier
–AMP IN	14	15	19	inverting input of the transconductance amplifier
AMP OUT	15	16	20	transconductance amplifier output (open collector)
n.c.			21, 22	not connected
MOT3	16	17	23, 24	driver output 3
n.c.		18	25	not connected
MOT0	17	19	26	input from the star point of the motor coils
GND1	18	20	27, 28	ground (0 V) motor supply return for output stages

FUNCTIONAL DESCRIPTION

The TDA5141 offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5141 offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5141 offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Built-in flyback diodes
- Three phase full-wave drive
- High output current (1.8 A)
- Outputs protected by current limiting and thermal protection of each output transistor
- Low current consumption by adaptive base-drive
- Soft-switching pulse output for low radiation
- Accurate frequency generator (FG) by using the motor EMF
- Amplifier for external position generator (PG) signal

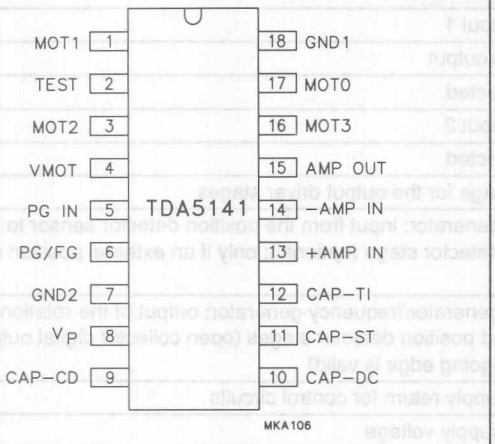


Fig.2 Pin configuration (SOT102; DIL18).

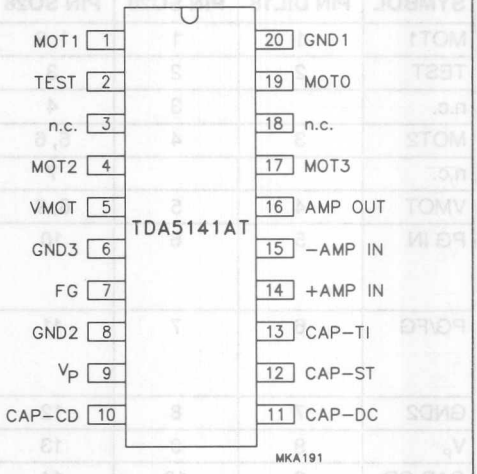


Fig.3 Pin configuration (SOT163A; SO20L).

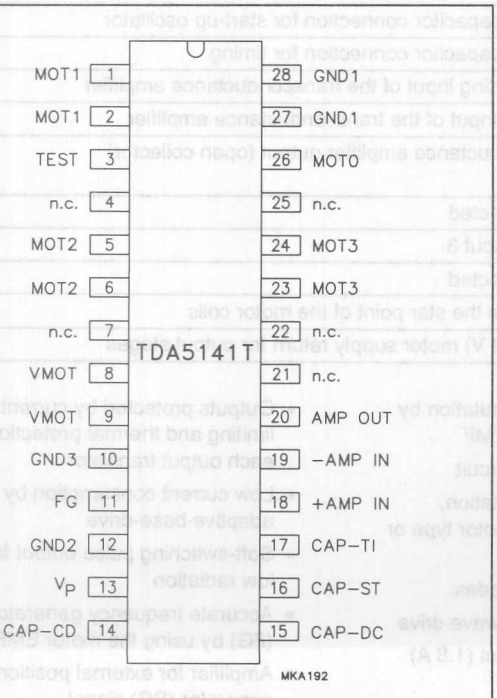


Fig.4 Pin configuration (SOT136A; SO28L).

- Suitable for use with a wide tolerance, external PG sensor
- Built-in multiplexer that combines the internal FG and external PG signals on one pin for easy use with a controlling microprocessor
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	–	18	V
V_I	input voltage; all pins except VMOT: $V_I < 18$ V	−0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage	−0.5	17	V
V_O	output voltage AMP OUT and PG/FG	GND	V_P	V
V_O	output voltage MOT0, MOT1, MOT2 and MOT3	−1	$V_{VMOT} + V_D$	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC	–	2.5	V
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
P_{tot}	total power dissipation	–	see Figs 5, 6 and 7	
V_{es}	electrostatic voltage; see also handling	–	500	V

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 2. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses – on each pin refernced to ground.

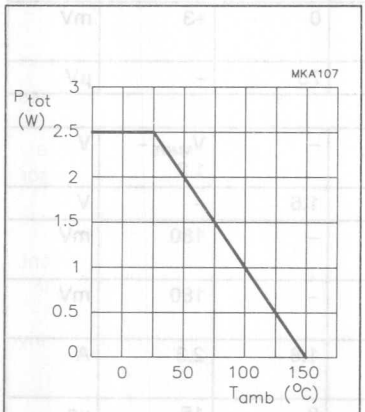


Fig.5 Power derating curve (SOT102; DIL18).

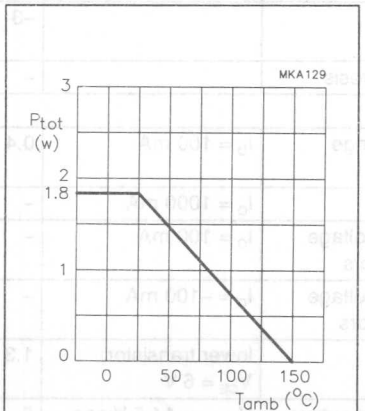


Fig.6 Power derating curve (SOT163A; SO20L).

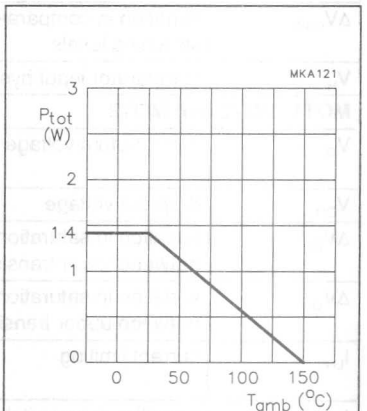


Fig.7 Power derating curve (SOT136A; SO28L).

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range	note 1	4	–	18	V
I_P	supply current range	note 2	–	4.9	6.8	mA
V_{VMOT}	input voltage to the driver output stages	see Fig.1	1.7	–	16	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
MOT0 - centre tape						
V_I	input voltage range		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	0	µA
V_{CSW}	comparator switching level	note 3	±20	±30	±40	mV
ΔV_{CSW}	variation in comparator switching levels		–3	0	+3	mV
V_H	comparator input hysteresis		–	75	–	µV
MOT1, MOT2 and MOT3						
V_O	driver output voltage range	I_O = 100 mA	0.4	–	V_{VMOT} – 1.2	V
V_{DO}	drop-out voltage	I_O = 1000 mA	–	1.6	–	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA	–	–	180	mV
I_{LIM}	current limiting	lower transistor; V_{CE} = 6 V	1.3	1.8	2.3	A
t_{tr}	transition time switching output	V_{VMOT} = 14.5 V;see Fig.8	5	9	15	µs
V_{DHF}	diode forward voltage (diode D_H)	I_O = –500 mA; notes 4 and 5; see Fig.1	–	–	1.5	V
V_{DLF}	diode forward voltage (diode D_L)	I_O = 500 mA; notes 4 and 5; see Fig.1	–1.5	–	–	V
I_{DM}	peak diode current	note 5	–	–	1.8	A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
+AMP IN and -AMP IN						
V_{IAMP}	input voltage range		−0.3	–	V_P − 1.7	V
V_{IAMP}	differential mode voltage without 'latch-up'		–	–	$\pm V_P$	V
I_B	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{OFFSET}	input offset voltage		–	–	10	mV
I_I	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_{Omax}	maximum output voltage		–	–	18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	–	60	–	mA/µs
G_{tr}	transfer gain		0.3	–	–	S
PG IN						
V_I	input voltage		−0.3	–	V_P − 1.7	V
I_B	input bias current		–	–	650	nA
R_I	input resistance		5	–	30	kΩ
V_{CWS}	comparator switching level		86	–	107	mV
V_H	comparator input hysteresis		–	±8	–	mV
PG/FG						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
V_{OHmax}	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	µs
	ratio of PG/FG frequency and commutation frequency		–	1 : 2	–	
δ	duty factor		–	50	–	%
t_{PL}	pulse width LOW	after a PG IN pulse	5	7	30	µs
CAP-ST						
I_I	output sink current		1.5	2.0	2.5	µA
I_O	output source current		−2.5	−2.0	−1.5	µA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_I	output sink current		–	28	–	µA
I_{OH}	HIGH level output source current		–	−57	–	µA
I_{OL}	LOW level output source current		–	−5	–	µA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CAP-CD						
I_I	ouput sink current		10.6	16.2	22	µA
I_O	output source current		–5.3	–8.1	–11	µA
I_I/I_O	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		–	875	–	mV
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V
CAP-DC						
I_I	output sink current		10.1	15.5	20.9	µA
I_O	output source current		–20.9	–15.5	–10.1	µA
I_I/I_O	ratio of sink to source current		0.9	1.025	1.15	

Notes to the characteristics

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P and $I_O = 0$ mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3.
4. Drivers are in the high-impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

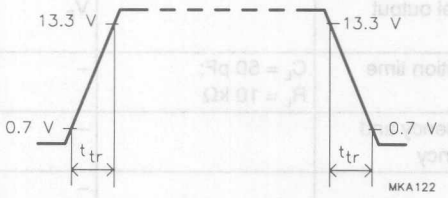
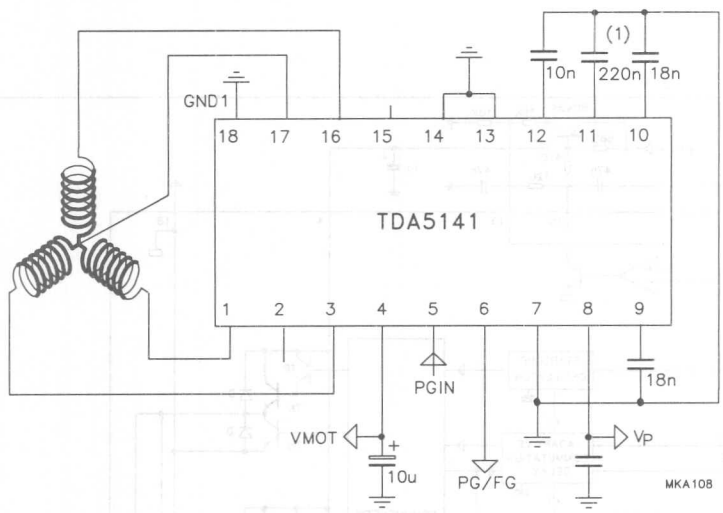


Fig.8 Output transition time measurement.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency

Fig.9 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction (see Fig.10)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The zero-crossings can be used to provide speed information such as the tacho signal FG. A VCR scanner also requires a PG phase sensor. This circuit has an interface for a simple pick-up coil. A multiplexer circuit is also provided to combine the FG and PG signals in time. This digital signal, FGPG, is available at an open-collector output.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5141 also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5141 is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented), possibility of using a pick-up coil without bias current.

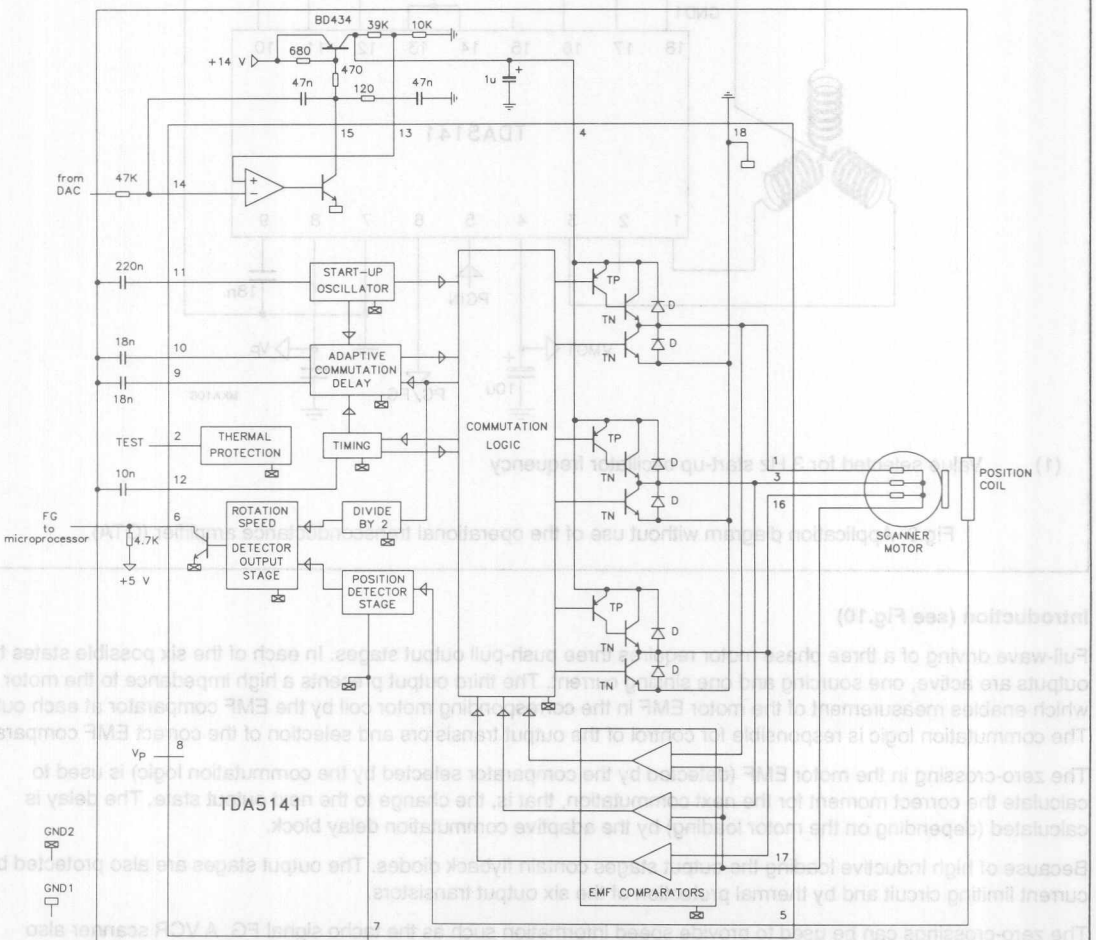


Fig.10 Typical application of the TDA5141 as a scanner driver, with use of OTA.

ADJUSTMENTS

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals
- Three external, damping RC-combinations that can be used to reduce HF interference and acoustic noise from the motor

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 µA, from 0.05 V to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

t_{start} = (2.15 x C) s (with C in µF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5141 will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$f_{osc} = 0.5/\pi \times (K_t \times I \times p/J)^{1/2}$

where:
K_t = torque constant (N.m/A)
I = current (A)
p = number of magnetic pole-pairs
J = inertia J ($kg.m^2$)

Example: J = 72 x 10^{-6} $kg.m^2$, K = 25 x 10^{-3} N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 µF, (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 µA and the discharging current 16.2 µA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

C = 8.1 x 10^{-6}/ f x 1.3 = 6231/f_{C1} (C in nF)

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 µA.

maximum delay = (0.076 x C) ms (witch C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

CAP-CD = 6231/400 = 15.6 (choose 18 nF)

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 20 µA. The same value can be chosen as for CAP-CD. Figure 11 illustrates typical voltage waveforms.

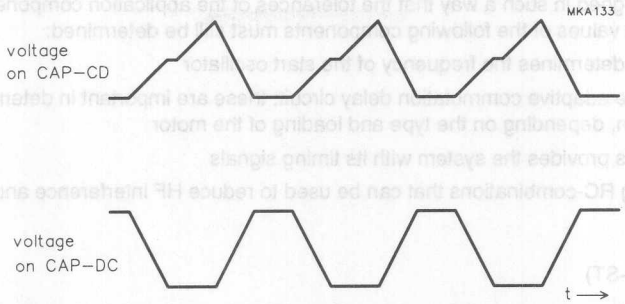


Fig.11 CAP-CD and CAP-DC voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 μA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 μA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 μA. The watchdog time is the time taken to charge the capacitor, with a current of 5 μA, from 0.3 to 2.2 V. The value of CAP-TI is given by:

$$C = 5 \times 10^{-6} \times t_m/1.9 = 2.63\, t_m \text{ (C in nF; t in ms)}$$

Example: If after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 20 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$$C = 2.63 \times 3.5 = 9.2 \text{ (choose 10 nF)}$$

Typical voltage waveforms are illustrated by Fig.12.

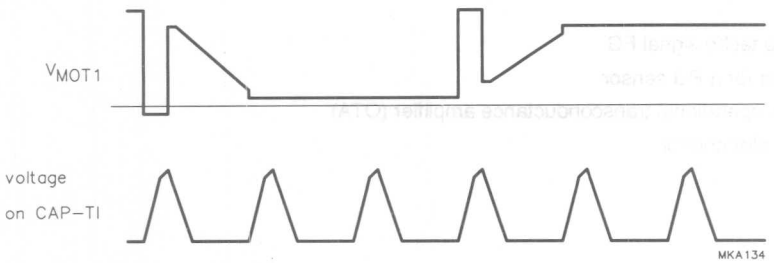


Fig.12 Typical CAP-TI and VMOT1 voltage waveforms in normal running mode.

Note to Fig.12

If the chosen value of CAP-TI is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

THE EXTERNAL DAMPING COMPONENTS

Flyback pulses from the motor windings may cause HF interference and acoustic noise. The flyback pulses can be damped by RC-combinations in parallel with the motor windings. This reduces the HF interference; it also reduces the acoustic noise by several dB, depending on the motor construction.

These damping components also have negative effects. They not only dissipate energy from the flyback pulses, but also contribute to the overall energy consumption. Other negative effects are discussed below.

One negative effect is the distortion of the motor EMF sensed by the comparators in the TDA5141. This distortion may influence the correct functioning of the TDA5141, for example, an (damped) oscillation occurring after the winding has been switched off. This oscillation must be critically (or over critically) damped, so that:

$R^2 \times C = 4 \times L$ (L = inductance of one coil, R and C for damping)

A second requirement is that the effect of the damping components must be negligible by the time that the zero-crossing of the EMF is expected. This is because the remainder of the step (due to RC components) causes shifting of the zero-crossing. For a critically damped combination the voltage can be calculated as a negative exponential with $\omega_o \times t$.

Example: Commutation frequency = 900 Hz, so t = 1100 µs, the time taken from the end of the diode pulse to the zero-crossing of the EMF will be approximately t = 440 µs. If a damping voltage from 9 V to 3 mV is required, then the reduction is 3000-fold, or e exp–8 = e exp $-\omega_o \times t$. This gives ω_o = 18180 rad/s. With L = 3 mH, C is found to be 1.01 µF (use 1 µF) and R is found to be 109.1 Ω (use 100 Ω).

A motor voltage of 7 V (peak-to-peak) at 150 Hz gives 3300 V/s, thus a 3 mV remainder shifts the zero-crossing 1 µs. Eddy currents will also contribue to this phase shift. A shift of 20 µs corresponds with 0.18 degrees (mechanically) for a 1500 rpm motor, or 0.1 mm on a VHS scanner drum.

OTHER DESIGN ASPECTS

There are other design aspects concerning the application of the TDA5141 besides the commutation function. They are:

- Generation of the tacho signal FG
- A built-in interface for a PG sensor
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability

FG SIGNAL

The FG signal is generated in the TDA5141 by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing (except for PG). The negative-going edges are called FG pulses because they generate an interrupt in a controlling microprocessor.

The accuracy of the FG output signal (jitter) is very good. This accuracy depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: A three phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 450 Hz.

PG SIGNAL

The accuracy of the PG signal in applications such as VCR must be high (phase information). This accuracy is obtained by combining the accurate FG signal with the PG signal by using a wide tolerance external PG sensor. The external PG signal (PG IN) is only used as an indicator to select a particular FG pulse. This pulse differs from the other FG pulses in that a short LOW-time of 15 µs after a HIGH-to-LOW transition. All other FG pulses have a 50% duty factor (see Fig.13).

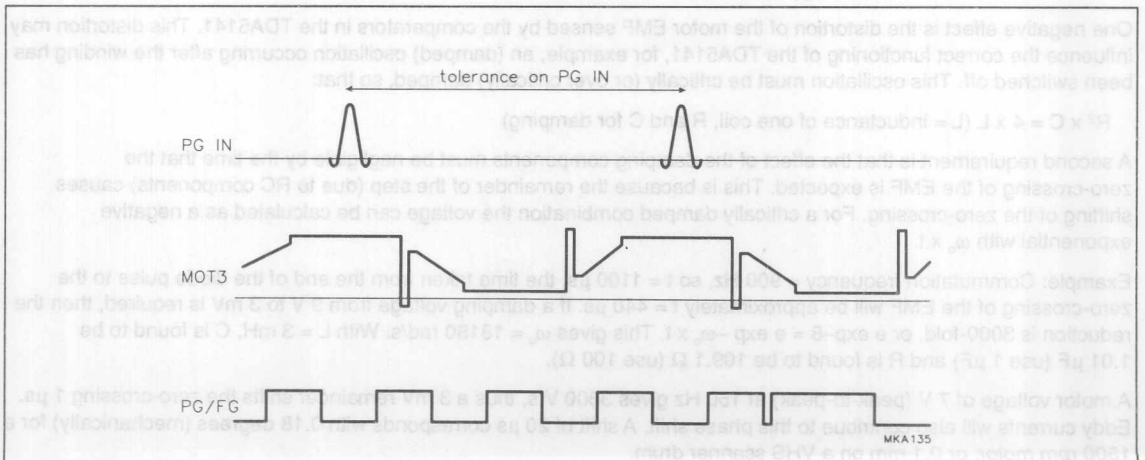


Fig.13 Timing and the FG and PGIN signals.

The special PG pulse is derived from the negative-going zero-crossing from the MOT3 output (pin 16). The external PG signal (PG IN on pin 5) must sense a positive going (>80 mV) within 1.5 to 7.5 commutation periods before the negative-going zero-crossing in MOT3 (see Fig.13).

The voltage requirements of the PG IN input are shut that a cheap pick-up coil can be used as a sensor (see Fig.14).

Example: If p = 6, then one revolution contains 6 x 6 = 36 commutations. The tolerance is 6 periods, that is 60 degrees (mechanically) or 6.67 ms at 1500 rpm.

If a PG sensor is not used, the PG IN input must be grounded, this will result in a 50% duty factor FG signal.

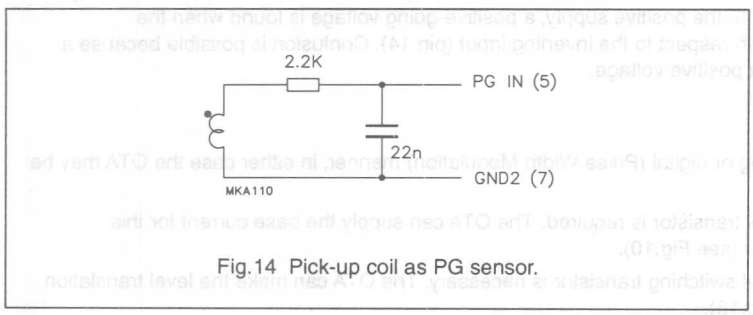


Fig.14 Pick-up coil as PG sensor.

The Operational Transconductance Amplifier (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier or as a level converter in a Switched Mode Power Supply (SMPS). The common mode input range includes ground (GND) and rises to V_P – 1.7 V. The high sinking current enables the OTA to drive a power transistor directly in an analog control amplifier or in a SMPS drive.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (pin 15) to the positive supply, a positive-going voltage is found when the non-inverting input (pin 13) is positive with respect to the inverting input (pin 14). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

Motor Control

DC motors can be controlled in an analog or digital (Pulse Width Modulation) manner, in either case the OTA may be used as follows:

- With analog control an external control transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.10).
- With digital or PWM control an external switching transistor is necessary. The OTA can make the level translation and drive the power transistor (see Fig.15).

A further aspect of motor control is current or voltage control; the TDA5141 is intended for voltage control applications. Both ground pins (7 and 18) must be connected externally. However the current from pin 7 can be considered as small and constant with respect to the current in the output stages. A resistor connected between pins 7, 18 and ground can be used for current control. Care must be taken that the voltage on pins 7, 18 does not disturb the (digital) FGPG signal too much (this signal is added to the digital signal).

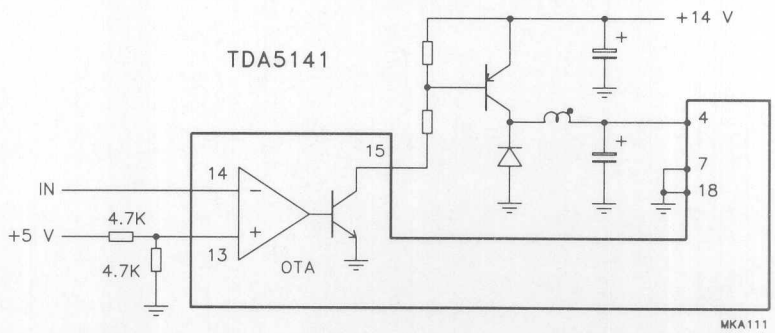


Fig.15 PWM drive of the output stages, OTA used as level converter.

An alternative method of voltage control is to increase the output impedance for a certain frequency, such as the commutation frequency; the circuit illustrated by Fig.10 uses this method. The low output impedance increases to approximately 10 Ω at 900 Hz. This circuit diagram is an example of the application of the TDA5141 with a VTR scanner for a PAL recorder running at 1500 rpm. The input signal is a PWM 5 V signal. The FGPG signal is read by a microprocessor that runs the servo control program.

A final aspect of motor control is braking; decreasing the speed to zero. No provisions have been made for this function. However, the generated voltage of the motor is rectified by the flyback diodes. If the voltage is loaded by a current drain on pin 5 then the motor will generate a braking torque that is proportional to the current.

Reliability

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection of the six output transistors is achieved by each transistor having a thermal sensor that is active when the transistor is switched on. The transistors are switched off when the local temperature becomes too high.

It is possible, that when braking (see previous section), the motor voltage (via the flyback diodes and the impedance on pin 5) may cause higher currents than allowed (>0.6 A). These currents must be limited externally.

Brushless DC motor drive circuit TDA5142T

FEATURES

- Full-wave commutation without position sensors
- Built-in start-up circuitry
- Six outputs that can drive three external transistor pairs:
  - 0.15 A output current
  - low saturation voltage
  - built-in current limiter
- Thermal protection
- Tacho output without extra sensor
- Transconductance amplifier for an external control transistor
- Motor brake facility

APPLICATIONS

- General purpose spindle driver (e.g. HDD, fan motor)

DESCRIPTION

The TDA5142T is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for power-drum motors (hard disk drives, tape drives, fan motors).

QUICK REFERENCE DATA

Measured over full voltage and temperature range

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range; note 1	4	–	18	V
I_P	supply current range; note 2	–	4.9	6.25	mA
V_{VMOT}	input voltage to the output driver stages	3	–	18	V
V_O	driver output voltage range;				
	I_O = 0 mA	0.2	–	–	V
	OUT-NA, NB, NC	–	–	V_{VMOT}	V
	OUT-PA, PB, PC	0.2	–	– 0.9	V
				–	

Notes to the quick reference data

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; all other inputs at 0 V; all outputs at V_P and I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5142T	24	SOL	plastic	SOT137A

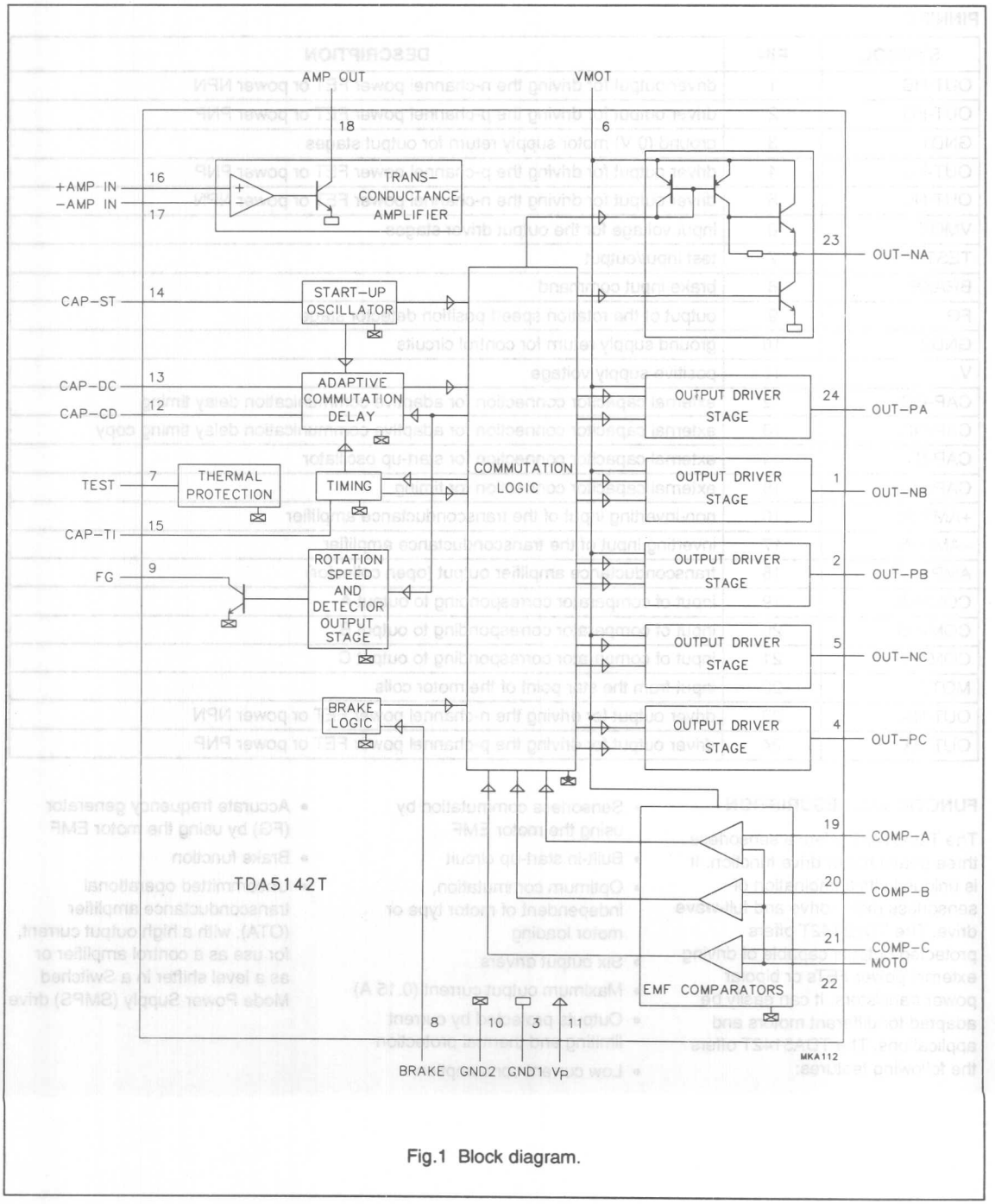


Fig.1 Block diagram.

Brushless DC motor drive circuit TDA5142T

PINNING

SYMBOL	PIN	DESCRIPTION
OUT-NB	1	driver output for driving the n-channel power FET or power NPN
OUT-PB	2	driver output for driving the p-channel power FET or power PNP
GND1	3	ground (0 V) motor supply return for output stages
OUT-PC	4	driver output for driving the p-channel power FET or power PNP
OUT-NC	5	driver output for driving the n-channel power FET or power NPN
VMOT	6	input voltage for the output driver stages
TEST	7	test input/output
BRAKE	8	brake input command
FG	9	output of the rotation speed position detector stage
GND2	10	ground supply return for control circuits
V_P	11	positive supply voltage
CAP-CD	12	external capacitor connection for adaptive communication delay timing
CAP-DC	13	external capacitor connection for adaptive communication delay timing copy
CAP-ST	14	external capacitor connection for start-up oscillator
CAP-TI	15	external capacitor connection for timing
+AMP IN	16	non-inverting input of the transconductance amplifier
–AMP IN	17	inverting input of the transconductance amplifier
AMP OUT	18	transconductance amplifier output (open collector)
COMP-A	19	input of comparator corresponding to output A
COMP-B	20	input of comparator corresponding to output B
COMP-C	21	input of comparator corresponding to output C
MOT0	22	input from the star point of the motor coils
OUT-NA	23	driver output for driving the n-channel power FET or power NPN
OUT-PA	24	driver output for driving the p-channel power FET or power PNP

FUNCTIONAL DESCRIPTION

The TDA5142T offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5142T offers protected outputs capable of driving external power FETs or bipolar power transistors. It can easily be adapted for different motors and applications. The TDA5142T offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Six output drivers
- Maximum output current (0.15 A)
- Outputs protected by current limiting and thermal protection
- Low current consumption
- Accurate frequency generator (FG) by using the motor EMF
- Brake function
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive

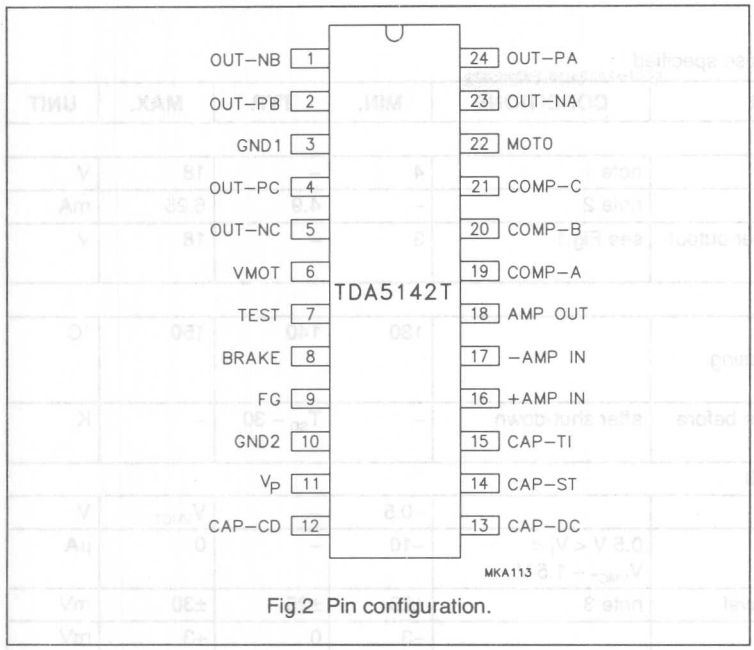


Fig.2 Pin configuration.

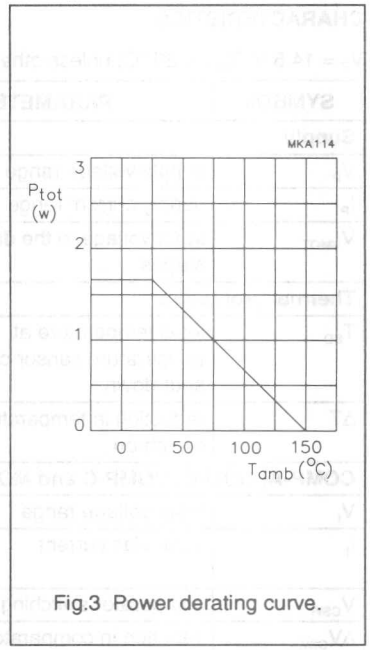


Fig.3 Power derating curve.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	4	18	V
V_I	input voltage; all pins except VMOT: $V_I < 18$ V	–0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage	3	18	V
V_O	output voltage FG AMP OUT	 GND –	 V_P 18	 V V
V_O	output voltage OUT-NA, NB, NC OUT-PA, PB, PC	 – 0.2	 $V_{VMOT} - 0.9$ –	 V V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC	–	2.5	V
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
P_{tot}	total power dissipation	–	see Fig. 3	
V_{es}	electrostatic voltage; see also handling	–	500	V

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 2. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses – on each pin referenced to ground.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range	note 1	4	–	18	V
I_P	supply current range	note 2	–	4.9	6.25	mA
V_{VMOT}	input voltage to the driver output stages	see Fig.1	3	–	18	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
COMP-A, COM-B, COMP-C and MOT0						
V_I	input voltage range		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	0	µA
V_{CSW}	comparator switching level	note 3	±20	±25	±30	mV
ΔV_{CSW}	variation in comparator switching levels		–3	0	+3	mV
V_H	comparator input hysteresis		–	75	–	µV
OUT-N(A,B,C) and OUT-P(A,B,C)						
V_{OH-N}	driver output voltage range; n-channel, upper transistor	I_O = –100 mA	–1.2	–	–	V
V_{OL-N}	driver output voltage range; n-channel, lower transistor	I_O = 10 mA	–	–	0.45	V
V_{OH-P}	driver output voltage range; p-channel, upper transistor	I_O = –10 mA	–1.2	–	–	V
V_{OL-P}	driver output voltage range; p-channel, lower transistor	I_O = 100 mA	–	–	0.45	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA	–	–	180	mV
I_{LIM}	current limiting	lower transistor; V_{CE} = 6 V	–	150	–	mA
VMOT						
V_{VMOT}	input voltage range		3	–	18	V

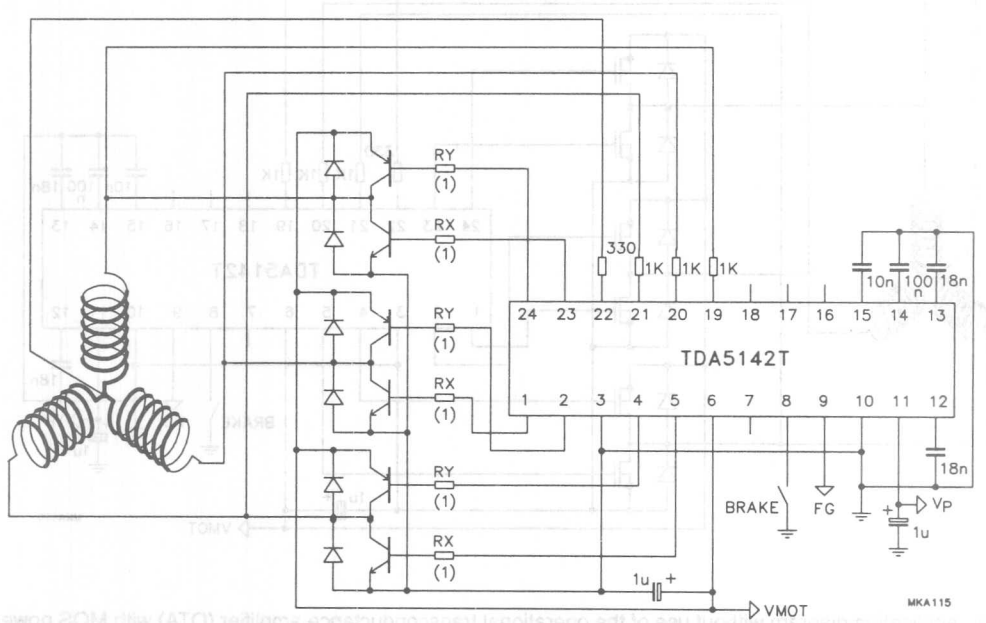
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
+AMP IN and -AMP IN						
V_{IAMP}	input voltage range		−0.3	–	$V_P - 1.7$	V
V_{IAMP}	differential mode voltage without 'latch-up'		–	–	$\pm V_P$	V
I_B	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{OFFSET}	input offset voltage		–	–	10	mV
AMP OUT						
I_I	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_{Omax}	maximum output voltage		–	–	18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	40	–	–	mA/μs
G_{tr}	transfer gain		0.3	–	–	S
BRAKE						
V_{BM}	break-mode voltage at pin 8	$4 < V_P < 18$ V	–	–	2.3	V
V_{DBM}	disable break-mode voltage	$4 < V_P < 18$ V	2.7	–	–	V
I_{BC}	brake current at pin 8		–	−20	30	μA
I_{NM}	normal-mode current at pin 8		–	0	–	μA
FG						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
V_{OHmax}	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	μs
	ratio of FG frequency and commutation frequency		–	1	–	
δ	duty factor		–	50	–	%
CAP-ST						
I_I	output sink current		1.5	2.0	2.5	μA
I_O	output source current		−2.5	−2.0	−1.5	μA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_I	output sink current		–	28	–	μA
I_{OH}	HIGH level output source current		–	−57	–	μA
I_{OL}	LOW level output source current		–	−5	–	μA
V_{SWL}	LOW level switching voltage		–	0.2	–	V
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CAP-CD						
I_I	ouput sink current		10.6	16.2	22	µA
I_O	output source current		−5.3	−8.1	−11	µA
I_I/I_O	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		–	875	–	mV
V_{IH}	HIGH level input voltage		2.3	–	2.5	V
CAP-DC						
I_I	output sink current		10.1	15.5	20.9	µA
I_O	output source current		−20.9	−15.5	−10.1	µA
I_I/I_O	ratio of sink to source current		0.9	1.025	1.15	

Notes to the characteristics

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P and $I_O = 0$ mA.
3. Switching levels with respect to driver outputs OUT-NA, NB, NC and OUT-PA, PB, PC.

APPLICATION INFORMATION



(1) RX = RY > 8 (VMOT – 1.5)

Fig.4 Application diagram without use of the operational transconductance amplifier (OTA) with bipolar power transistors.

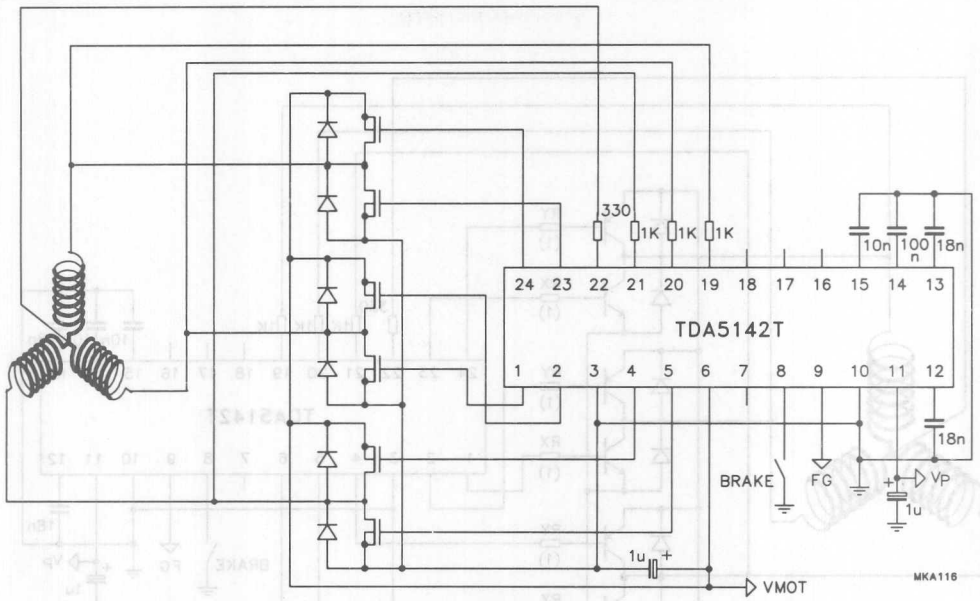


Fig.5 Application diagram without use of the operational transconductance amplifier (OTA) with MOS power transistors.

Introduction (see Fig.6)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

The driver output stages are also protected by a current limiting circuit and by thermal protection.

The zero-crossings can be used to provide speed information such as the tacho signal FG.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5142T also contains an uncommitted transconductance amplifier (OTA) that can be used as a control amplifier. The output is capable of directly driving an external power transistor.

The TDA5142T is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented).

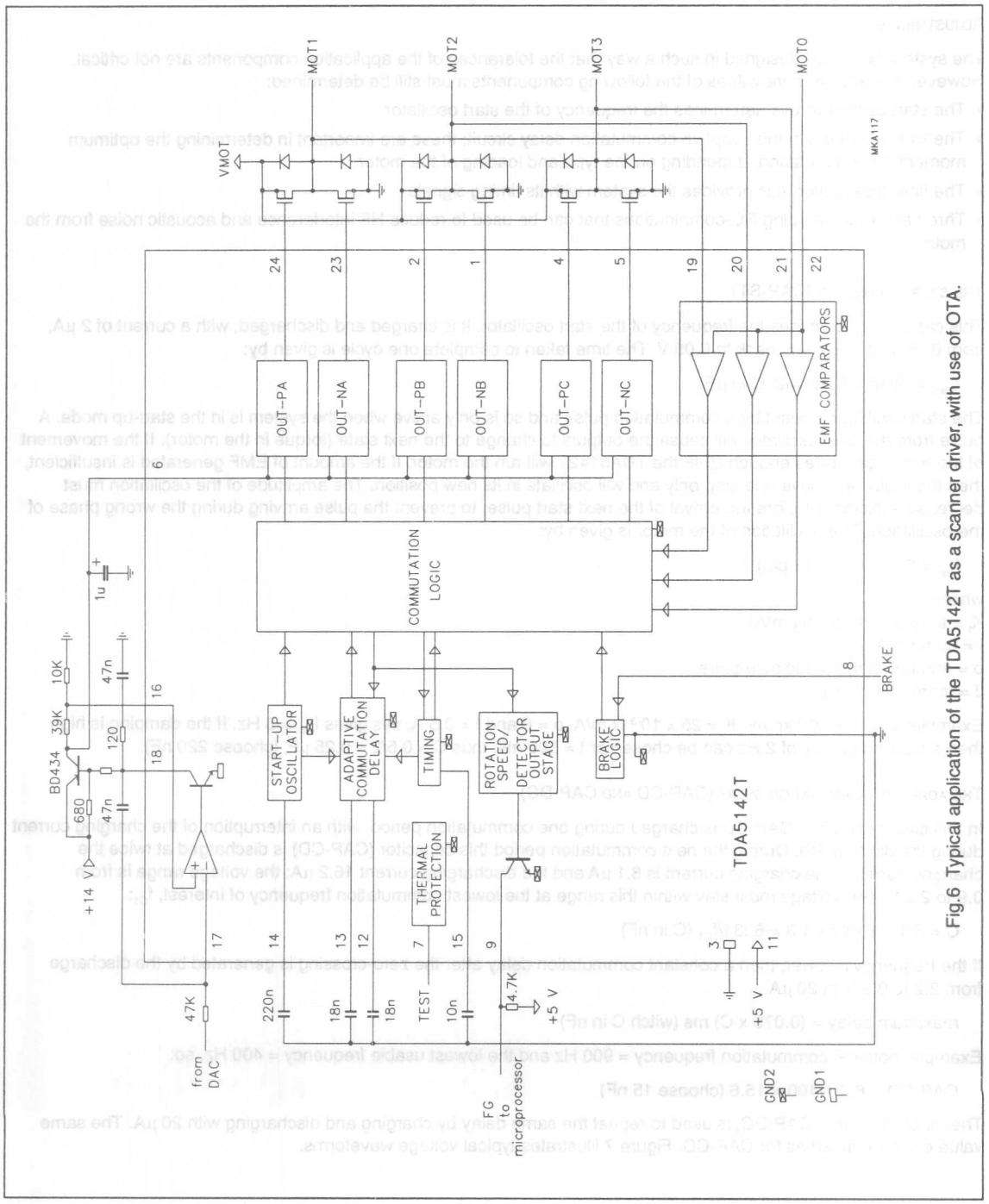


Fig.6 Typical application of the TDA5142T as a scanner driver, with use of OTA.

ADJUSTMENTS

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals
- Three external, damping RC-combinations that can be used to reduce HF interference and acoustic noise from the motor

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 µA, from 0.05 V to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

$$t_{start} = (2.15 \times C)\ s \text{ (with C in } \mu F)$$

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5142T will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$$f_{osc} = 0.5/\pi \times (K_t \times I \times p/J)^{1/2}$$

where:
K_t = torque constant (N.m/A)
I = current (A)
p = number of magnetic pole-pairs
J = inertia J ($kg.m^2$)

Example: $J = 72 \times 10^{-6}$ $kg.m^2$, $K = 25 \times 10^{-3}$ N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 µF, (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 µA and the discharging current 16.2 µA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

$$C = 8.1 \times 10^{-6}/\ f \times 1.3 = 6231/f_{C1} \text{ (C in nF)}$$

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 20 µA.

$$\text{maximum delay} = (0.076 \times C)\ ms \text{ (witch C in nF)}$$

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

$$CAP\text{-}CD = 6231/400 = 15.6 \text{ (choose 15 nF)}$$

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 20 µA. The same value can be chosen as for CAP-CD. Figure 7 illustrates typical voltage waveforms.

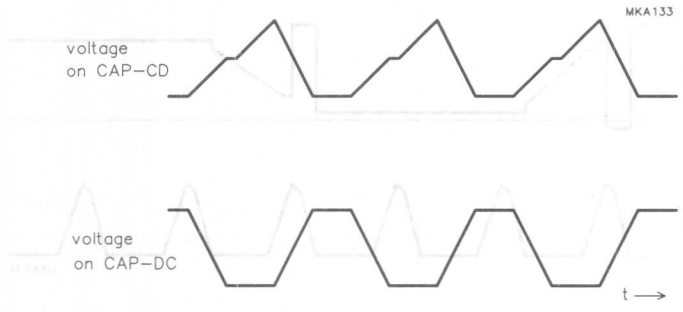


Fig.7 CAP-CD and CAP-DC voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 µA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 µA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 µA. The watchdog time is the time taken to charge the capacitor, with a current of 5 µA, from 0.3 to 2.2 V. The value of CAP-TI is given by:

$C = 5 \times 10^{-6} \times t_m/1.9 = 2.63\ t_m$ (C in nF; t in ms)

Example: If after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 20 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$C = 2.63 \times 3.5 = 9.2$ (choose 10 nF)

Typical voltage waveforms are illustrated by Fig.8.

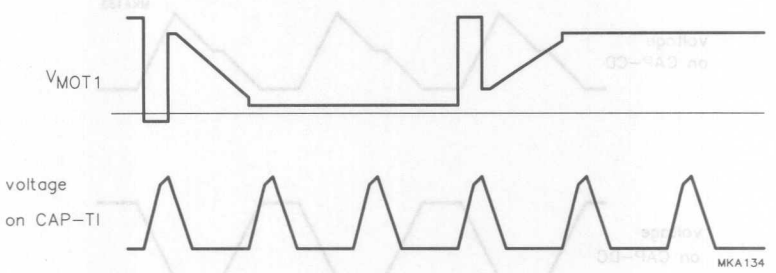


Fig.8 Typical CAP-TI and VMOT1 voltage waveforms in normal running mode.

Note to Fig.8

If the chosen value of CAP-TI is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

THE EXTERNAL DAMPING COMPONENTS

Flyback pulses from the motor windings may cause HF interference and acoustic noise. The flyback pulses can be damped by RC-combinations in parallel with the motor windings. This reduces the HF interference; it also reduces the acoustic noise by several dB, depending on the motor construction.

These damping components also have negative effects. They not only dissipate energy from the flyback pulses, but also contribute to the overall energy consumption. Other negative effects are discussed below.

One negative effect is the distortion of the motor EMF sensed by the comparators in the TDA5142T. This distortion may influence the correct functioning of the TDA5142T, for example, an (damped) oscillation occurring after the winding has been switched off. This oscillation must be critically (or over critically) damped, so that:

$R^2 \times C = 4 \times L$ (L = inductance of one coil, R and C for damping)

A second requirement is that the effect of the damping components must be negligible by the time that the zero-crossing of the EMF is expected. This is because the remainder of the step (due to RC components) causes shifting of the zero-crossing. For a critically damped combination the voltage can be calculated as a negative exponential with $\omega_o \times t$.

Example: Commutation frequency = 900 Hz, so t = 1100 µs, the time taken from the end of the diode pulse to the zero-crossing of the EMF will be approximately t = 440 µs. If a damping voltage from 9 V to 3 mV is required, then the reduction is 3000-fold, or e exp−8 = e exp $-\omega_o \times t$. This gives ω_o = 18180 rad/s. With L = 3 mH, C is found to be 1.01 µF (use 1 µF) and R is found to be 109.1 Ω (use 100 Ω).

A motor voltage of 7 V (peak-to-peak) at 150 Hz gives 3300 V/s, thus a 3 mV remainder shifts the zero-crossing 1 µs. Eddy currents will also contribue to this phase shift. A shift of 20 µs corresponds with 0.18 degrees (mechanically) for a 1500 rpm motor, or 0.1 mm on a VHS scanner drum.

OTHER DESIGN ASPECTS

There are other design aspects concerning the application of the TDA5142T besides the commutation function. They are:

- Generation of the tacho signal FG
- General purpose operational transconductance amplifier (OTA)
- Possibilities of motor control
- Reliability

FG SIGNAL

The FG signal is generated in the TDA5142T by using the zero-crossing of the motor EMF from the three motor windings and the commutation signal.

Output FG switches from HIGH-to-LOW on all zero crossings and from LOW-to-HIGH on all commutations. Output FG can source typically 75 μA and sink more than 3 mA.

Example: A three phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 900 Hz.

The Operational Transconductance Amplifier (OTA)

The OTA is an uncommitted amplifier with a high output current (40 mA) that can be used as a control amplifier or as a level converter in a Switched Mode Power Supply (SMPS). The common mode input range includes ground (GND) and rises to V_P – 1.7 V. The high sinking current enables the OTA to drive a power transistor directly in an analog control amplifier or in a SMPS drive.

Although the gain is not extremely high (0.3 S), care must be taken with the stability of the circuit if the OTA is used as a linear amplifier as no frequency compensation has been provided.

The convention for the inputs (inverting or not) is the same as for a normal operational amplifier: with a resistor (as load) connected from the output (pin 18) to the positive supply, a positive-going voltage is found when the non-inverting input (pin 16) is positive with respect to the inverting input (pin 17). Confusion is possible because a 'plus' input causes less current, and so a positive voltage.

Motor Control

DC motors can be controlled in an analog or digital (Pulse Width Modulation) manner, in either case the OTA may be used as follows:

- With analog control an external control transistor is required. The OTA can supply the base current for this transistor and act as a control amplifier (see Fig.6).
- With digital or PWM control an external switching transistor is necessary. The OTA can make the level translation and drive the power transistor (see Fig.9).

A further aspect of motor control is current or voltage control; the TDA5142T is intended for voltage control applications. Both ground pins (3 and 10) must be connected externally. However the current from pin 10 can be considered as small and constant with respect to the current in the output stages. A resistor connected between pins 3, 10 and ground can be used for current control. Care must be taken that the voltage on pins 3, 10 does not disturb the (digital) FG signal too much (this signal is added to the digital signal).

An alternative method of voltage control is to increase the output impedance for a certain frequency, such as the commutation frequency; the circuit illustrated by Fig.6 uses this method. The low output impedance increases to approximately 10 Ω at 900 Hz. This circuit diagram is an example of the application of the TDA5142T with a VTR scanner for a PAL recorder running at 1500 rpm. The input signal is a PWM 5 V signal. The FG signal is read by a microprocessor that runs the servo control program.

A final aspect of motor control is braking; decreasing the speed to zero. No provisions have been made for this function:

- If the voltage on pin 8 is less than 2.3 V the motor brakes.
- If pin 8 is floating or if the voltage on pin 8 is greater than 2.7 V the motor runs normally.

Reliability

It is necessary to protect high current circuits and the output stages are protected in two ways:

- Current limiting of the 'lower' output transistors. The 'upper' output transistors use the same base current as the conducting 'lower' transistor (+15%). This means that the current to and from the output stages is limited.
- Thermal protection is achived:
  the transistors are switched off when the local temperature becomes too high.

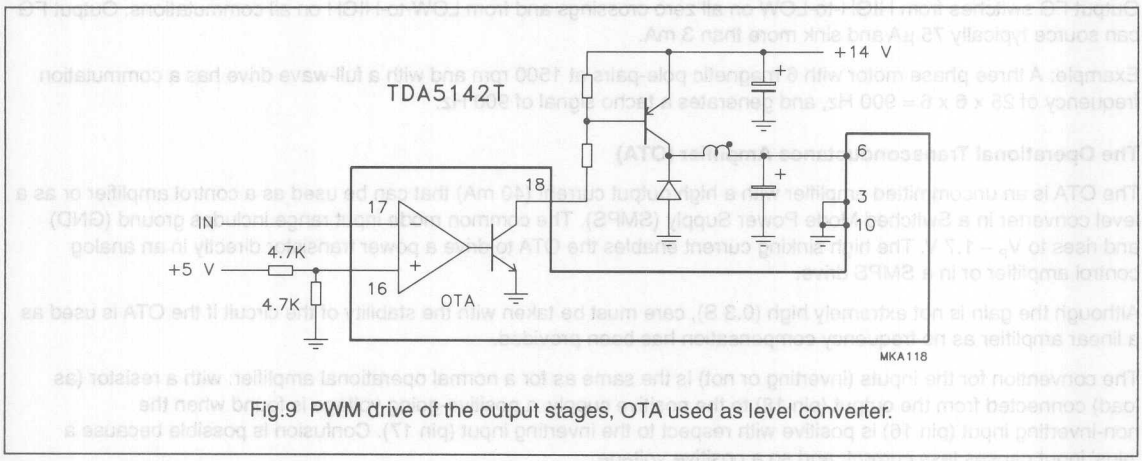


Fig.9 PWM drive of the output stages, OTA used as level converter.

Brushless DC motor drive circuit TDA5145

FEATURES

- Full-wave commutation (using push/pull drivers at the output stages) without position sensors
- Built-in start-up circuitry
- Three push-pull outputs:
  - 1.8 A output current
  - built-in current limiter
- Thermal protection
- Soft-switching outputs
- Flyback diodes
- Tacho output without extra sensor
- Motor brake facility
- Direction control input
- Reset function
- Transconductance amplifier for an external control transistor

APPLICATIONS

- General purpose spindle driver (e.g.HDD, tape drives)

DESCRIPTION

The TDA5145 is a bipolar integrated circuit used to drive brushless DC motors in full-wave mode. The device senses the rotor position using an EMF-sensing technique and is ideally suited as a drive circuit for a hard disk drive motor or tape driver.

QUICK REFERENCE DATA

Measured over full voltage and temperature range

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range; note 1	4	–	18	V
I_P	supply current range; note 2	–	4.9	6.8	mA
V_{VMOT}	input voltage to the output driver stages	1.7	–	16	V
V_O	driver output voltage range; I_O = 0 mA	0.2	–	V_{VMOT} – 0.9	V
I_{LIM}	current limiting	1.45	1.75	2	A

Notes to the quick reference data

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$; +AMP IN and –AMP IN at 0 V; all outputs I_O = 0 mA.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA5145	28	DIL	plastic	SOT117AG

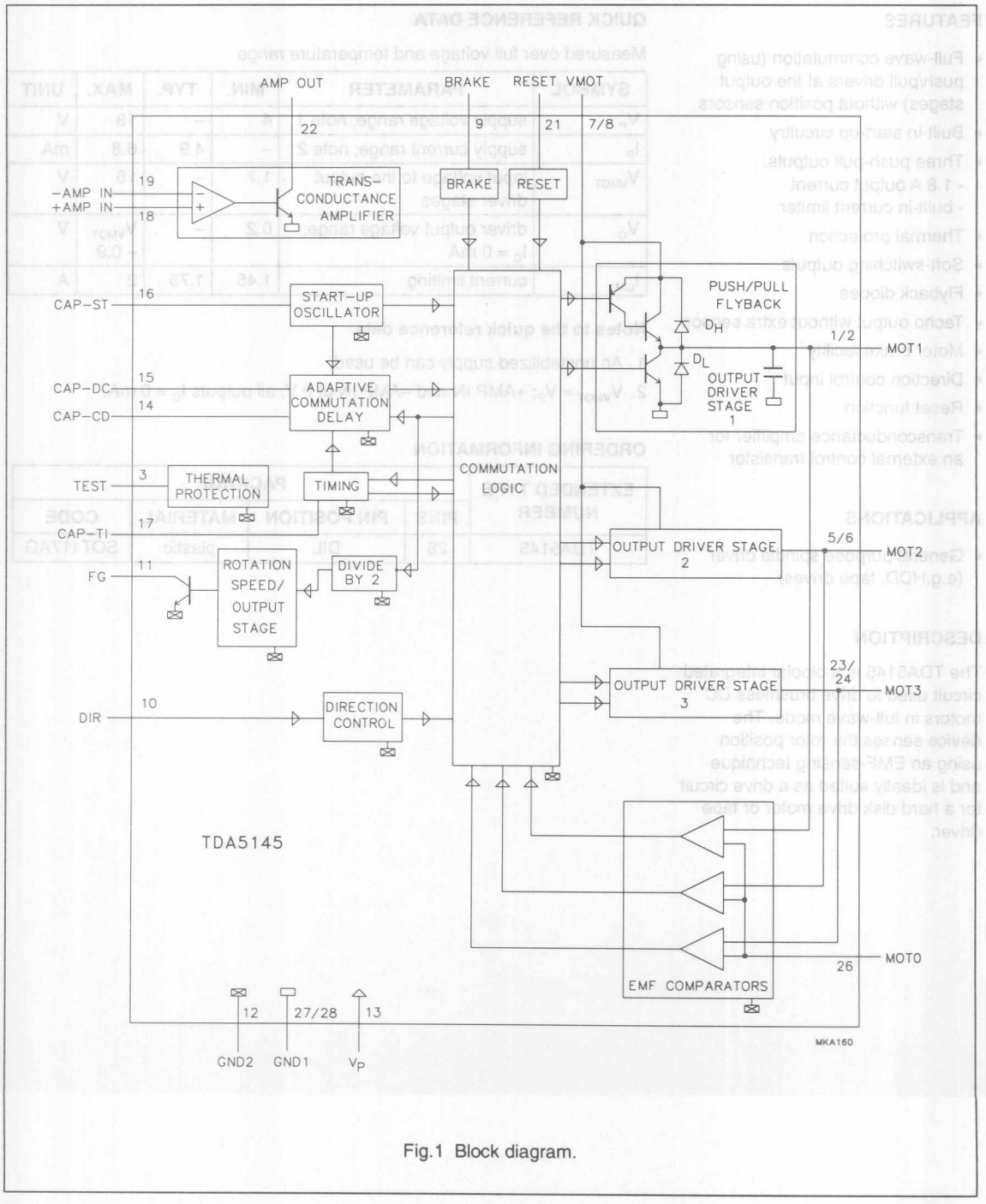


Fig.1 Block diagram.

Brushless DC motor drive circuit TDA5145

PINNING

SYMBOL	PIN	DESCRIPTION
MOT1	1, 2	driver output 1
TEST	3	test input/output
n.c.	4	not connected
MOT2	5, 6	driver output 2
VMOT	7, 8	input voltage for the output driver stages
BRAKE	9	brake input
DIR	10	direction control input
FG	11	frequency generator: output of the rotation speed and position detector stages (open collector digital output, negative-going edge is valid)
GND2	12	ground supply return for control circuits
V_P	13	positive supply voltage
CAP-CD	14	external capacitor connection for adaptive communication delay timing
CAP-DC	15	external capacitor connection for adaptive communication delay timing copy
CAP-ST	16	external capacitor connection for start-up oscillator
CAP-TI	17	external capacitor connection for timing
+AMP IN	18	non-inverting input of the transconductance amplifier
–AMP IN	19	inverting input of the transconductance amplifier
n.c.	20	not connected
RESET	21	reset input
AMP OUT	22	transconductance amplifier output (open collector)
MOT3	23, 24	driver output 3
n.c.	25	not connected
MOT0	26	input from the star point of the motor coils
GND1	27, 28	ground (0 V) motor supply return for output stages

FUNCTIONAL DESCRIPTION

The TDA5145 offers a sensorless three phase motor drive function. It is unique in its combination of sensorless motor drive and full-wave drive. The TDA5145 offers protected outputs capable of handling high currents and can be used with star or delta connected motors. It can easily be adapted for different motors and applications. The TDA5145 offers the following features:

- Sensorless commutation by using the motor EMF
- Built-in start-up circuit
- Optimum commutation, independent of motor type or motor loading
- Built-in flyback diodes
- Three phase full-wave drive
- High output current (1.8 A)
- Outputs protected by current limiting and thermal protection of each output transistor
- Low current consumption by adaptive base-drive
- Soft-switching pulse output for low radiation
- Accurate frequency generator (FG) by using the motor EMF
- Direction of rotation controlled by one pin
- Uncommitted operational transconductance amplifier (OTA), with a high output current, for use as a control amplifier or as a level shifter in a Switched Mode Power Supply (SMPS) drive
- Brake function

Brushless DC motor drive circuit TDA5145

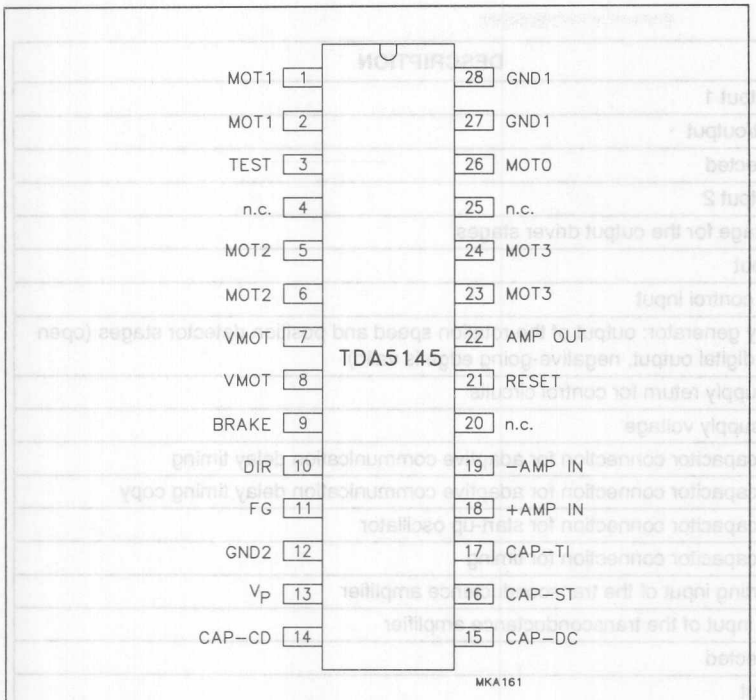


Fig.2 Pin configuration.

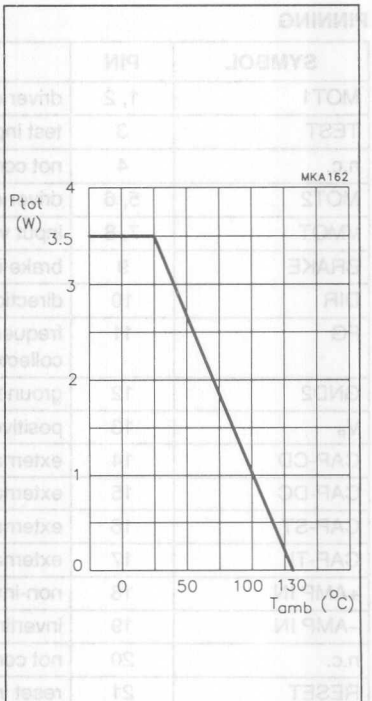


Fig.3 Power derating curve.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	positive supply voltage	–	18	V
V_I	input voltage; all pins except VMOT: $V_I < 18$ V	−0.3	$V_P + 0.5$	V
V_{VMOT}	VMOT input voltage	−0.5	17	V
V_O	output voltage AMP OUT and FG	GND	V_P	V
V_O	output voltage MOT0, MOT1, MOT2 and MOT3	−1	$V_{VMOT} + V_D$	V
V_I	input voltage CAP-ST, CAP-TI, CAP-CD and CAP-DC	–	2.5	V
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
P_{tot}	total power dissipation	–	see Fig. 3	
V_{es}	electrostatic voltage; see also handling	–	2000	V

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 2. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses + and 3 pulses – on each pin referenced to ground.

CHARACTERISTICS

V_P = 14.5 V; T_{amb} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range	note 1	4	–	18	V
I_P	supply current range	note 2	–	4.9	6.8	mA
V_{VMOT}	input voltage to the driver output stages	see Fig.1	1.7	–	16	V
Thermal protection						
T_{SD}	local temperature at temperature sensor causing shut-down		130	140	150	°C
ΔT	reduction in temperature before switch-on	after shut-down	–	T_{SD} – 30	–	K
MOT0 - centre tape						
V_I	input voltage range		–0.5	–	V_{VMOT}	V
I_I	input bias current	0.5 V < V_I < V_{VMOT} – 1.5 V	–10	–	–	µA
V_{CSW}	comparator switching level	note 3	±20	±25	±30	mV
ΔV_{CS}	variation in threshold voltage between comparators	note 3	–	–	3	mV
V_H	comparator input hysteresis		–	75	–	µV
MOT1, MOT2 and MOT3						
V_O	driver output voltage range	I_O = 100 mA	0.4	–	V_{VMOT} – 1.2	V
V_{DO}	drop-out voltage	I_O = 1000 mA	–	–	2	V
ΔV_{OL}	variation in saturation voltage between lower transistors	I_O = 100 mA	–	–	180	mV
ΔV_{OH}	variation in saturation voltage between upper transistors	I_O = –100 mA	–	–	180	mV
I_{LIM}	current limiting	lower transistor; V_{CE} = 6 V	1.45	1.75	2	A
t_{tr}	transition time switching output	V_{VMOT} = 14.5 V; see Fig.5	5	9	15	µs
V_{DHF}	diode forward voltage (diode D_H)	I_O = –500 mA; notes 4 and 5; see Fig.1	–	–	1.5	V
V_{DLF}	diode forward voltage (diode D_L)	I_O = 500 mA; notes 4 and 5; see Fig.1	–1.5	–	–	V
I_{DM}	peak diode current	note 5	–	–	1	A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
+AMP IN and -AMP IN						
V_{IAMP}	input voltage range		−0.3	–	$V_P - 1.7$	V
V_{IAMP}	differential mode voltage without 'latch-up'		–	–	$\pm V_P$	V
I_B	input bias current		–	–	650	nA
C_I	input capacitance		–	4	–	pF
V_{OFFSET}	input offset voltage		–	–	10	mV
I_I	output sink current		40	–	–	mA
V_{sat}	saturation voltage	I_I = 40 mA	–	1.5	2.1	V
V_{Omax}	maximum output voltage		–	–	18	V
SR	slew rate	R_L = 330 Ω; C_L = 50 pF	–	60	–	mA/µs
G_{tr}	transfer gain		0.3	–	–	S
DIR						
V_{IH}	normal rotation voltage at pin 5; HIGH level	4 V < V_P < 18 V	2.0	–	–	V
V_{IL}	reverse rotation voltage at pin 5; LOW level	4 V < V_P < 18 V	–	–	0.8	V
I_{IL}	reverse rotation current; LOW level		–	−20	–	µA
I_{IH}	normal rotation current; HIGH level		–	−20	–	µA
RESET						
V_{IH}	HIGH level input voltage in reset mode	4 V < V_P < 18 V	2.0	–	–	V
V_{IL}	LOW level input voltage in normal mode	4 V < V_P < 18 V	–	–	0.8	V
I_{IL}	LOW level input current	V_I = 2.0 V	–	−20	–	µA
I_{IH}	HIGH level input current	V_I = 0.8 V	–	−20	–	µA
BRAKE						
V_{IH}	HIGH level input voltage in brake mode	4 V < V_P < 18 V	2.0	–	–	V
V_{IL}	LOW level input voltage in normal mode	4 V < V_P < 18 V	–	–	0.8	V
I_{IL}	LOW level input current	V_I = 2.0 V	–	−20	–	µA
I_{IH}	HIGH level input current	V_I = 0.8 V	–	−20	–	µA
FG						
V_{OL}	LOW level output voltage	I_O = 1.6 mA	–	–	0.4	V
V_{OHmax}	maximum HIGH level output voltage		V_P	–	–	V
t_{THL}	HIGH-to-LOW transition time	C_L = 50 pF; R_L = 10 kΩ	–	0.5	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FG						
	ratio of FG frequency and commutation frequency		–	1 : 2	–	
δ	duty factor		–	50	–	%
CAP-ST						
I_I	output sink current		1.5	2.0	2.5	µA
I_O	output source current		–2.5	–2.0	–1.5	µA
V_{SWL}	LOW level switching voltage		–	0.20	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-TI						
I_I	output sink current		–	28	–	µA
I_{OH}	HIGH level output source current		–	–57	–	µA
I_{OL}	LOW level output source current		–	–5	–	µA
V_{SWL}	LOW level switching voltage		–	50	–	mV
V_{SWM}	MIDDLE level switching voltage		–	0.30	–	V
V_{SWH}	HIGH level switching voltage		–	2.20	–	V
CAP-CD						
I_I	ouput sink current		10.6	16.2	22	µA
I_O	output source current		–5.3	–8.1	–11	µA
I_I/I_O	ratio of sink to source current		1.85	2.05	2.25	
V_{IL}	LOW level input voltage		0.85	–	0.9	V
V_{IH}	HIGH level input voltage		2.3	2.4	2.55	V
CAP-DC						
I_I	output sink current		10.1	15.5	20.9	µA
I_O	output source current		–20.9	–15.5	–10.1	µA
I_I/I_O	ratio of sink to source current		0.9	1.025	1.15	

Notes to the characteristics

1. An unstabilized supply can be used.
2. $V_{VMOT} = V_P$, all other inputs at 0 V; all outputs at V_P and $I_O = 0$ mA.
3. Switching levels with respect to MOT1, MOT2 and MOT3; see also Fig.4.
4. Drivers are in the high-impedance OFF-state.
5. The outputs are short-circuit protected by limiting the current and the IC temperature.

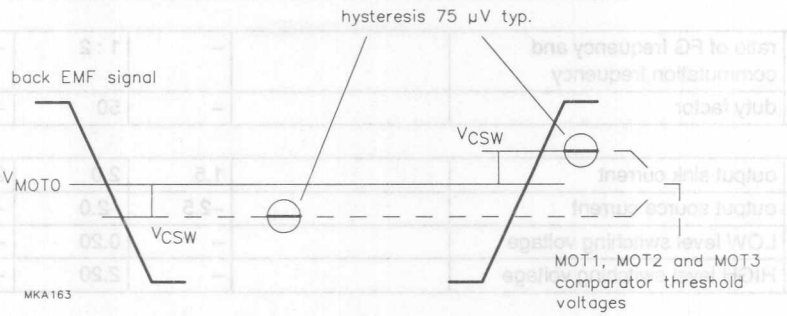


Fig.4 Switching levels with respect to MOT1, MOT2 and MOT3.

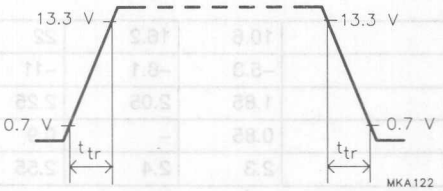
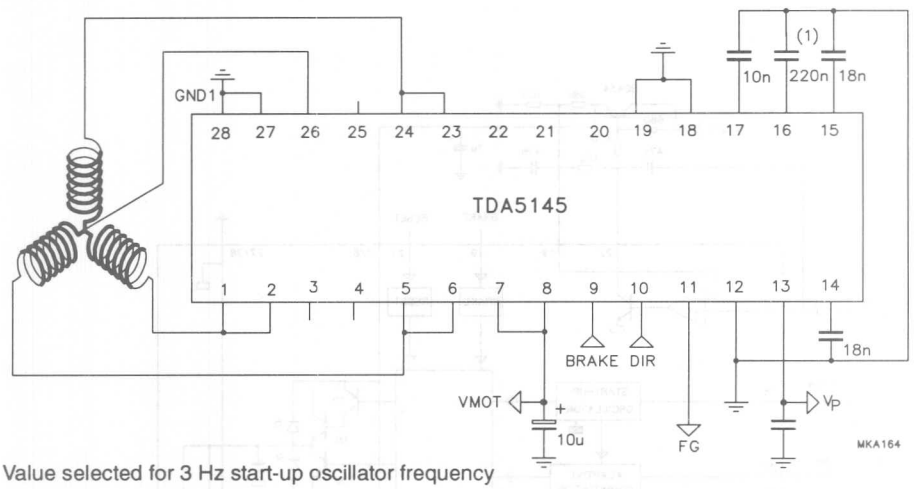


Fig.5 Output transition time measurement.

APPLICATION INFORMATION



(1) Value selected for 3 Hz start-up oscillator frequency

Fig.6 Application diagram without use of the operational transconductance amplifier (OTA).

Introduction (see Fig.7)

Full-wave driving of a three phase motor requires three push-pull output stages. In each of the six possible states two outputs are active, one sourcing and one sinking current. The third output presents a high impedance to the motor which enables measurement of the motor EMF in the corresponding motor coil by the EMF comparator at each output. The commutation logic is responsible for control of the output transistors and selection of the correct EMF comparator.

The zero-crossing in the motor EMF (detected by the comparator selected by the commutation logic) is used to calculate the correct moment for the next commutation, that is, the change to the next output state. The delay is calculated (depending on the motor loading) by the adaptive commutation delay block.

Because of high inductive loading the output stages contain flyback diodes. The output stages are also protected by a current limiting circuit and by thermal protection of the six output transistors.

The zero-crossings can be used to provide speed information such as the tacho signal FG.

The system will only function when the EMF voltage from the motor is present. Therefore, a start oscillator is provided that will generate commutation pulses when no zero-crossings in the motor voltage are available.

A timing function is incorporated into the device for internal timing and for timing of the reverse rotation detection.

The TDA5145 is designed for systems with low current consumption: use of I^2L logic, adaptive base drive for the output transistors (patented).

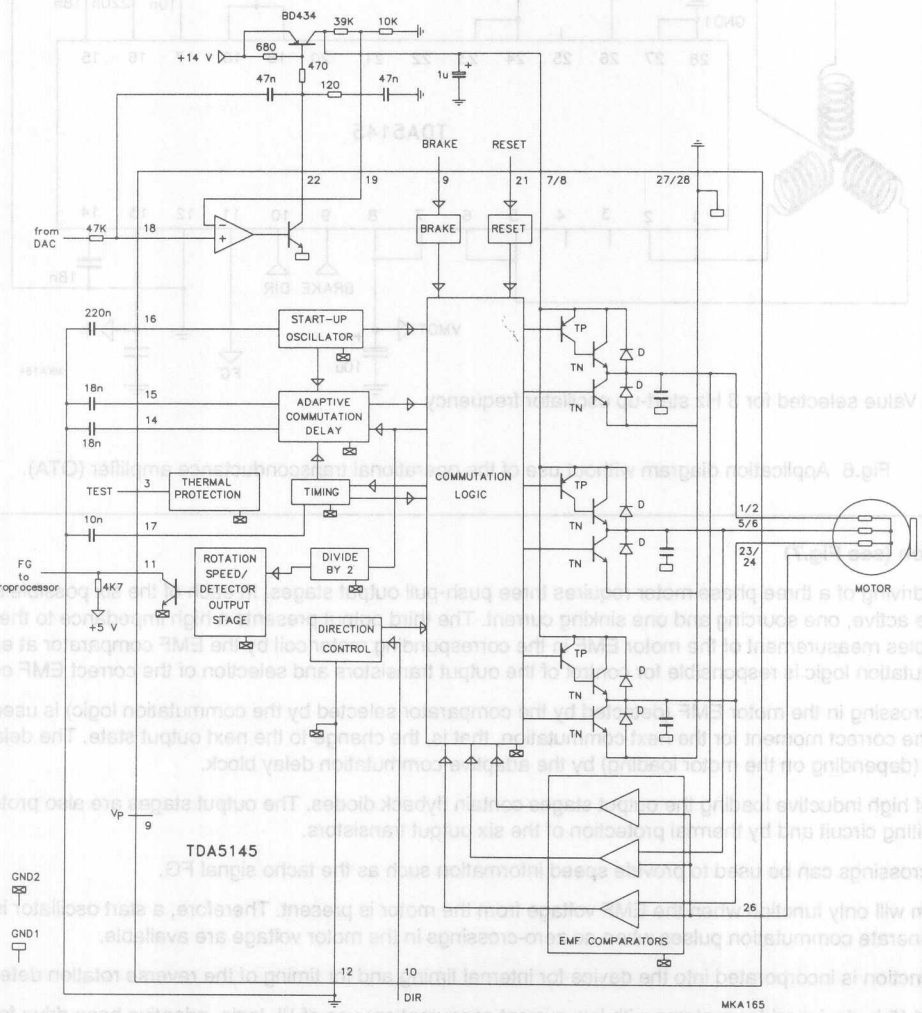


Fig.7 Typical application of the TDA5145 as a scanner driver, with use of OTA.

ADJUSTMENTS

The system has been designed in such a way that the tolerances of the application components are not critical. However, the approximate values of the following components must still be determined:

- The start capacitor; this determines the frequency of the start oscillator
- The two capacitors in the adaptive commutation delay circuit; these are important in determining the optimum moment for commutation, depending on the type and loading of the motor
- The timing capacitor; this provides the system with its timing signals
- Three external, damping RC-combinations that can be used to reduce HF interference and acoustic noise from the motor

THE START CAPACITOR (CAP-ST)

This capacitor determines the frequency of the start oscillator. It is charged and discharged, with a current of 2 μA, from 0.05 V to 2.2 V and back to 0.05 V. The time taken to complete one cycle is given by:

t_{start} = (2.15 x C) s (with C in μF)

The start oscillator is reset by a commutation pulse and so is only active when the system is in the start-up mode. A pulse from the start oscillator will cause the outputs to change to the next state (torque in the motor). If the movement of the motor generates enough EMF the TDA5145 will run the motor. If the amount of EMF generated is insufficient, then the motor will move one step only and will oscillate in its new position. The amplitude of the oscillation must decrease sufficiently before the arrival of the next start pulse, to prevent the pulse arriving during the wrong phase of the oscillation. The oscillation of the motor is given by:

$f_{osc} = 0.5/\pi \times (K_t \times I \times p/J)^{1/2}$

where:
K_t = torque constant (N.m/A)
I = current (A)
p = number of magnetic pole-pairs
J = inertia J (kg.m^2)

Example: J = 72 x 10^{-6} kg.m^2, K = 25 x 10^{-3} N.m/A, p = 6 and I = 0.5 A; this gives f_{osc} = 5 Hz. If the damping is high then a start frequency of 2 Hz can be chosen or t = 500 ms, thus C = 0.5/2 = 0.25 μF, (choose 220 nF).

THE ADAPTIVE COMMUTATION DELAY (CAP-CD AND CAP-DC)

In this circuit capacitor CAP-CD is charged during one commutation period, with an interruption of the charging current during the diode pulse. During the next commutation period this capacitor (CAP-CD) is discharged at twice the charging current. The charging current is 8.1 μA and the discharging current 16.2 μA; the voltage range is from 0.9 to 2.2 V. The voltage must stay within this range at the lowest commutation frequency of interest, f_{C1}:

C = 8.1 x 10^{-6}/ f x 1.3 = 6231/f_{C1} (C in nF)

If the frequency is lower, then a constant commutation delay after the zero-crossing is generated by the discharge from 2.2 to 0.9 V at 16.2 μA.

maximum delay = (0.076 x C) ms (witch C in nF)

Example: nominal commutation frequency = 900 Hz and the lowest usable frequency = 400 Hz, so:

CAP-CD = 6231/400 = 15.6 (choose 18 nF)

The other capacitor, CAP-DC, is used to repeat the same delay by charging and discharging with 20 μA. The same value can be chosen as for CAP-CD. Figure 8 illustrates typical voltage waveforms.

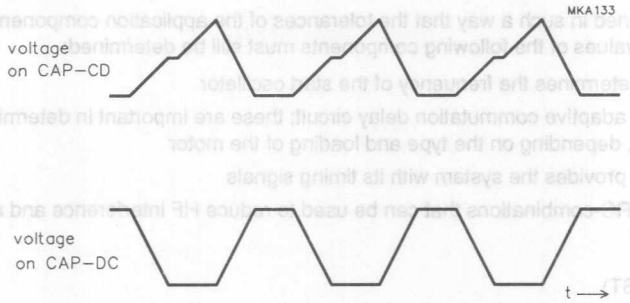


Fig.8 CAP-CD and CAP-DC voltage waveforms in normal running mode.

THE TIMING CAPACITOR (CAP-TI)

Capacitor CAP-TI is used for timing the successive steps within one commutation period; these steps include some internal delays.

The most important function is the watchdog time in which the motor EMF has to recover from a negative diode-pulse back to a positive EMF voltage (or vice versa). A watchdog timer is a guarding function that only becomes active when the expected event does not occur within a predetermined time.

The EMF usually recovers within a short time if the motor is running normally (<<ms). However, if the motor is motionless or rotating in the reverse direction, then the time can be longer (>>ms).
A watchdog time must be chosen so that it is long enough for a motor without EMF (still) and eddy currents that may stretch the voltage in a motor winding; however, it must be short enough to detect reverse rotation. If the watchdog time is made too long, then the motor may run in the wrong direction (with little torque).

The capacitor is charged, with a current of 57 µA, from 0.2 to 0.3 V. Above this level it is charged, with a current of 5 µA, up to 2.2 V only if the selected motor EMF remains in the wrong polarity (watchdog function). At the end, or, if the motor voltage becomes positive, the capacitor is discharged with a current of 28 µA. The watchdog time is the time taken to charge the capacitor, with a current of 5 µA, from 0.3 to 2.2 V. The value of CAP-TI is given by:

$$C = 5 \times 10^{-6} \times t_m / 1.9 = 2.63\, t_m \text{ (C in nF; t in ms)}$$

Example: If after switching off, the voltage from a motor winding is reduced, in 3.5 ms, to within 20 mV (the offset of the EMF comparator), then the value of the required timing capacitor is given by:

$$C = 2.63 \times 3.5 = 9.2 \text{ (choose 10 nF)}$$

Typical voltage waveforms are illustrated by Fig.9.

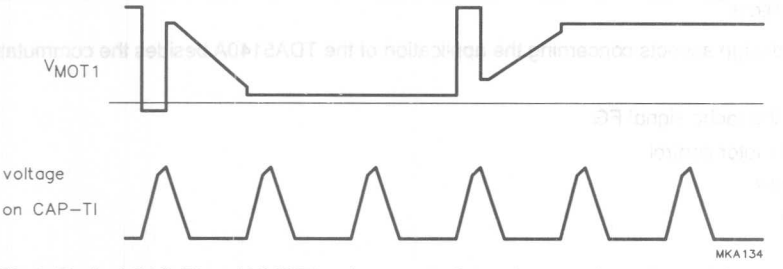


Fig.9 Typical CAP-TI and VMOT1 voltage waveforms in normal running mode.

Note to Fig. 9

If the chosen value of CAP-TI is too small, then oscillations can occur in certain positions of a blocked rotor. If the chosen value is too large, then it is possible that the motor may run in the reverse direction (synchronously with little torque).

THE EXTERNAL DAMPING COMPONENTS

Flyback pulses from the motor windings may cause HF interference and acoustic noise. The flyback pulses can be damped by RC-combinations in parallel with the motor windings. This reduces the HF interference; it also reduces the acoustic noise by several dB, depending on the motor construction.

These damping components also have negative effects. They not only dissipate energy from the flyback pulses, but also contribute to the overall energy consumption. Other negative effects are discussed below.

One negative effect is the distortion of the motor EMF sensed by the comparators in the TDA5145. This distortion may influence the correct functioning of the TDA5145, for example, an (damped) oscillation occurring after the winding has been switched off. This oscillation must be critically (or over critically) damped, so that:

$R^2 \times C = 4 \times L$ (L = inductance of one coil, R and C for damping)

A second requirement is that the effect of the damping components must be negligible by the time that the zero-crossing of the EMF is expected. This is because the remainder of the step (due to RC components) causes shifting of the zero-crossing. For a critically damped combination the voltage can be calculated as a negative exponential with $\omega_o \times t$.

Example: Commutation frequency = 900 Hz, so t = 1100 µs, the time taken from the end of the diode pulse to the zero-crossing of the EMF will be approximately t = 440 µs. If a damping voltage from 9 V to 3 mV is required, then the reduction is 3000-fold, or e exp–8 = e exp $-\omega_o \times t$. This gives ω_o = 18180 rad/s. With L = 3 mH, C is found to be 1.01 µF (use 1 µF) and R is found to be 109.1 Ω (use 100 Ω).

A motor voltage of 7 V (peak-to-peak) at 150 Hz gives 3300 V/s, thus a 3 mV remainder shifts the zero-crossing 1 µs. Eddy currents will also contribue to this phase shift. A shift of 20 µs corresponds with 0.18 degrees (mechanically) for a 1500 rpm motor, or 0.1 mm on a VHS scanner drum.

OTHER DESIGN ASPECTS

There are other design aspects concerning the application of the TDA5140A besides the commutation function. They are:

- Generation of the tacho signal FG
- Possibilities of motor control
- Preposition input
- Direction input
- Brake input
- Reliability

FG SIGNAL

The FG signal is generated in the TDA5145 by using the zero-crossing of the motor EMF from the three motor windings. Every zero-crossing in a (star connected) motor winding is used to toggle the FG output signal. The FG frequency is therefore half the commutation frequency. All transitions indicate the detection of a zero-crossing (except for PG). The negative-going edges are called FG pulses because they generate an interrupt in a controlling microprocessor.

The accuracy of the FG output signal (jitter) is very good. This accuracy depends on the symmetry of the motor's electromagnetic construction, which also effects the satisfactory functioning of the motor itself.

Example: A three phase motor with 6 magnetic pole-pairs at 1500 rpm and with a full-wave drive has a commutation frequency of 25 x 6 x 6 = 900 Hz, and generates a tacho signal of 450 Hz.

Direction input

If the voltage at pin 10 is less than 0.8 V, the motor is running in one direction (depending on the motor connections). If the voltage at pin 10 is higher than 2.0 V, the motor is running in the other direction.

Brake function

If the voltage at pin 9 is higher than 2.0 V, the motor brakes. In that condition, the 3 outputs MOT1, MOT2 and MOT3 are forced at a LOW voltage level and the current limitation is done internally by the sink drivers.

Test function

It is possible to turn off the three outputs by forcing a current of 600 μA into pin 3 (see Fig.10).

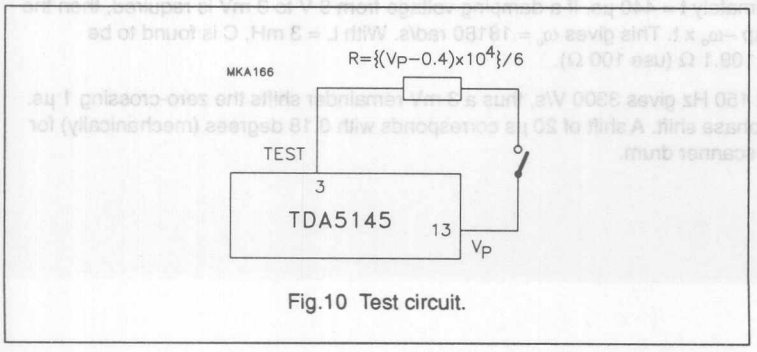


Fig.10 Test circuit.

Reset function

If the voltage at pin 21 is higher than 2.0 V, the output states are:

- MOT1 - FLOATING (F)
- MOT2 - LOW (L)
- MOT3 - HIGH (H)

Table 1 Switching sequence after a reset pulse

DIR	RESET	MOT1	MOT2	MOT3	FUNCTION
H	H	F	L	H	reset
H	L	F	L	H	normal direction mode sequence
H	L	H	L	F	
H	L	H	F	L	
H	L	F	H	L	
H	L	L	H	F	
H	L	L	F	H	
L	H	H	L	F	reset
L	L	H	L	F	reverse direction mode sequence
L	L	F	L	H	
L	L	L	F	H	
L	L	L	H	F	
L	L	F	H	L	
L	L	H	F	L	

Table 2 Priority of function

BRAKE	TEST	RESET	FUNCTION
L	L	L	normal
L	L	H	reset
L	H	L	test
L	H	H	test
H	L	L	brake
H	L	H	brake
H	H	L	brake
H	H	H	brake

Reset function

If the voltage at pin 21 is higher than 2.0 V, the output states are:

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H	H	F	L	H	reset
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H	L	H	L	F	
H	L	H	F	L	
H	L	F	H	L	
H	L	L	H	F	
H	L	L	F	H	
L	H	H	L	F	reset
L	L	H	L	F	reverse direction mode sequence
L	L	F	L	H	
L	L	L	F	H	
L	L	L	H	F	
L	L	F	H	L	
L	L	H	F	L	

Table 2 Priority of function

BRAKE	TEST	RESET	FUNCTION
L	L	L	normal
L	L	H	reset
L	H	L	test
L	H	H	test
H	L	L	brake
H	L	H	brake
H	H	L	brake
H	H	H	brake

Section 16
Miscellaneous

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NE5044	Programmable seven-channel RC encoder	939
NE630	Single-pole double-throw switch	945

Section 16
Miscellaneous

INDEX

NE5044 Programmable seven-channel RC encoder 839
NE850 Single-pole double-throw switch 845

Programmable seven-channel RC encoder NE5044

DESCRIPTION

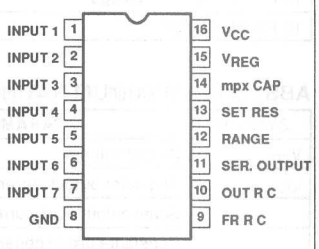
The NE5044 is a programmable parallel input, serial output pulse width encoder. A multiplexed dual linear ramp technique is used to allow up to 7 inputs to be converted to a serial pulse width modulated signal with excellent linearity and minimal crosstalk. Fixed or variable frame rates can be used, externally controlled, for ease of demodulation. An on-board 5V regulator eliminates power supply sensitivities and provides up to 20mA current capability for driving external loads.

APPLICATIONS

- Radio-controlled aircraft, cars, boats, trains
- Industrial controllers
- Remote-controlled entertainment systems
- Security systems
- Instrumentation recorders/controls
- Remote analog/digital data transmission
- Automotive sensor systems
- Robotics
- Telemetry

PIN CONFIGURATION

D, N Packages

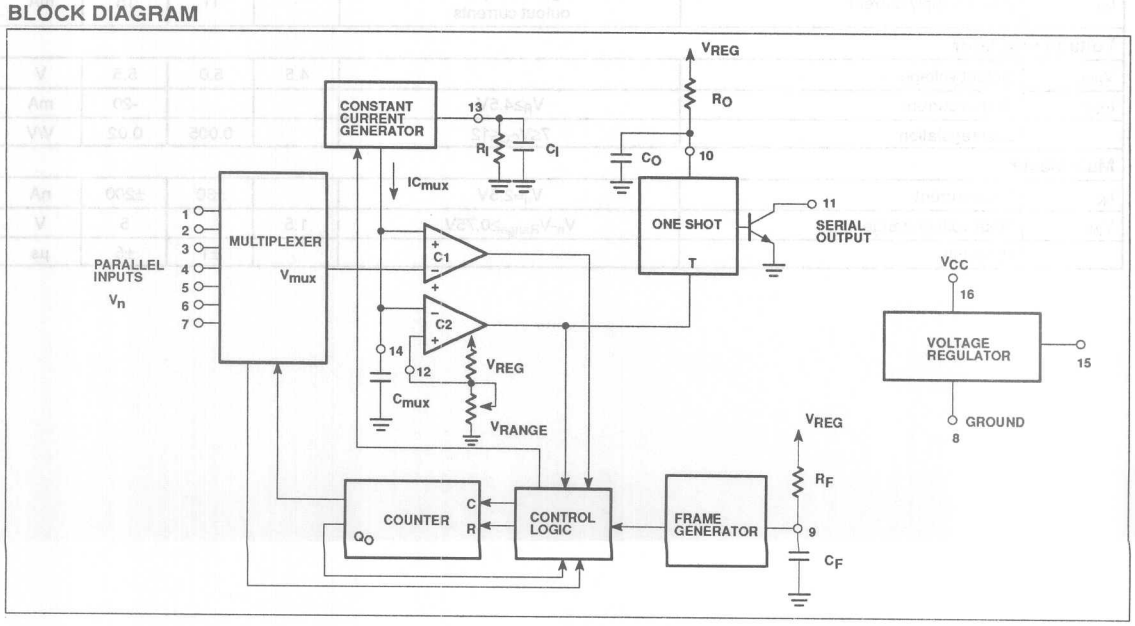


TOP VIEW

FEATURES

- 3 to 7 channels, externally selectable
- Constant-current dual linear ramp for linearity better than 0.3%
- Internal voltage regulator for low drift
- Wide supply range 4.5-12V
- Fixed or variable frame rate set by external RC
- External control for channel gain or range
- Versatile applications: exponential rates, mixing, dual rate, reversing, etc.
- Compatible with all transmission mediums

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO Package	0 to +70°C	NE5044D
16-Pin Plastic DIP	0 to +70°C	NE5044N

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	13	V
I_{OUT}	Regulator output current	-25	mA
	Serial output peak current	30	mA
	Constant-current generator	-1	mA
	Parallel inputs, range input	0-V_{REG}	V
	One-shot input, frame generator input	0-V_{REG}	V
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:
1. T_A=25°Cunless otherwise stated.

DC ELECTRICAL CHARACTERISTICS

Test Conditions T_A = 25°C V_{CC}=10V using Test Circuit, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Power supply requirements						
V_{CC}	Power supply voltage range		4.5		12	V
I_{CC}	Power supply current	Excluding control pots and serial output currents		11	15	mA
Voltage regulator						
V_{REG}	Output voltage		4.5	5.0	5.5	V
I_{OUT}	Output current	$V_R \geq 4.5V$			-20	mA
	Line regulation	$7 \leq V_{CC} \leq 12$		0.005	0.02	V/V
Multiplexer						
I_{IN}	Input current	V_n=2.5V		±30	±200	nA
V_{IN}	Input voltage range	V_n-$V_{Range} \geq 0.75V$	1.5		5	V
	Crosstalk			±1	±5	µs

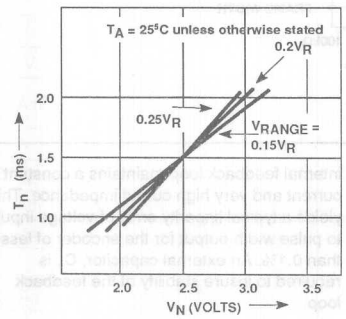
AC ELECTRICAL CHARACTERISTICS

Test conditions T_A=25°C, V_{CC}=10V using Test Circuit, unless otherwise stated.

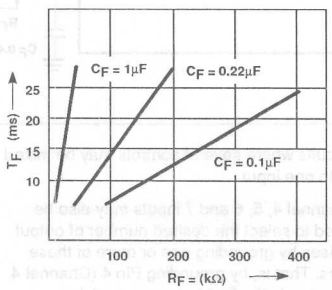
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Output pulse						
t_n	Position	$R_I \bullet C_{MUX}$=1.25ms V_n=0.5V_{REG}; V_{RANGE}=0.2V_{REG}	1350	1500	1650	µs
	Position linearity error			5		µs
	Position tempco	0°C ≤ T_A ≤70°C		0.15		µs/°C
	Position PSR	6V≤V_{CC} ≤12V		0.5	1	µs/V
t_O	Width	R_OC_O=300µs	240	285	330	µs
	Saturation voltage	I_O=25mA		0.6	1	V
I_{11}	Leakage current			0.05	50	µA
R_I	Range input voltage	R_I=50kΩ R_I=25kΩ	0.75 1.00			V V
	Frame time (fixed)	R_FC_F=30ms	17	20	23	ms
	Inhibit threshold				0.4	V

TYPICAL PERFORMANCE CHARACTERISTICS

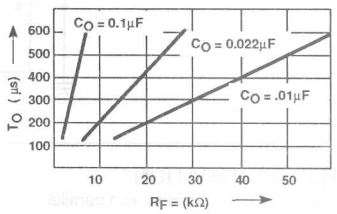
Output Pulse Width (T_n) vs Input Voltage (V_n)



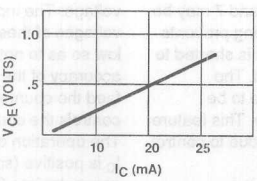
Frame Time (t_F) vs R_F



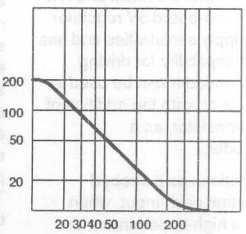
Output One-Shot Time (t_O) vs R_O



Output Saturation Voltage vs Output Current

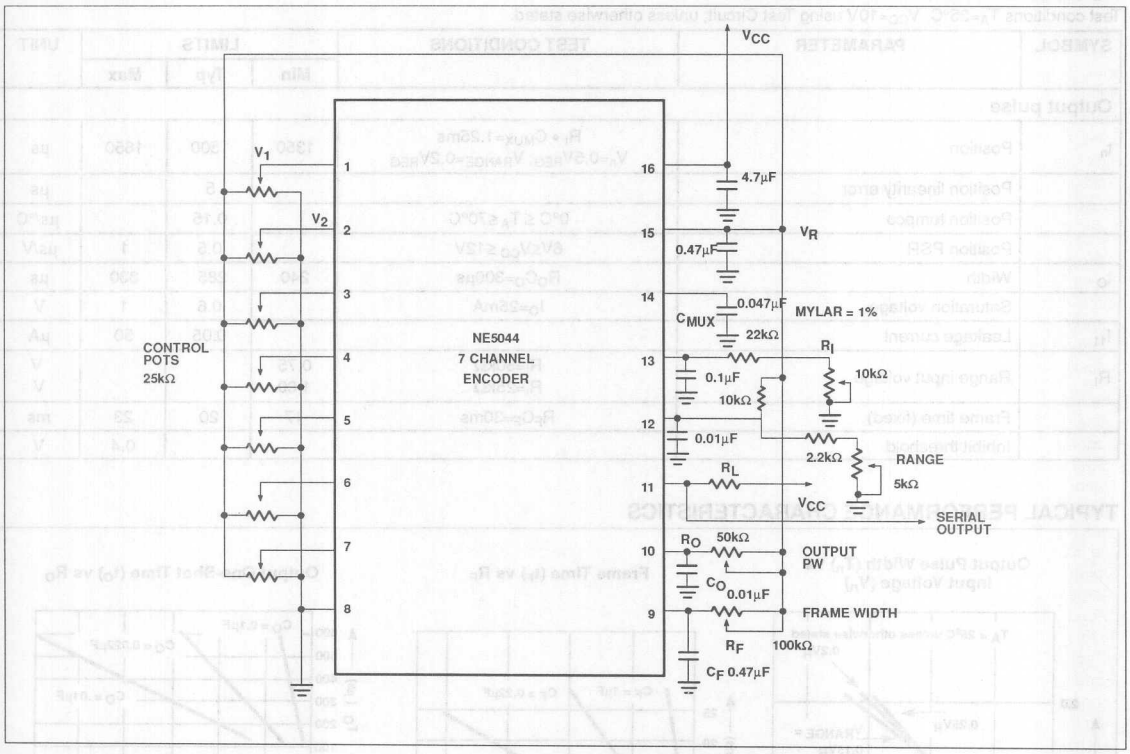


Consistent-Current vs R_I



Programmable seven-channel RC encoder NE5044

TEST CIRCUIT



CIRCUIT OPERATION

The NE5044 is a programmable parallel input, serial output encoder containing all the active circuitry necessary to generate a precise pulse width modulated signal with 3 to 7 channels. The number of channels is externally programmable by grounding unused control inputs. A multiplexed dual linear ramp technique is used to provide excellent linearity, minimal crosstalk and low temperature drift. An on-board 5V regulator eliminates power supply sensitivities and has up to 20mA current capability for driving external loads. The encoder can be used in the fixed-frame mode or, with the addition of one external NPN transistor, as a variable-frame encoder.

The multiplexer functions as a strobed voltage-follower so that each input, when active, appears as a high-impedance input (>1MΩ) and transfers the input voltage to the output. Only one of the seven inputs is active at any time and when a given input is inactive, it appears as an open circuit. The high-impedance multiplexer inputs eliminate loading on control inputs and simplify mixing circuits where several controls may be mixed onto one input.

Channel 4, 5, 6 and 7 inputs may also be used to select the desired number of output pulses by grounding one or more of these pins. That is, by grounding Pin 4 (Channel 4 input) only the first three inputs of the encoder will be used and a 3-channel encoder results. Grounding Pin 5 results in a 4-channel encoder, and so on. Thus, any number of channels between 3 and 7 may be selected. Internal voltage clamping prevents encoder malfunction if any input is shorted to supply, ground or open-circuited. The remaining channels will continue to be encoded except as noted above. This feature eliminates catastrophic failures due to control pot open- or short-circuits.

The constant-current generator is a bidirectional current source whose current is set by an external resistor R_I, where:

$$I_C = \pm \frac{V_R}{2R_I}$$

The current generator alternately charges and discharges the capacitor C_{MUX}. An internal feedback loop maintains a constant current and very high output impedance. This yields a typical linearity error of voltage input to pulse width output for the encoder of less than 0.1%. An external capacitor, C_I, is required to insure stability of the feedback loop.

Two high gain comparators, C1 and C2, compare the voltage across C_{MUX} with the multiplexer output voltage and the range input voltage. The input bias currents and offset voltages of these comparators are sufficiently low so as to not influence the overall accuracy of the encoder. The comparators feed the counter control logic which in turn controls the counter and current generator. The operation of this loop is as follows: When I_C is positive (sourced from the current generator into C_{MUX}) the capacitor linearly charges up until it reaches a voltage equal to the multiplexer output voltage; assume this to be the voltage at Pin 1, V1. At this time the output of C1 goes high, which reverses the direction of I_C (sinking into current generator from C_{MUX}). C_{MUX} now linearly discharges until it reaches the voltage set on Pin 12,

V_{RANGE}. At this time the output of C2 goes high, which again reverses the polarity of I_C, clocks the counter, and triggers the output one-shot. C_{MUX} again charges up but now C1 goes high when C_{MUX} reaches V2, the voltage on Pin 2. The resulting voltage waveform on C_{MUX} is a triangle wave whose positive peaks correspond to the voltages on Pins 1 through 7 for the first through seventh peaks and whose negative peaks are constant and equal to V_{RANGE}. This waveform is shown in the first portion of Figure 1.

Independent control of I_C and V_{RANGE} allows the encoder to be tailored to virtually any combination of input voltage changes and output pulse width changes. The functional relationships between these variables will be defined in the next section.

The frame generator controls the encoder frame time. It can operate as an astable or monostable multivibrator whose period is $0.66 \times R_F C_F$. The encoder will generate a synchronizing pulse at the end of each frame. When C_{MUX} reaches the seventh positive peak it reverses and discharges to V_{RANGE}. The counter is clocked to the state where Q_O is high when $VC_{MUX}=V_{RANGE}$. C_{MUX} again charges up, but now the output of C1 is ignored, due to Q_O being high, and charges up to V_{CLAMP} and remains there. The encoder will remain in this state until a pulse from the frame generator is received. If R_F and C_F are connected as shown in the Block Diagram, then the frame generator operates in the astable mode, producing a narrow pulse output. This pulse allows C_{MUX} to start discharging again. When C_{MUX} reaches V_{RANGE}, the counter is clocked to the state where Q_1 is high (channel 1) and the entire process starts over. The frame period in this mode is $0.66 \times R_F C_F$ and is referred to as the fixed-frame mode. The variable-frame mode will be discussed in the application section.

The output one-shot generates a positive pulse whose width is equal to $R_O C_O$. The output is an open-collector, NPN transistor capable of sinking 25mA. This configuration allows the encoder to drive a wide variety of RF stages as well as providing current pulses in 2-wire communications applications.

ENCODER DESIGN EQUATIONS

The triangular waveform on C_{MUX} has a fixed slope (constant current) and variable positive peak voltages. The time between the negative peaks of C_{MUX}, which is equal to the output period for that channel, is given by:

$$t_n = \frac{2\ (V_n - V_{RANGE})\ C_{MUX}}{I_C}$$

I_C is given by:

$$I_C = \frac{V_R}{2R_I}$$

where V_R=Reference Voltage.

Additionally, V_n, the voltage on Pin n, which is the control voltage for Channel n, is typically the wiper voltage on a pot connected between V_R and ground. Thus $V_n=X_nV_R$.

V_{RANGE} is also derived from V_R so that $V_{RANGE}=Y\ V_R$. The resulting channel time period is:

$$t_n = \frac{2\ (X_n - Y)\ V_R \cdot C_{MUX}}{(V_R\ /\ 2R_I)}$$

$$\boxed{t_n = 4R_I\ C_{MUX}\ (X_n - Y)}$$

Thus, each channel pulse width, t_n, is independent of supply voltage and depends only on external passive components.

The conversion rate, CR, for each channel is the change in output period, Δt_n, divided by the change in input voltage for that channel, ΔV_n.

$$CR = \frac{\Delta\ t_n}{\Delta\ V_n} = \frac{\Delta\ t_n}{\Delta\ X_n} = 4\ R_I\ C_{MUX}$$

In most applications, the input variable X_n will have some neutral or center value about which it will vary, thus $X_n = X_O + X_n$,

and

$$\boxed{CR = \frac{\Delta\ t_n}{\Delta\ X_n} = 4R_I\ C_{MUX}}$$

Where X_O is the neutral value for X and is assumed to be the same for all n. Now

$$t_n=4R_IC_{MUX}\ (X_O-Y+X_n)$$

If we let $t_{NEUTRAL}=4R_IC_{MUX}\ (X_O-Y)$ be the neutral value for t_n, then

$$\boxed{t_n = t_{NEUTRAL} + 4R_I\ C_{MUX}\ (X_n)}$$

Consider the following example to see how these design equations are used.

Assume:

$t_{NEUTRAL}$=1.5ms

X_O=0.5—Control pot in center at

$t_n=t_{NEUTRAL}$

$\Delta x_n=\pm 0.1$—Control pot resistance varies ±10% (of total resistance) around neutral. This should include mechanical trim if used.

$\Delta t_n=\pm 0.5$ms

For this example, the conversion rate is

$$CR = \frac{\Delta\ t_n}{\Delta\ X_n} = \frac{0.5ms}{0.1} = 5ms$$

so

$4R_IC_{MUX}$=5ms.

If we let C_{MUX}=0.047µF then

$$R_I = \frac{5ms}{4\ X\ 0.047\mu F} = 26.5k\Omega = 27k\Omega$$

and

$t_{NEUTRAL}=1.5ms=4R_IC_{MUX}(X_o-Y)$

$$Y = 0.5 - \frac{1.5ms}{5ms} = 0.2$$

The output pulse width is given by

$t_O=R_OC_O$

so if t_O=330µs and C_O=0.01µF then

$$R_O = \frac{330\mu s}{0.01\mu F} = 33k\Omega$$

The frame time constant, t_F, is given by

$t_F=0.66\ R_FC_F$.

If t_F=20ms and C_F=0.47µF

$$R_F = \frac{20ms}{0.66X0.47\mu F} = 62k$$

Figure 2 shows the external connections for this example.

It should be noted that the temperature stability of all the encoded times depend on the temperature coefficients of the respective external R_C time constants. No internal temperature compensation is used on the chip. The typical temperature sensitivity of t_n using wirewound resistors and polycarbonate capacitors is less than 100ppm/°C in the -20°C to +70°C temperature range. For the above example, this corresponds to a change in t_n of ±7.5µs for a change in temperature of ±50°C.

Programmable seven-channel RC encoder NE5044

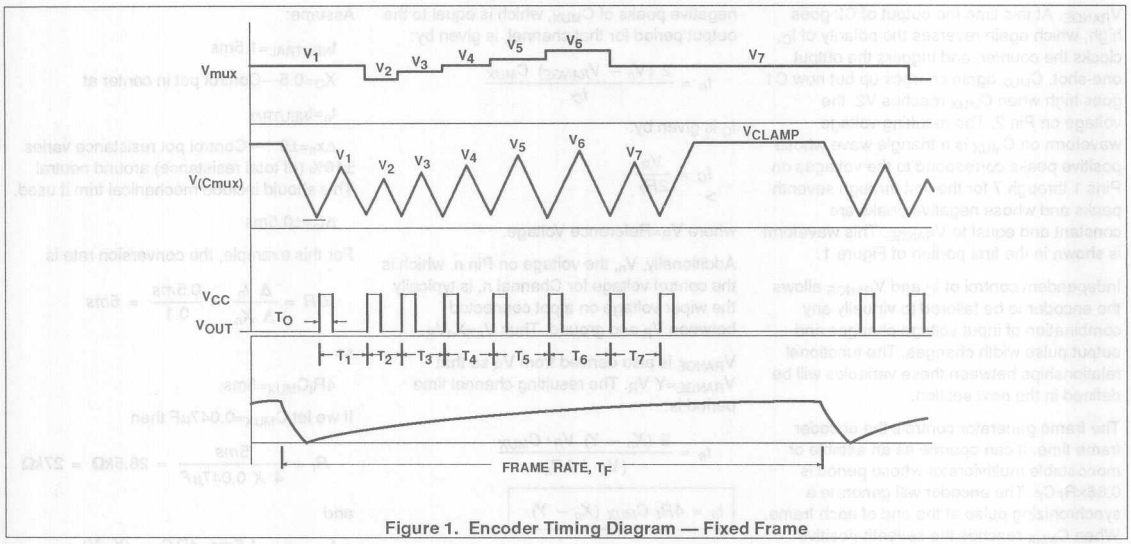


Figure 1. Encoder Timing Diagram — Fixed Frame

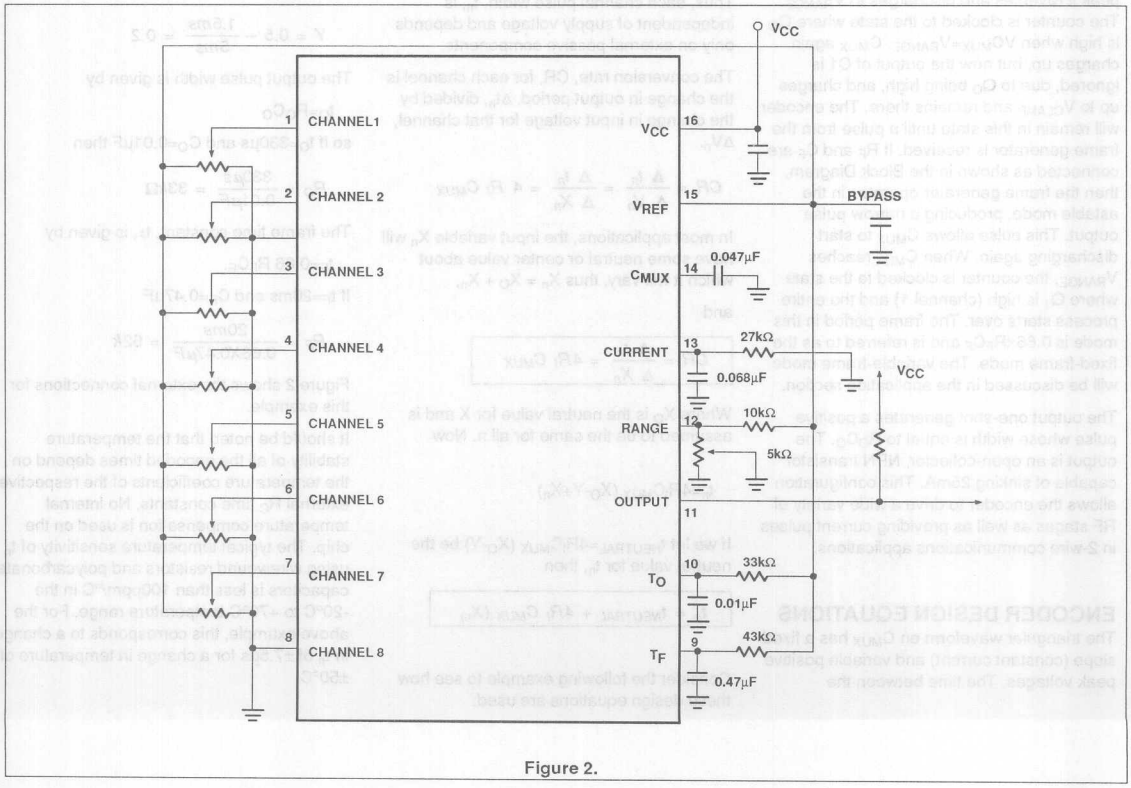


Figure 2.

Single pole double throw (SPDT) switch NE/SA630

DESCRIPTION

The NE630 is a wideband RF switch fabricated in BiCMOS technology and incorporating on-chip CMOS/TTL compatible drivers. Its primary function is to switch signals in the frequency range DC - 1GHz from one 50Ω channel to another. The switch is activated by a CMOS/TTL compatible signal applied to the enable channel 1 pin (ENCH1).

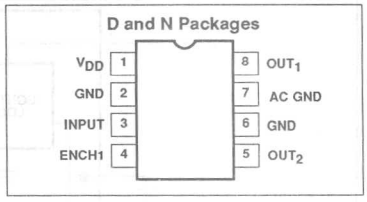
The extremely low current consumption makes the NE/SA630 ideal for portable applications. The excellent isolation and low loss makes this a suitable replacement for PIN diodes.

The NE/SA630 is available in an 8-pin dual in-line plastic package and an 8-pin SO (surface mounted miniature) package.

FEATURES

- Wideband (DC - 1GHz)
- Low through loss (1dB typical at 200MHz)
- Unused input is terminated internally in 50Ω
- Excellent overload capability (1dB gain compression point +18dBm at 300MHz)
- Low DC power (170μA from 5V supply)
- Fast switching (20ns typical)
- Good isolation (off channel isolation 60dB at 100MHz)
- Low distortion (IP_3 intercept +33dBm)
- Good 50Ω match (return loss 18dB at 400MHz)
- Full ESD protection
- Bidirectional operation

PIN CONFIGURATION



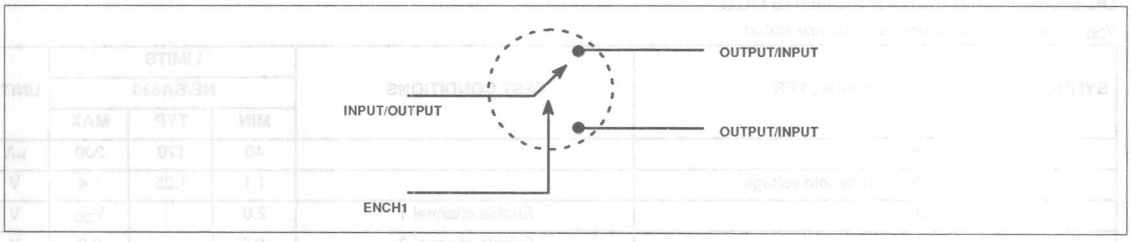
APPLICATIONS

- Digital transceiver front-end switch
- Antenna switch
- Filter selection
- Video switch
- FSK transmitter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to 70°C	NE630N
8-Pin Plastic SO (Surface-mount)	0 to 70°C	NE630D
8-Pin Plastic DIP	-40 to +85°C	SA630N
8-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA630D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

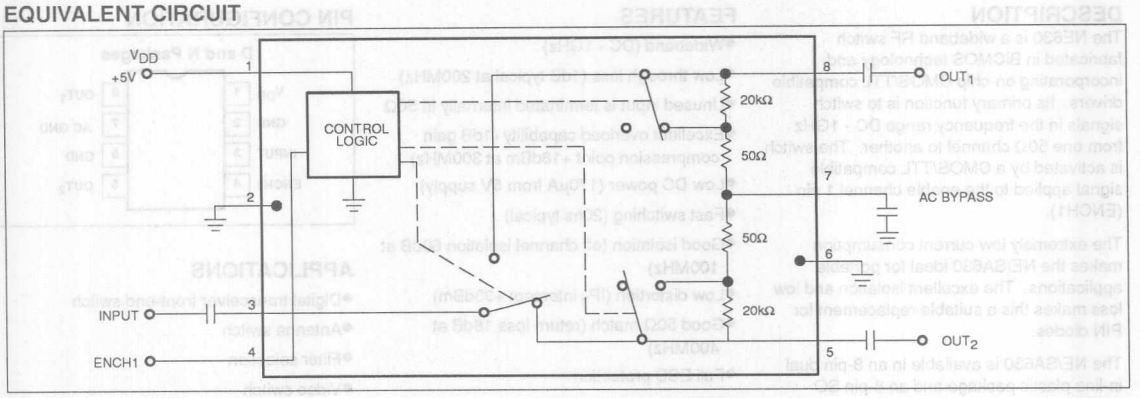
SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	-0.5 to +5.5	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 8-Pin Plastic DIP 8-Pin Plastic SO	 1160 780	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	-65 to +150	°C

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   8-Pin DIP: θ_{JA} = 108°C/W
   8-Pin SO: θ_{JA} = 158°C/W

Single pole double throw (SPDT) switch NE/SA630

EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	3.0 to 5.5V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA630			UNITS
			MIN	TYP	MAX	
I_{DD}	Supply current		40	170	300	µA
V_T	TTL/CMOS logic threshold voltage[1]		1.1	1.25	1.4	V
V_{IH}	Logic 1 level	Enable channel 1	2.0		V_{DD}	V
V_{IL}	Logic 0 level	Enable channel 2	-0.3		0.8	V
I_{IL}	ENCH1 input current	ENCH1 = 0.4V	-1	0	1	µA
I_{IH}	ENCH1 input current	ENCH1 = 2.4V	-1	0	1	µA

NOTE:
1. The ENCH1 input must be connected to a valid Logic Level for proper operation of the NE/SA630.

AC ELECTRICAL CHARACTERISTICS[1] - D PACKAGE

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA630			
			MIN	TYP	MAX	
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2	 2.8	dB
S_{21}, S_{12}	Isolation (OFF channel)[2]	10MHz 100MHz 500MHz 900MHz	70 24	80 60 50 30		dB
S_{11}, S_{22}	Return loss (ON channel)	DC - 400MHz 900MHz		20 12		dB
S_{11}, S_{22}	Return loss (OFF channel)	DC - 400MHz 900MHz		17 13		dB
t_D	Switching speed (on-off delay)	50% TTL to 90/10% RF		20		ns
t_r, t_f	Switching speeds (on-off rise/fall time)	90%/10% to 10%/90% RF		5		ns
	Switching transients			165		mV_{P-P}
P_{-1dB}	1dB gain compression	DC - 1GHz		+18		dBm
IP_3	Third-order intermodulation intercept	100MHz		+33		dBm
IP_2	Second-order intermodulation intercept	100MHz		+52		dBm
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.0		dB

NOTE:
1. All measurements include the effects of the D package NE/SA630 Evaluation Board (see Figure 1B). Measurement system impedance is 50Ω.
2. The placement of the AC bypass capacitor is critical to achieve these specifications. See the applications section for more details.

AC ELECTRICAL CHARACTERISTICS[1] - N PACKAGE

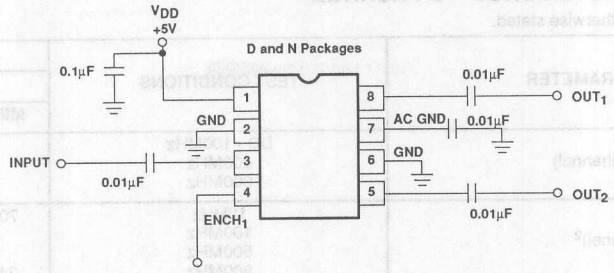
V_{DD} = +5V, T_A = 25°C; all other characteristics similar to the D-Package, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA630			
			MIN	TYP	MAX	
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2.5		dB
S_{21}, S_{12}	Isolation (OFF channel)	10MHz 100MHz 500MHz 900MHz	58	68 50 37 15		dB
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.5		dB

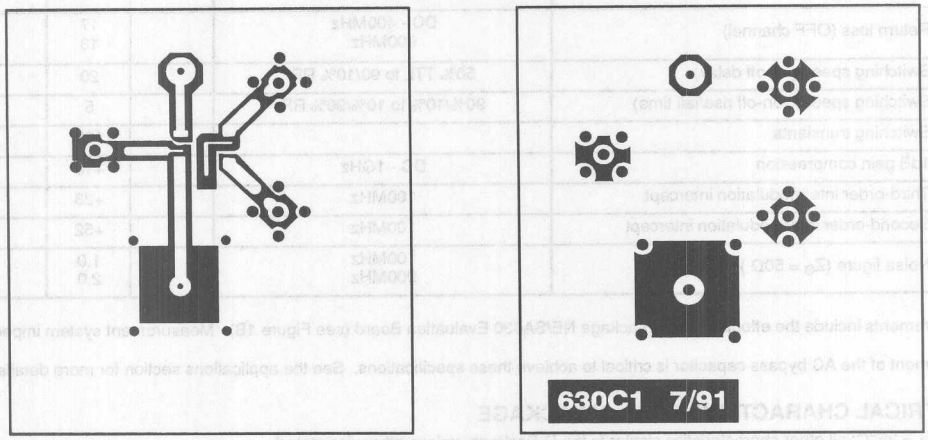
NOTE:
1. All measurements include the effects of the N package NE/SA630 Evaluation Board (see Figure 1C). Measurement system impedance is 50Ω.

APPLICATIONS

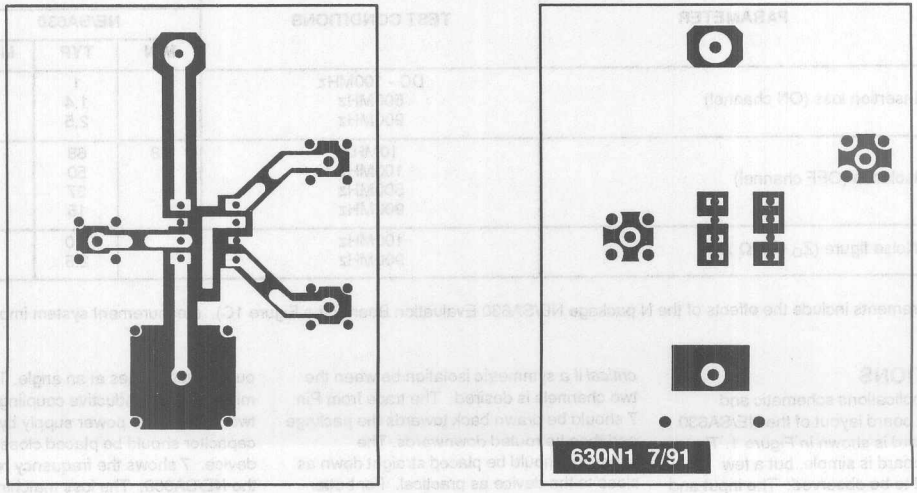
The typical applications schematic and printed circuit board layout of the NE/SA630 evaluation board is shown in Figure 1. The layout of the board is simple, but a few cautions need to be observed. The input and output traces should be 50Ω. The placement of the AC bypass capacitor is *extremely critical* if a symmetric isolation between the two channels is desired. The trace from Pin 7 should be drawn back towards the package and then be routed downwards. The capacitor should be placed straight down as close to the device as practical. For better isolation between the two channels at higher frequencies, it is also advisable to run the two output/input traces at an angle. This also minimizes any inductive coupling between the two traces. The power supply bypass capacitor should be placed close to the device. 7 shows the frequency response of the NE/SA630. The loss matching between the two channels is excellent to 1.2GHz as shown in



a. NE/SA Evaluation Board Schematic



b. NE/SA630 D-Package Board Layout



c. NE/SA630 N-Package Board Layout

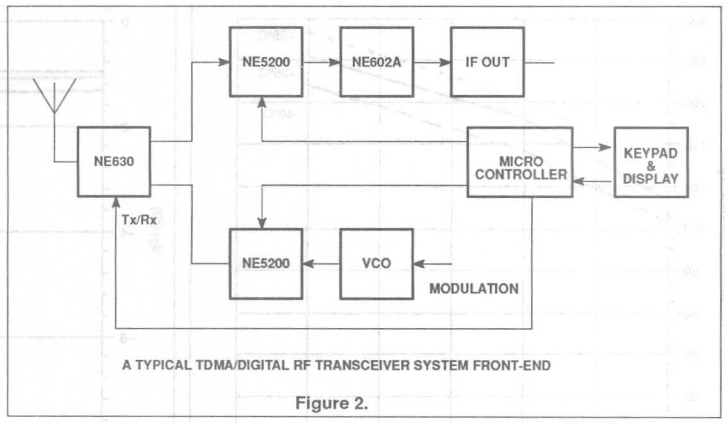
Figure 1.

10. The isolation and matching of the two channels over frequency is shown in 12 and 14, respectively.

The NE630 is a very versatile part and can be used in many applications. 2 shows a block diagram of a typical Digital RF transceiver front-end. In this application the NE630 replaces the duplexer which is typically very bulky and lossy. Due to the low power consumption of the device, it is ideally suited for handheld applications such as in CT2 cordless telephones. The NE630 can also be used to generate Amplitude Shift Keying (ASK) or On-Off Keying (OOK) and Frequency Shift Keying (FSK) signals for digital RF communications systems. Block diagrams for these applications are shown in 3 and 4, respectively.

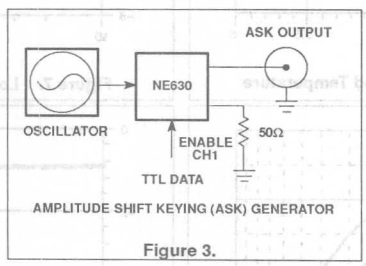
For applications that require a higher isolation at 1GHz than obtained from a single NE630, several NE630s can be cascaded as shown in 5. The cascaded configuration will have a higher loss but greater than 35dB of isolation at 1GHz and greater than 65dB @ 500MHz can be obtained from this configuration. By modifying the enable control, an RF multiplexer/ de-multiplexer or antenna selector can be constructed. The simplicity of NE630 coupled with its ease of use and high performance lends itself to many innovative applications.

The NE/SA630 switch terminates the OFF channel in 50Ω. The 50Ω resistor is internal and is in series with the external AC bypass capacitor. Matching to impedances other than 50Ω can be achieved by adding a resistor in series with the AC bypass capacitor (e.g., 25Ω additional to match to a 75Ω environment).



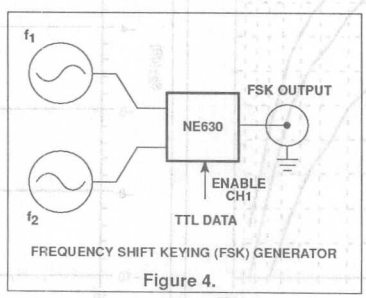
A TYPICAL TDMA/DIGITAL RF TRANSCEIVER SYSTEM FRONT-END

Figure 2.



AMPLITUDE SHIFT KEYING (ASK) GENERATOR

Figure 3.



FREQUENCY SHIFT KEYING (FSK) GENERATOR

Figure 4.

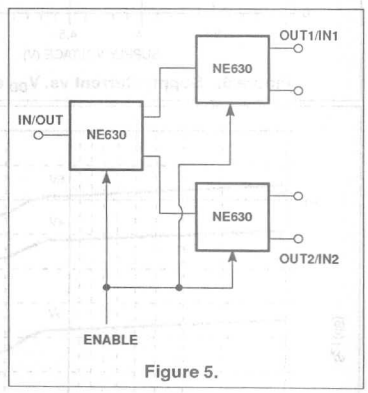


Figure 5.

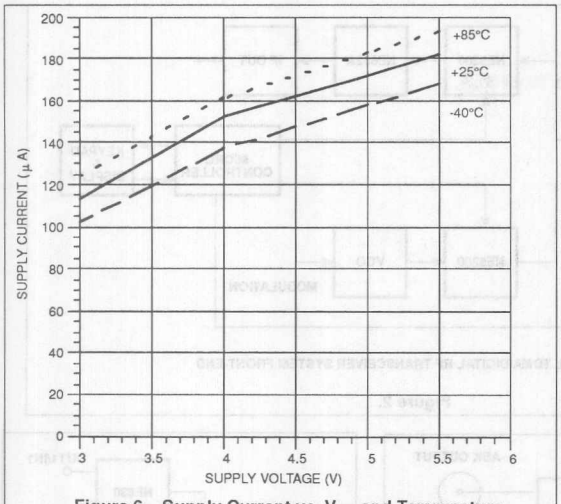


Figure 6. Supply Current vs. V_{DD} and Temperature

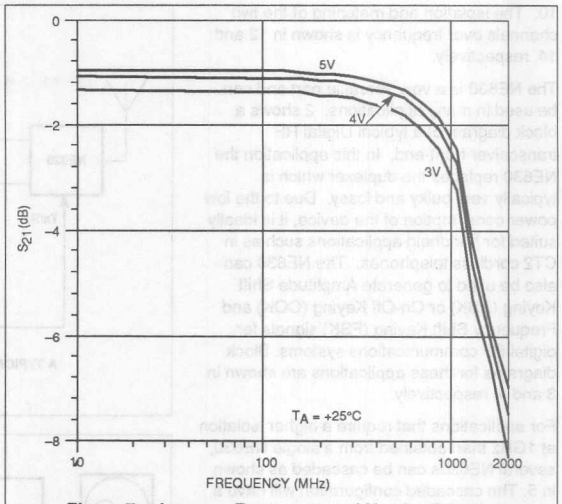


Figure 7. Loss vs. Frequency and V_{DD} for D-Package

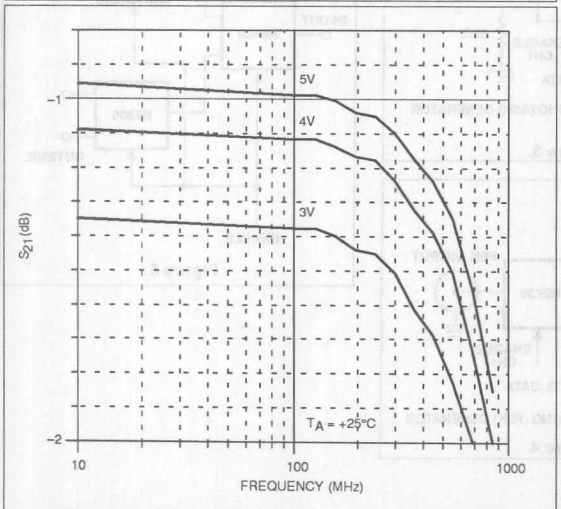


Figure 8. Loss vs. Frequency and V_{DD} for D-Package -Expanded Detail-

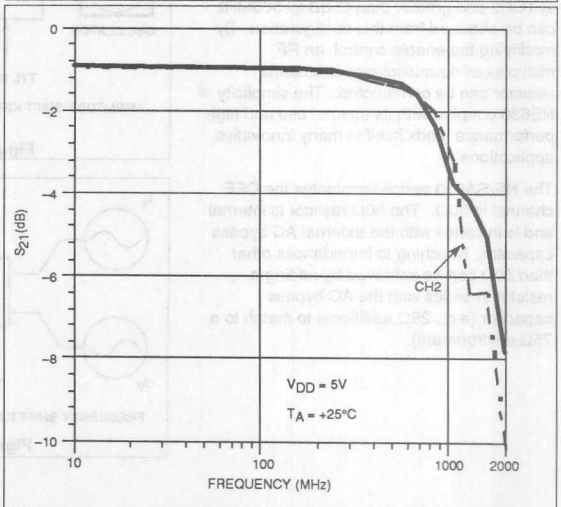


Figure 9. Loss Matching vs. Frequency for N-Package (DIP)

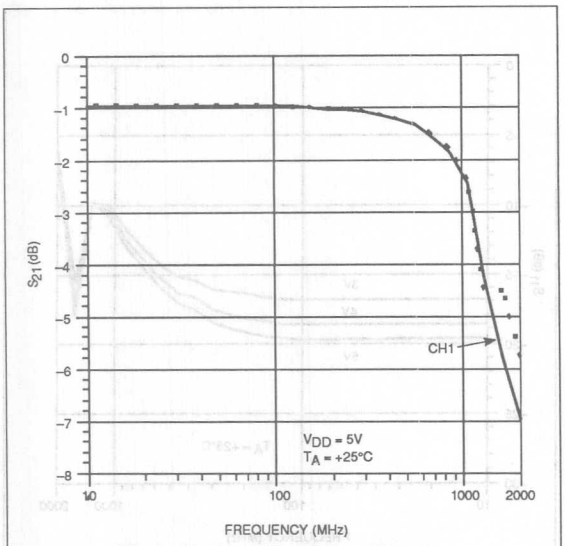


Figure 10. Loss Matching vs. Frequency; CH1 vs. CH2 for D-Pakage

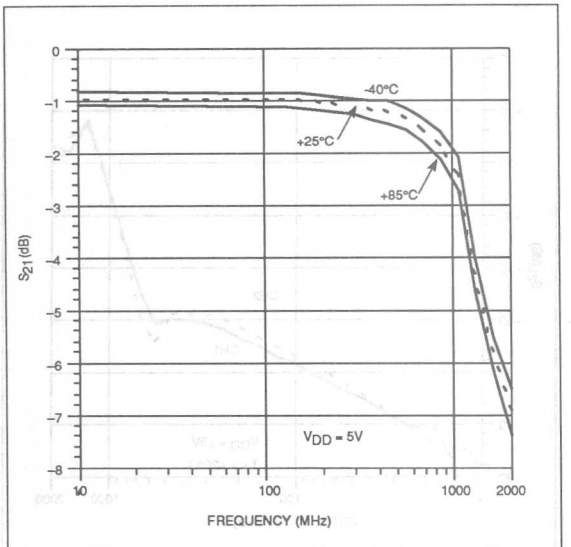


Figure 11. Loss vs. Frequency and Temperature for D-Package

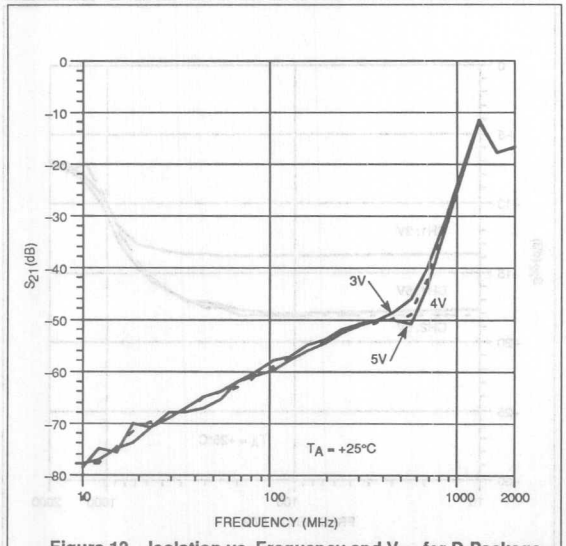


Figure 12. Isolation vs. Frequency and V_{DD} for D-Package

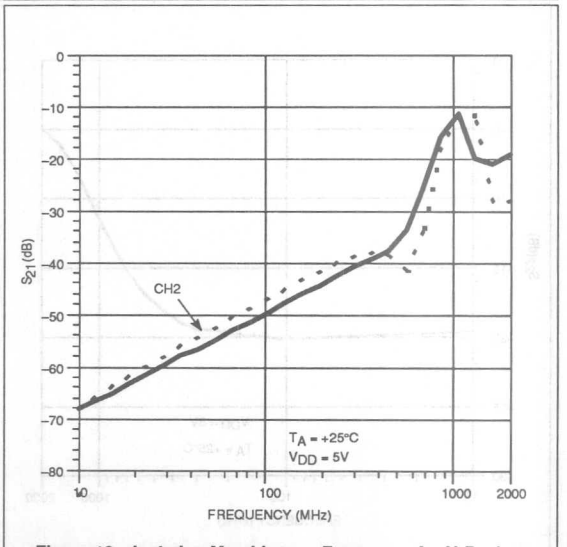


Figure 13. Isolation Matching vs. Frequency for N-Package (DIP)

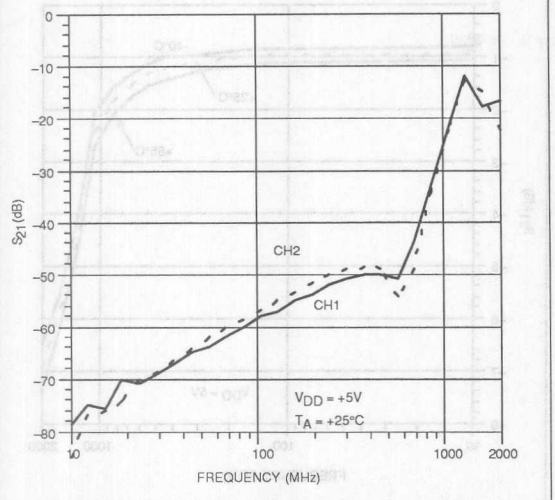


Figure 14. Isolation Matching vs. Frequency; CH1 vs. CH2 for D-Package

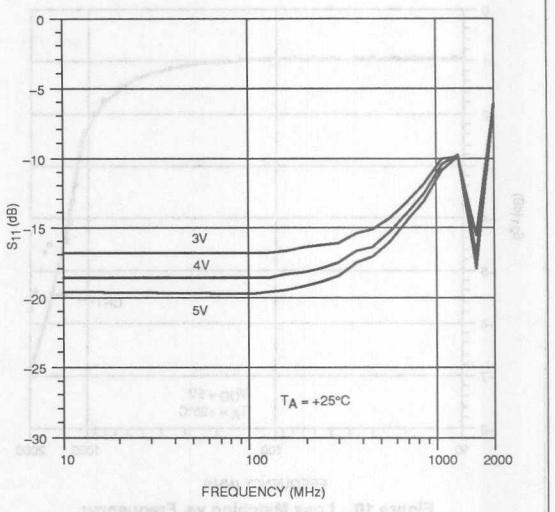


Figure 15. Input Match On-Channel vs. Frequency and V_{DD}

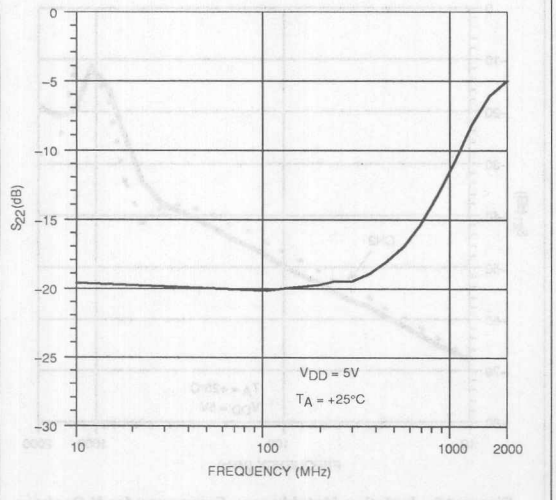


Figure 16. Output Match On-Channel vs. Frequency

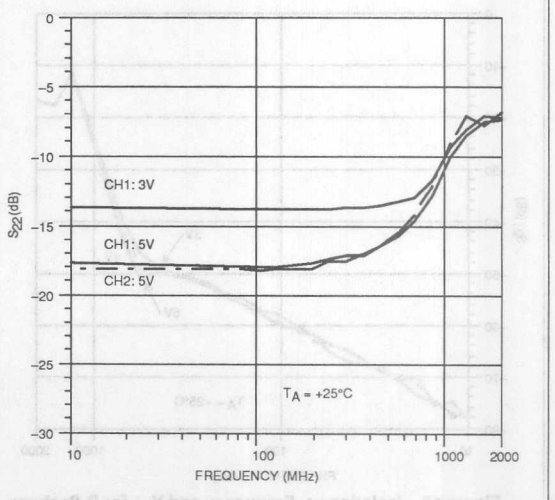


Figure 17. OFF-Channel Match vs. Frequency and V_{DD}

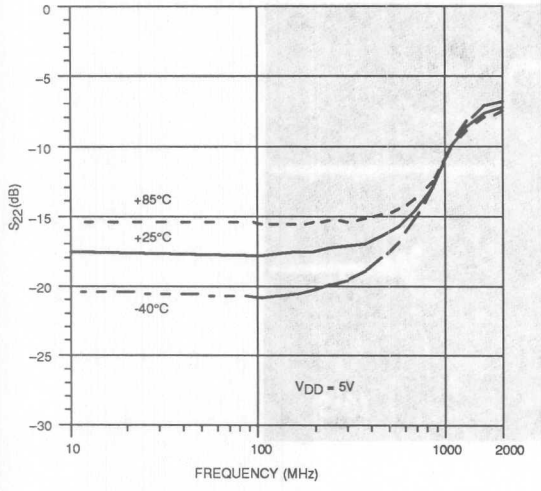


Figure 18. OFF Channel Match vs. Frequency and Temperature

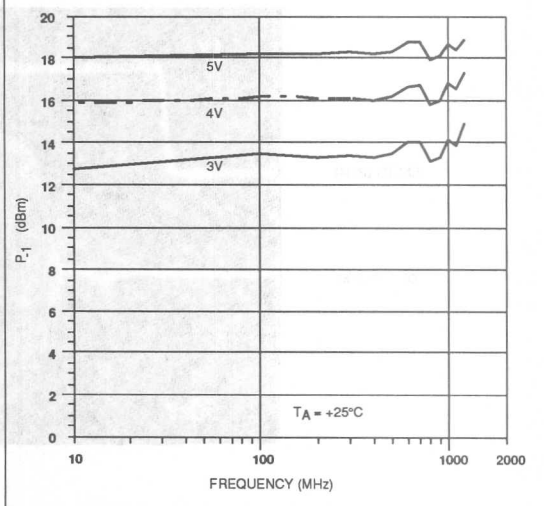


Figure 19. P_{-1} dB vs. Frequency and V_{DD}

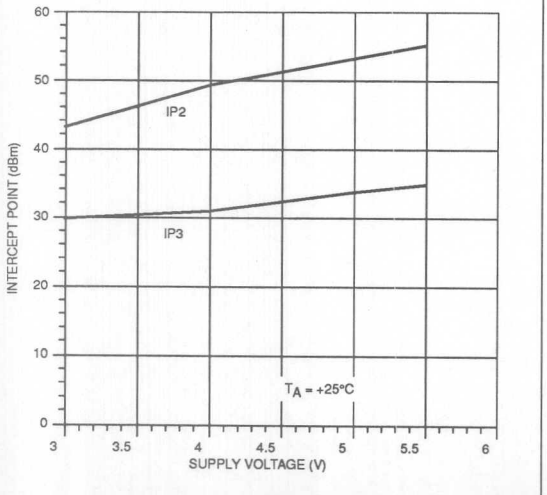


Figure 20. Intercept Points vs.V_{DD}

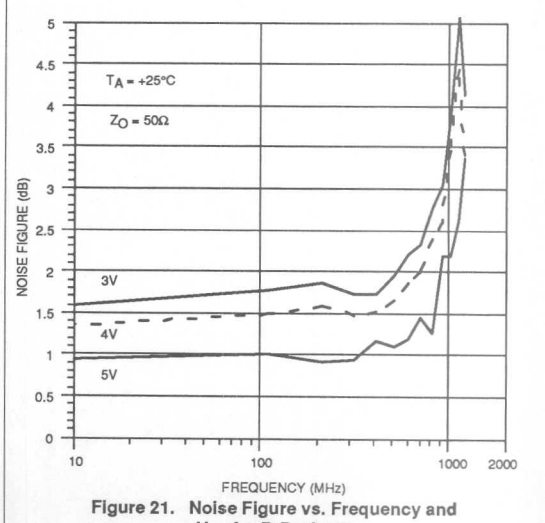


Figure 21. Noise Figure vs. Frequency and V_{DD} for D-Package

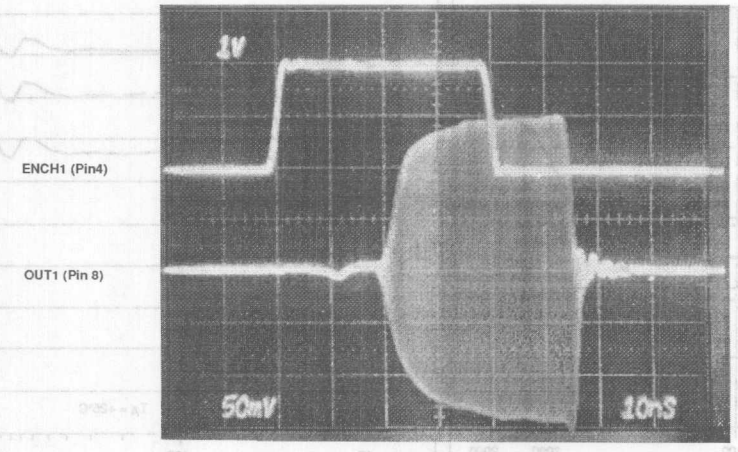


Figure 22. Switching Speed; f_{IN} = 100MHz at -6dBm, V_{DD} = 5V

Section 17
Package outlines

General Purpose/Linear ICs

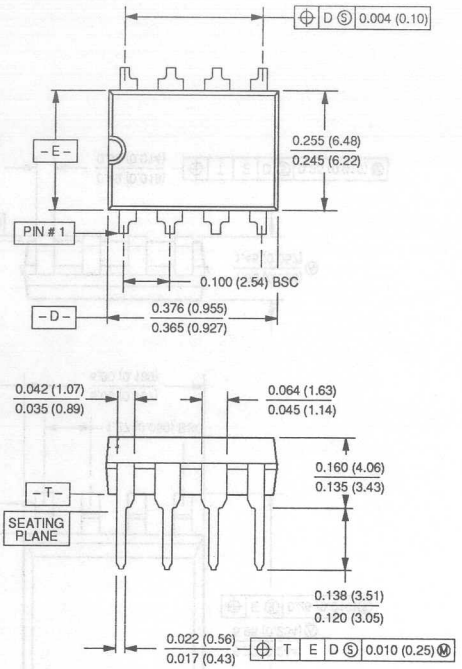
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8-Pin Ceramic Dual In-Line (F) Package 959
14-PIn (300 mils wide) Plastic Dual In-Line (N) package 960
14-Pin (157 mils wide) Plastic SO (Small Outline) Dual In-Line (D) Package 961
14-Pin Ceramic Dual In-line (F) Package 962
16-Pin (300 mils wide) Plastic Dual In-Line (N) Package 963
16-Pin (300 mils wide) Plastic SOL (Small Outline Large) Dual In-Line (D) Package 964
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24-Pin (600 mils wide) Ceramic Dual In-Line (F) Package 980
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SOT110B 9-Pin Plastic Single In-line (U) Package 986
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SOT146 20-Pin Plastic Dual In-Line (N/P) Package 991
SOT163A 20-Pin SO (Small Outline) Plastic Dual In-Line (D/T) Package 992
SOT101 24-Pin Plastic Dual In-Line (N/P) Package with Internal Heatspreader ... 993
SOT137A 24-Pin Plastic SO (Small Outline) Dual In-Line (D/T) Package 994
SOT117 28-Pin Plastic Dual In-Line (N/P) Package 995
SOT136A 28-Pin Plastic SOL (Small Outline Large) Dual In-Line (N/P) Package . 996
SOT232 32-Pin Plastic Shrink Dual In-Line (N/P) Package 997

Section 17
Package outlines

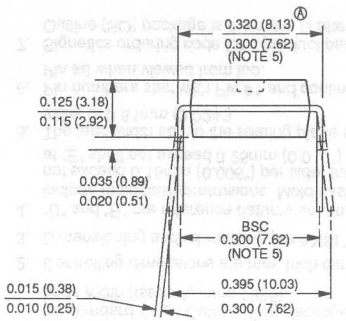
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SOT136A 28-Pin Plastic SOL (Small Outline Large) Dual In-Line (N/P) Package .. 996
SOT232 32-Pin Plastic-Shrink Dual In-Line (N/P) Package 997



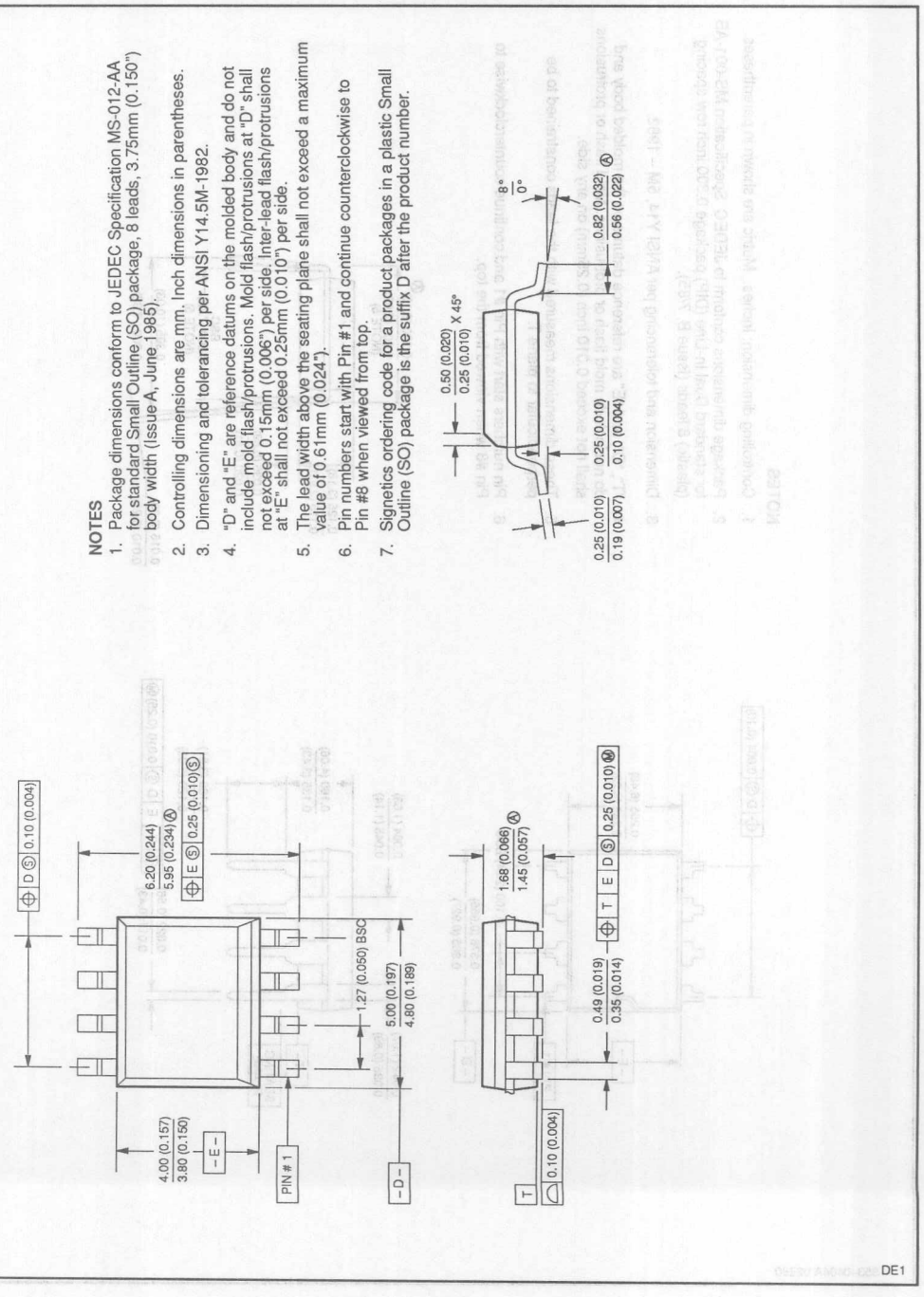
NOTES

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AB for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 8 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from the top.



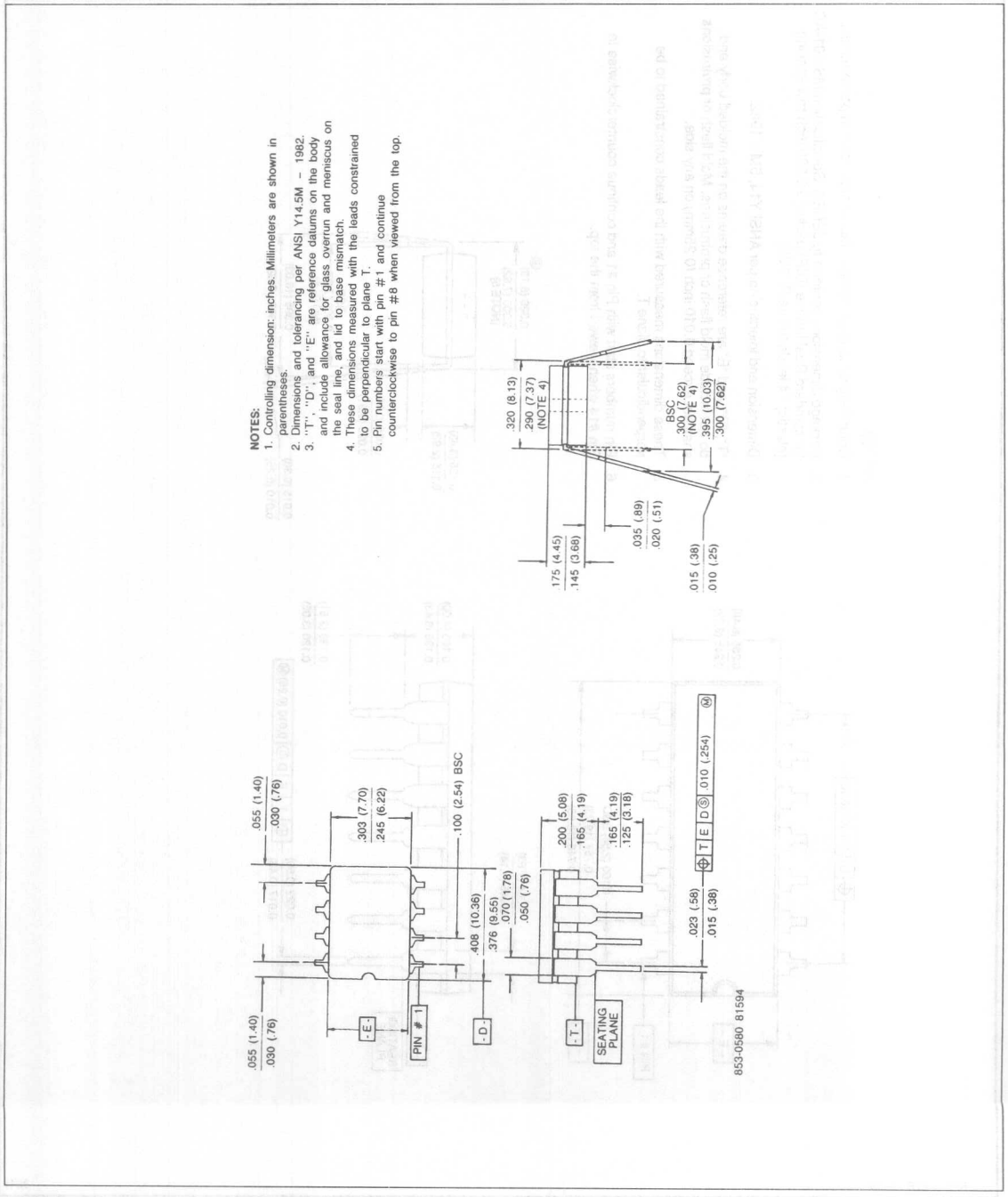
Package outlines

8-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE



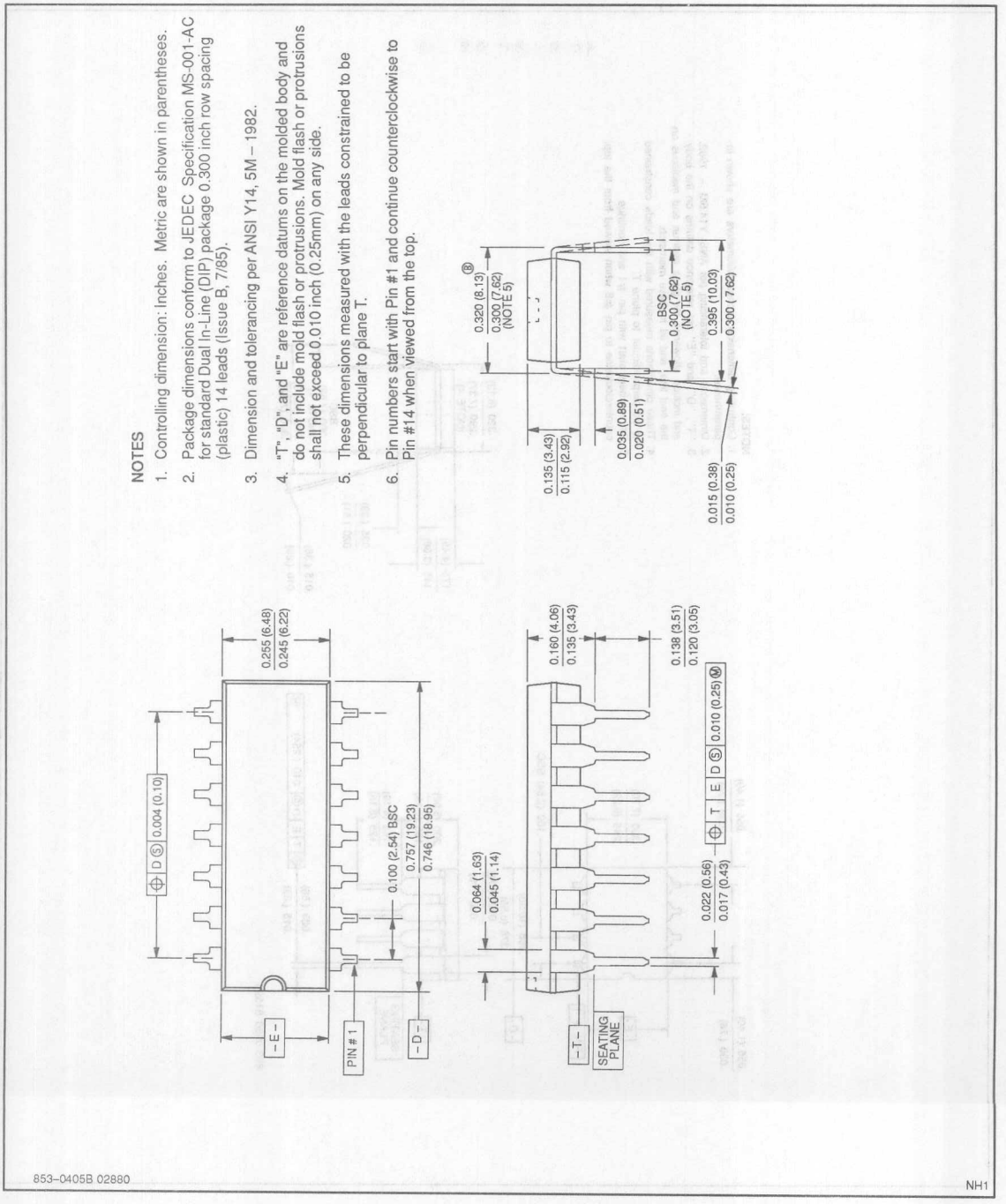
Package outlines

8-PIN CERAMIC DUAL IN-LINE (F) PACKAGE



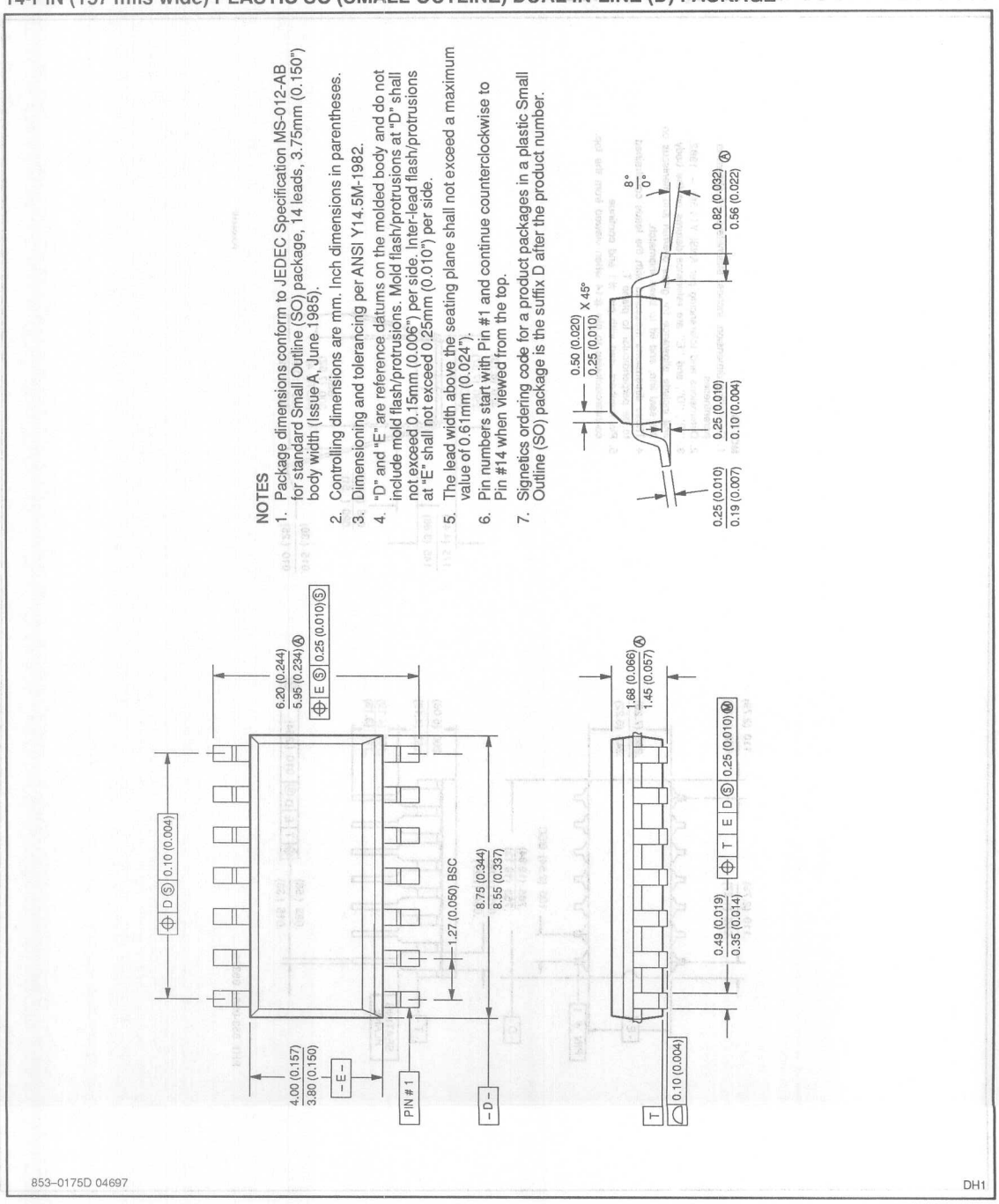
Package outlines

14-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



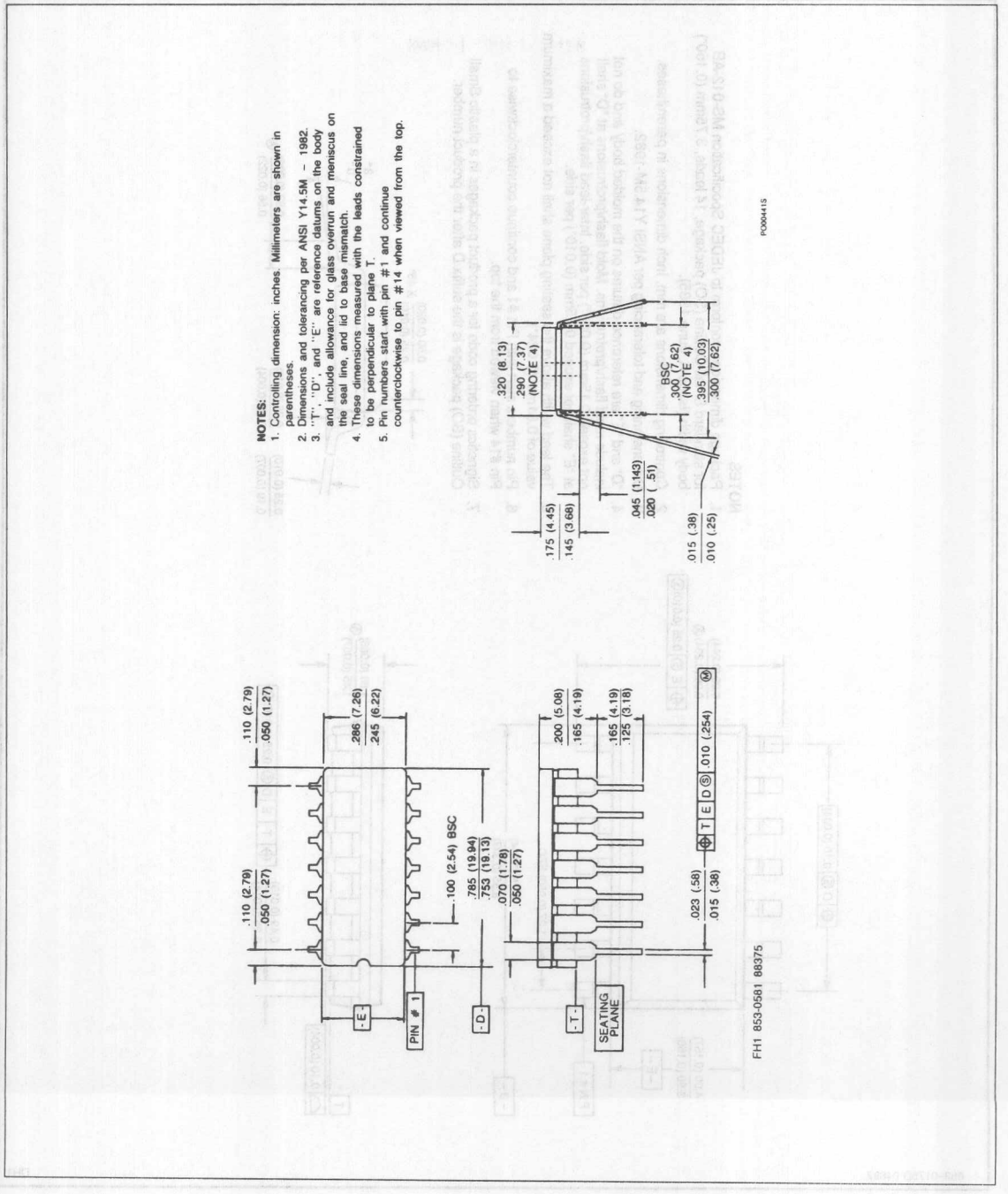
Package outlines

14-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE



Package outlines

14-PIN CERAMIC DUAL IN-LINE (F) PACKAGE

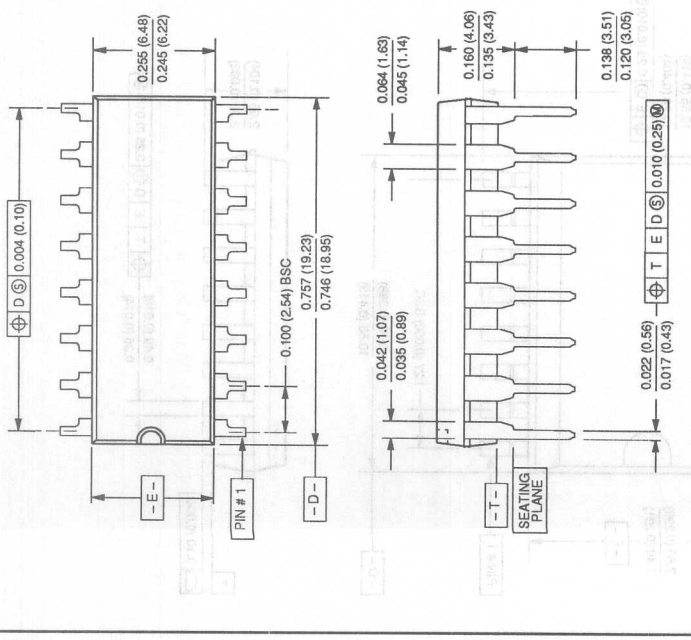


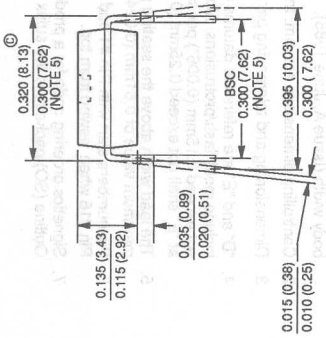
Package outlines

16-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE

NOTES

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AA for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 16 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #16 when viewed from the top.



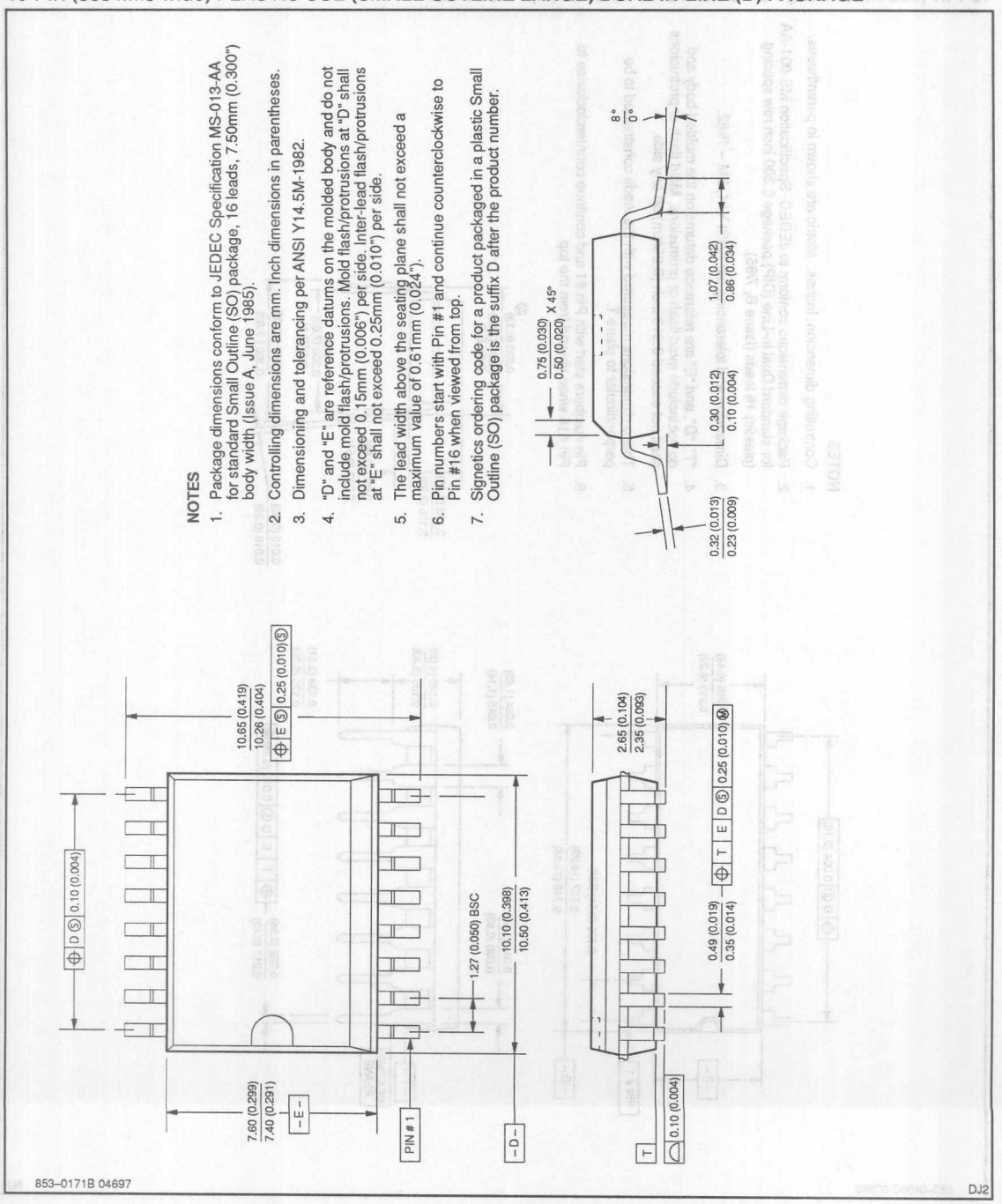


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NJ1

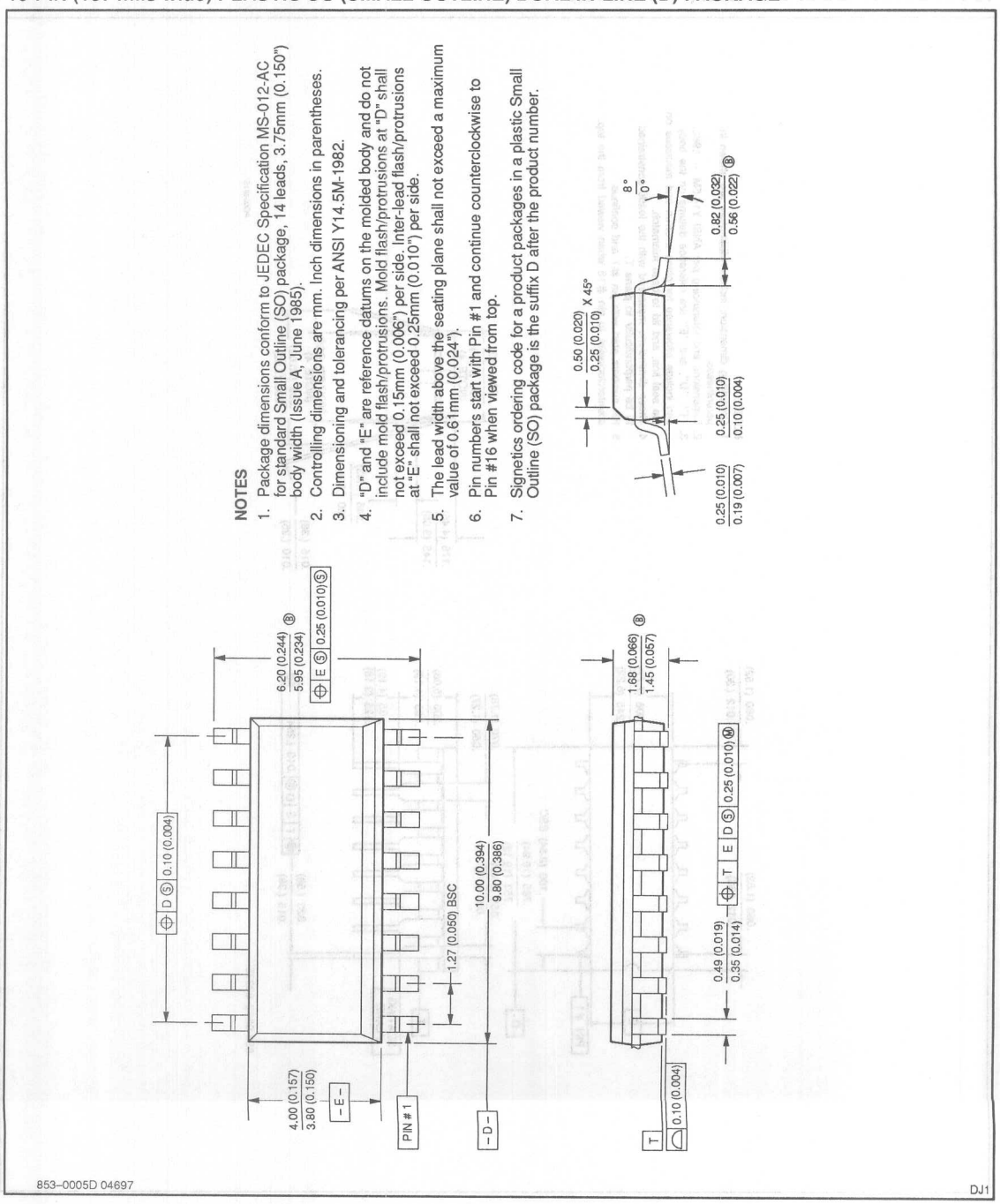
Package outlines

16-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



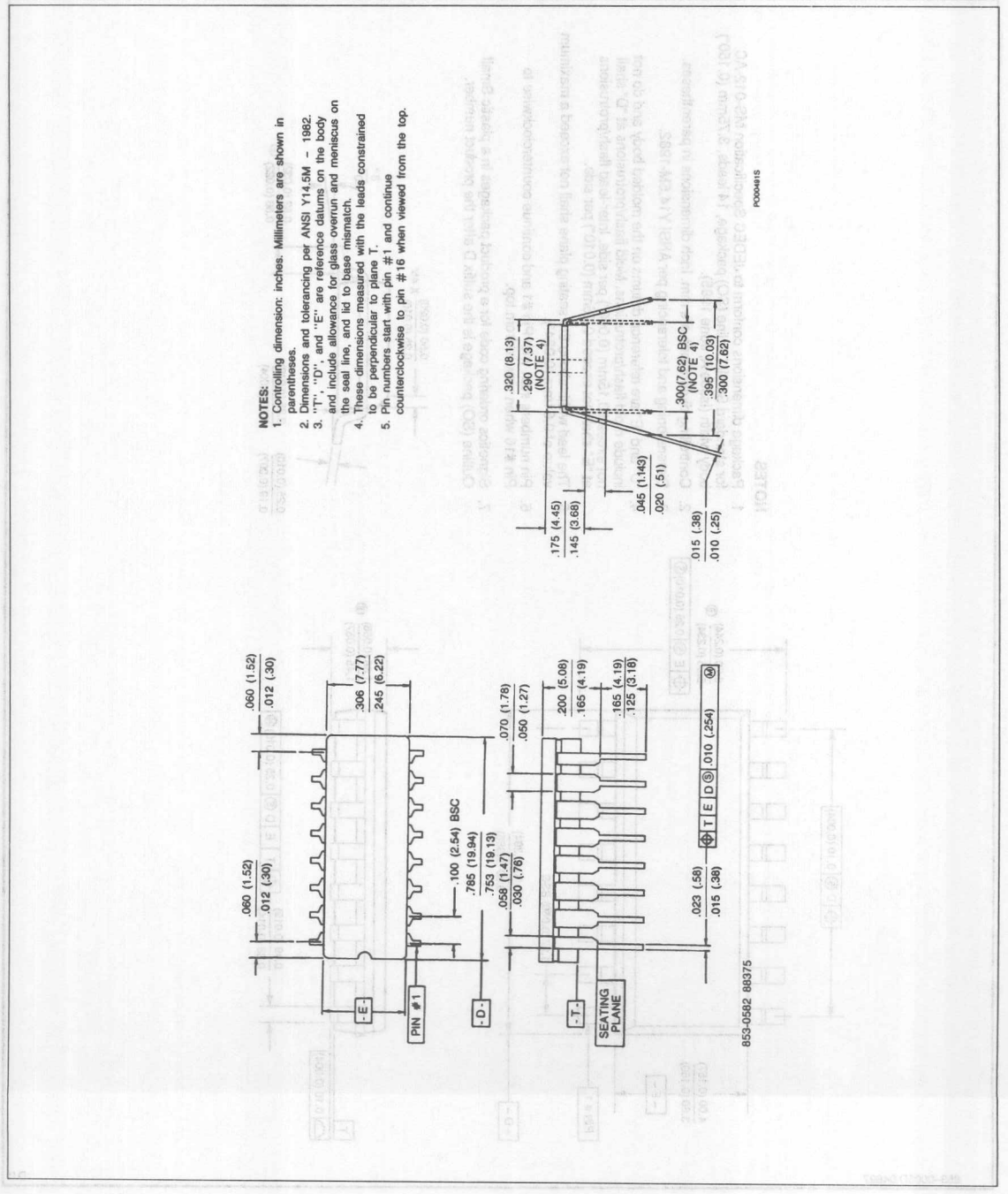
Package outlines

16-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE



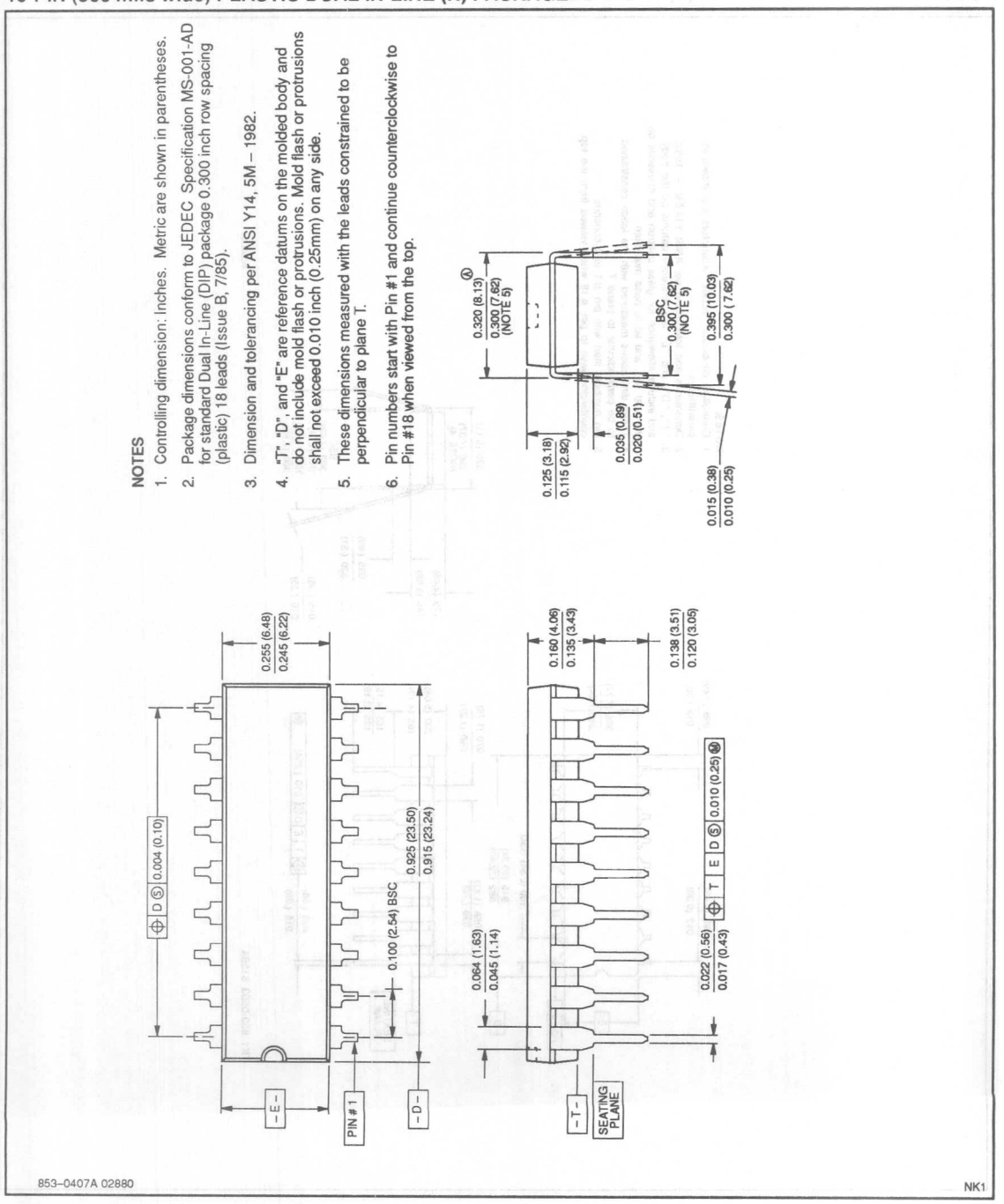
Package outlines

16-PIN CERAMIC DUAL IN-LINE (F) PACKAGE



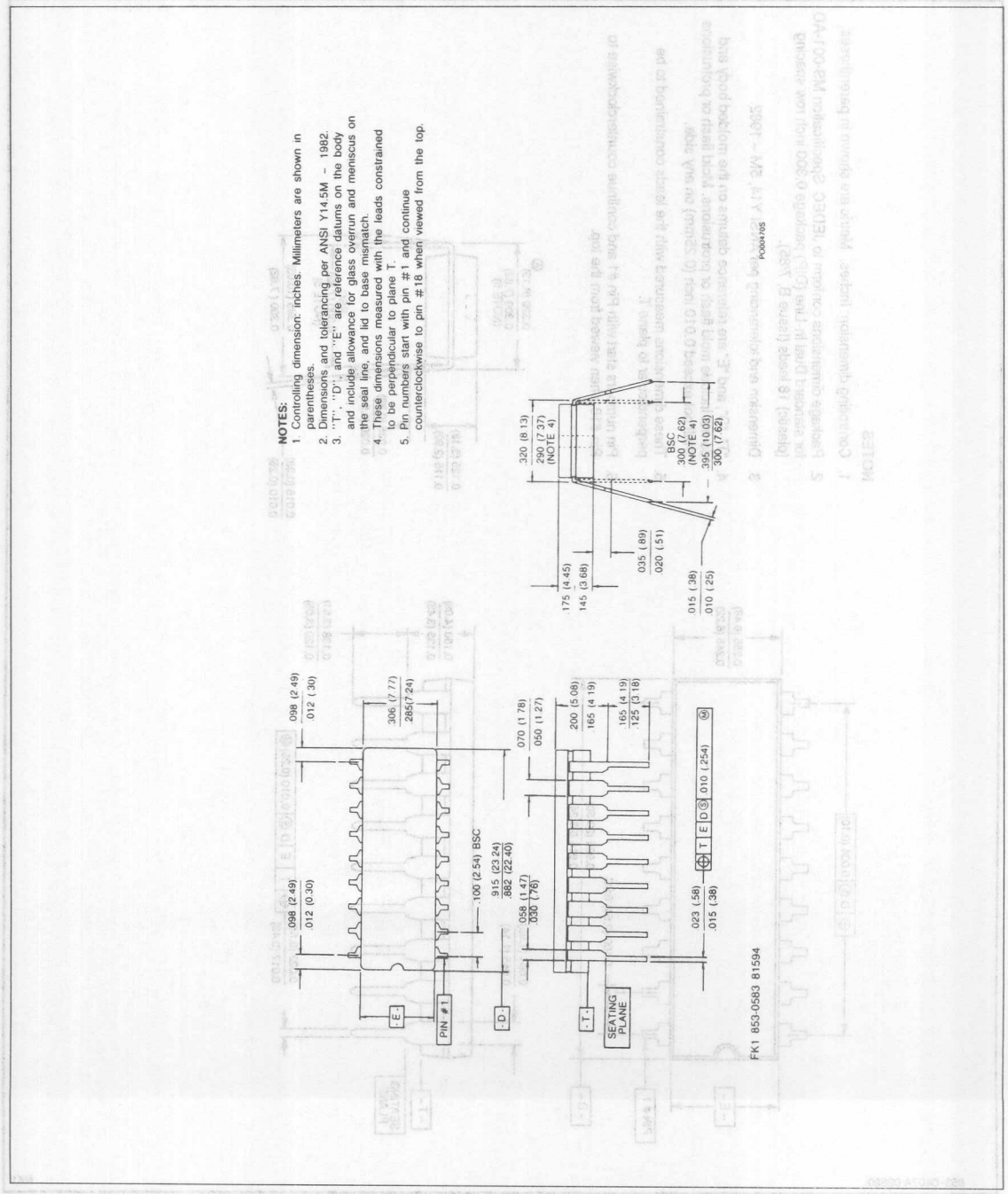
Package outlines

18-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



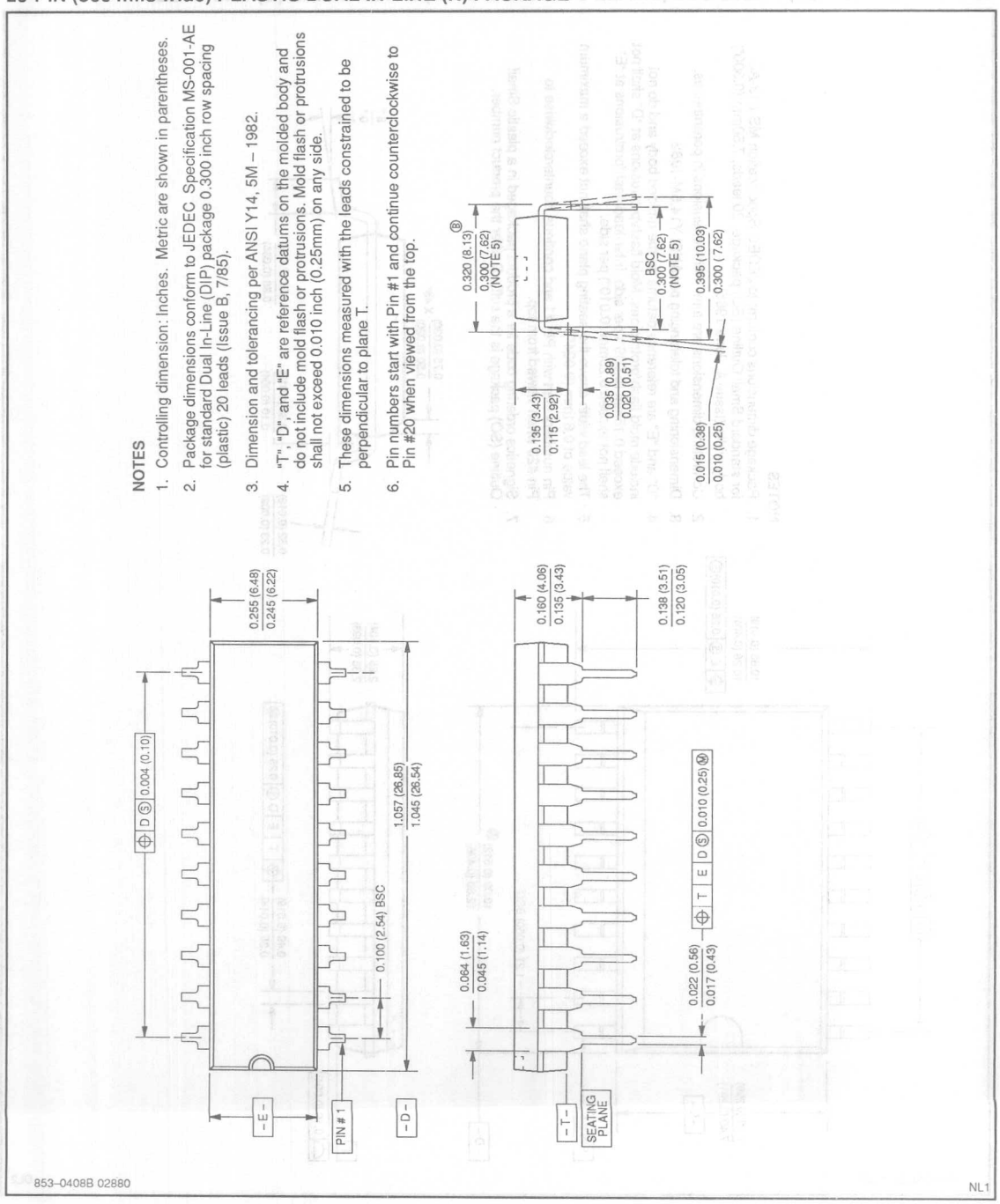
Package outlines

18-PIN CERAMIC DUAL IN-LINE (F) PACKAGE



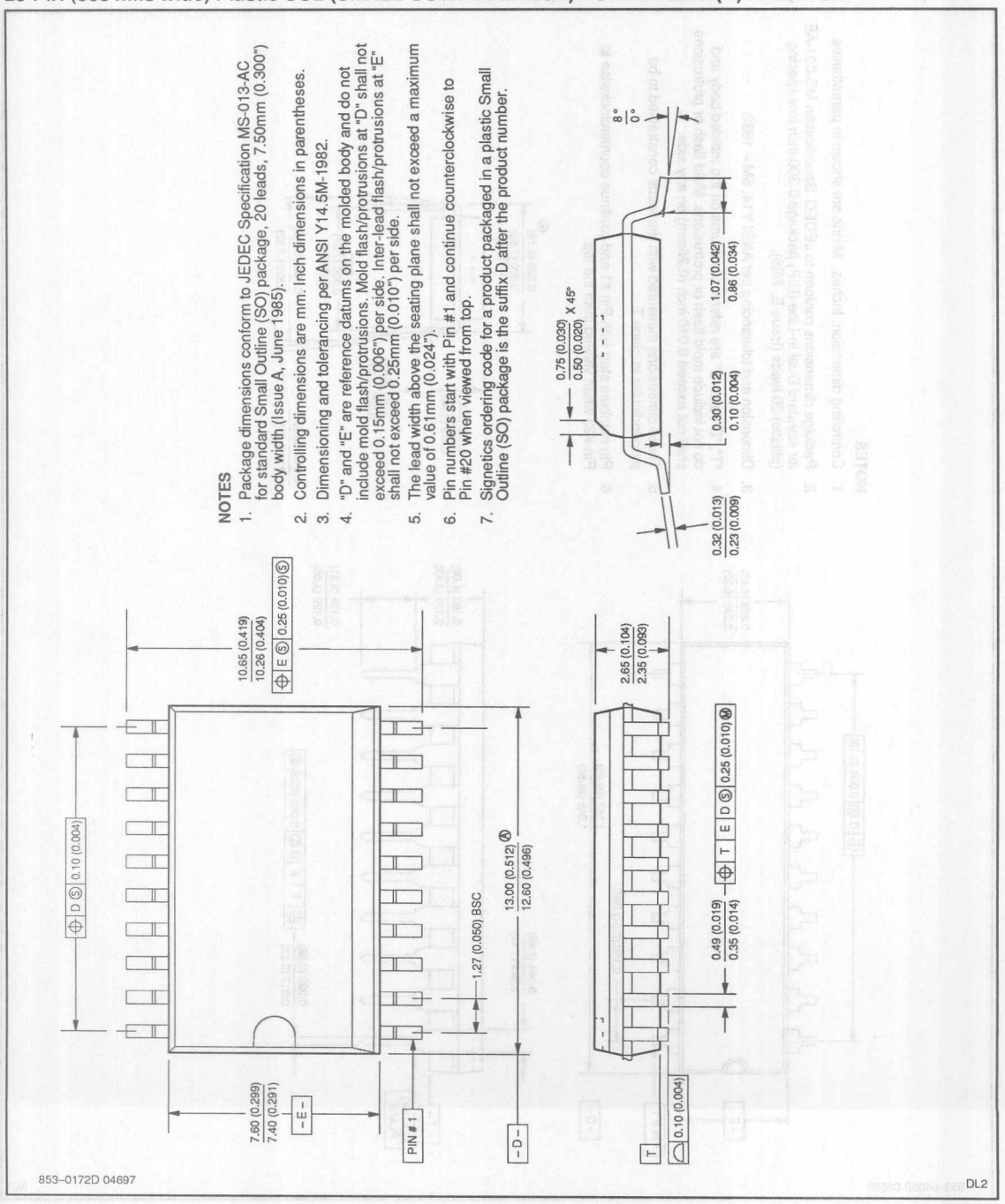
Package outlines

20-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



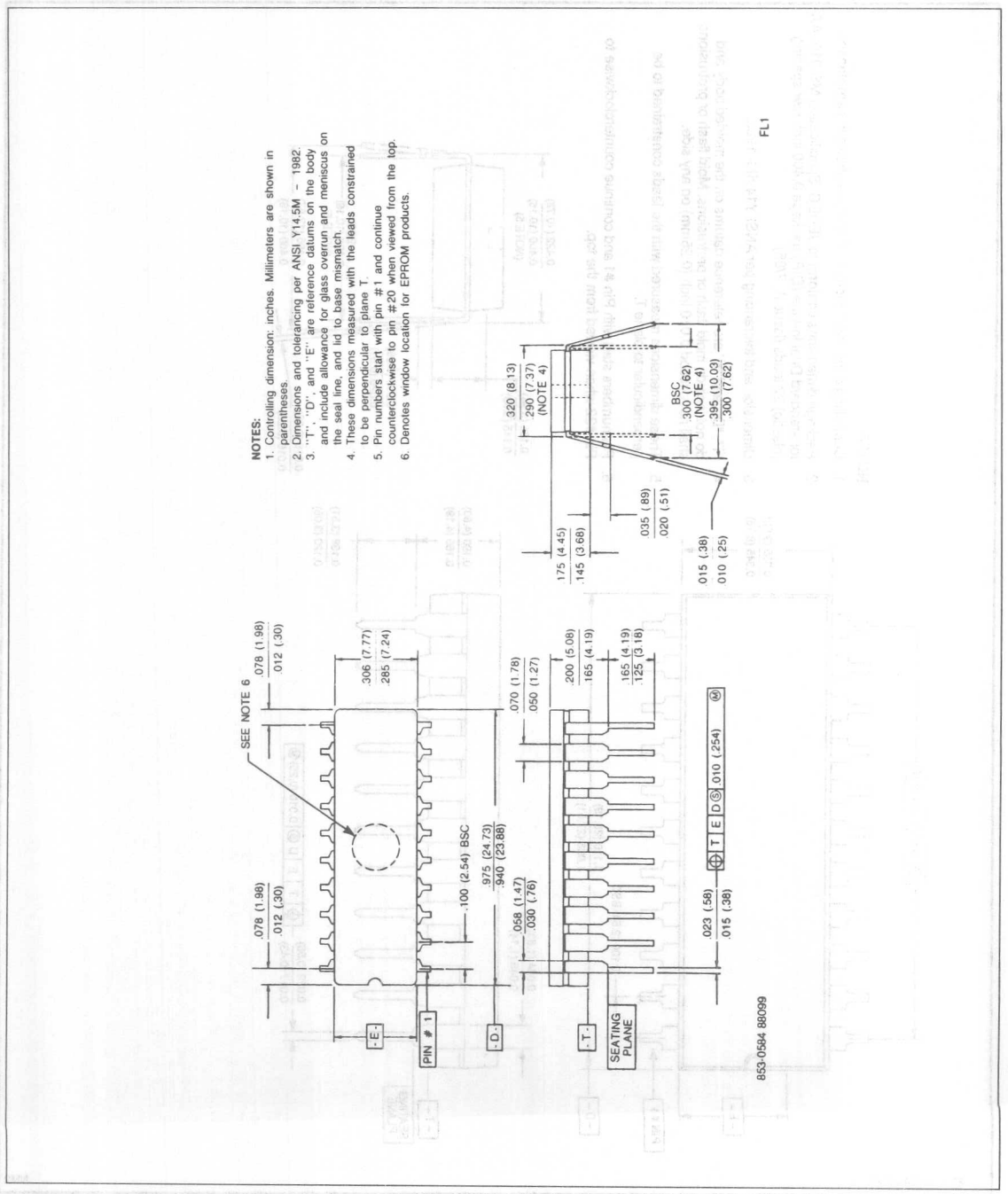
Package outlines

20-PIN (300 mils wide) Plastic SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE

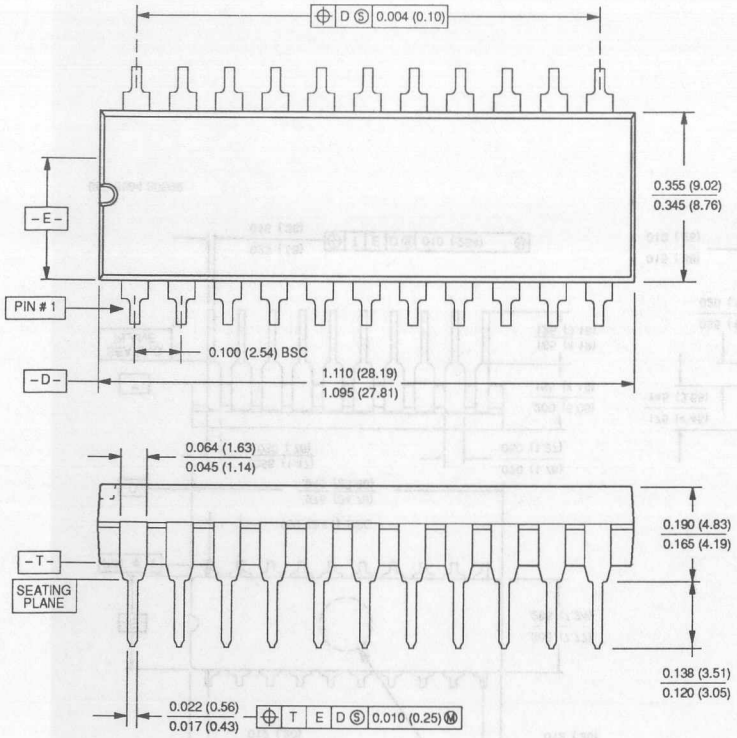


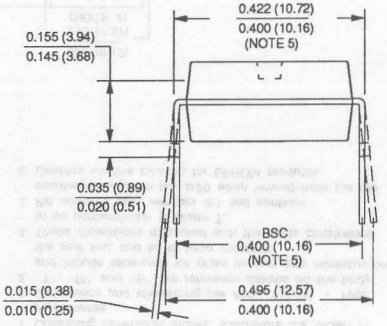
Package outlines

20-PIN CERAMIC DUAL IN-LINE (F) PACKAGE



22-PIN (400 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE





NOTES

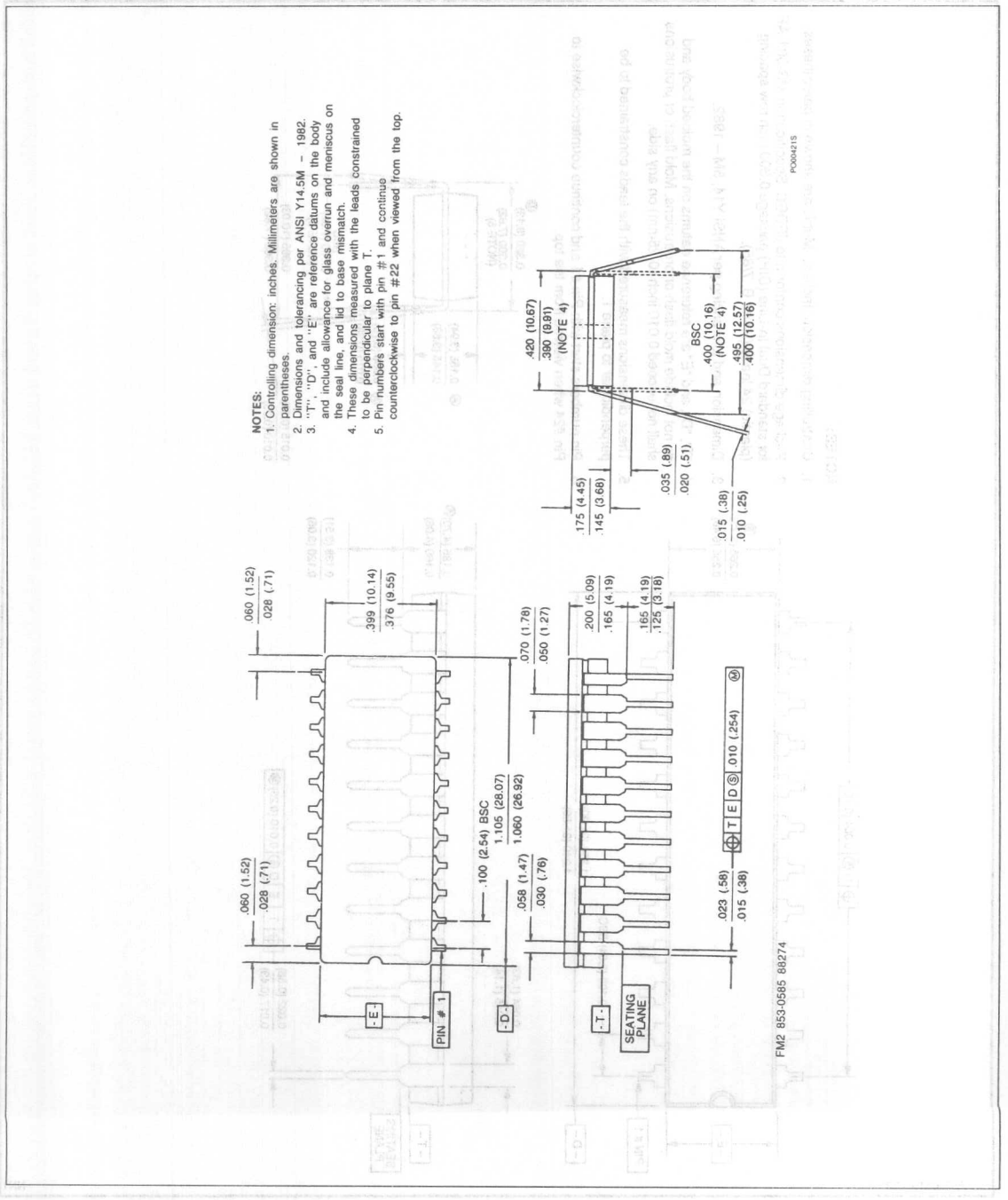
1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-010–AA for standard Dual In-Line (DIP) package 0.400 inch row spacing (plastic) 22 leads (issue A, 7/85).
3. Dimension and tolerancing per ANSI Y14.5M–1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #22 when viewed from the top.

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NM2

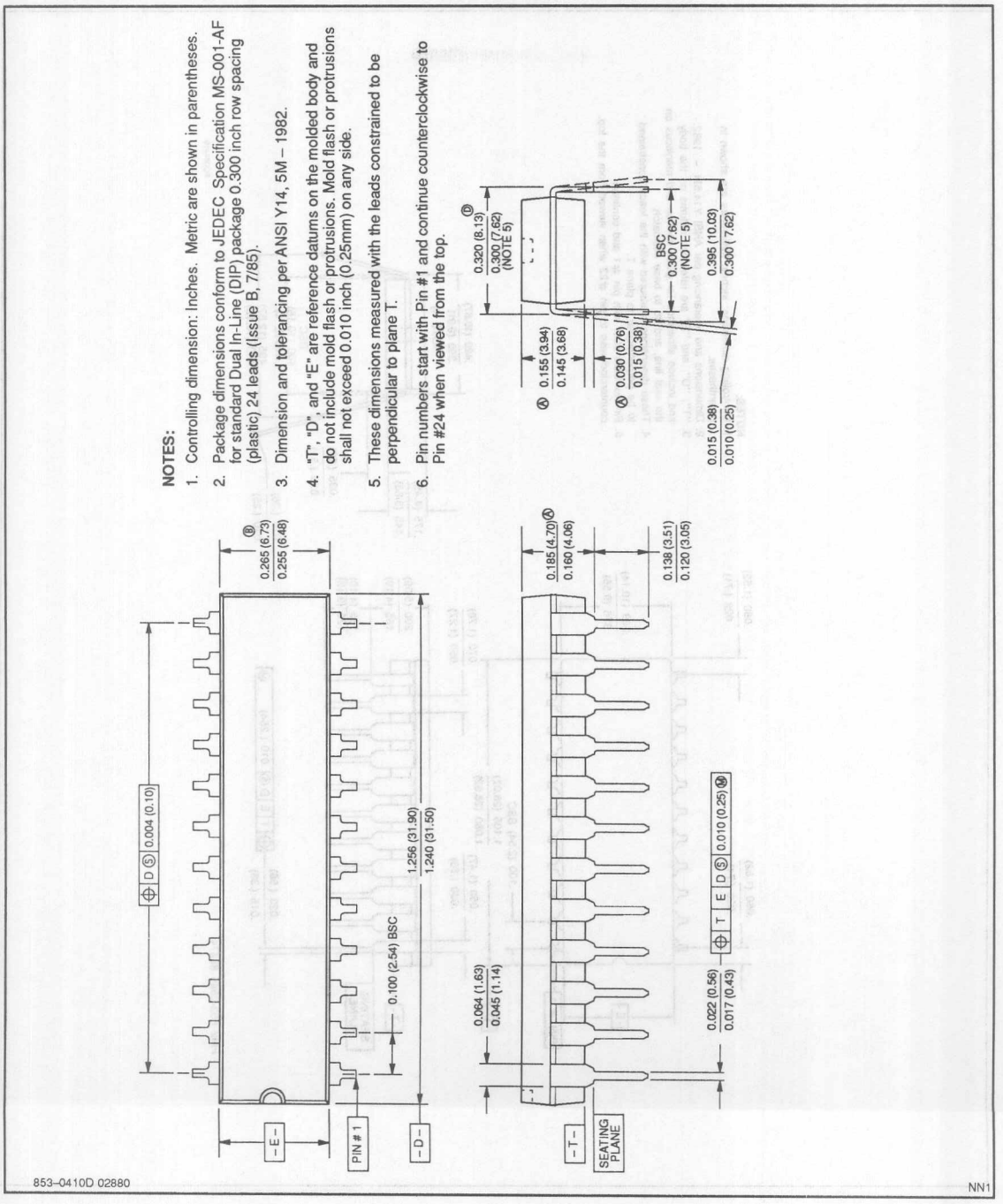
Package outlines

22-PIN CERAMIC DUAL IN-LINE (F) PACKAGE



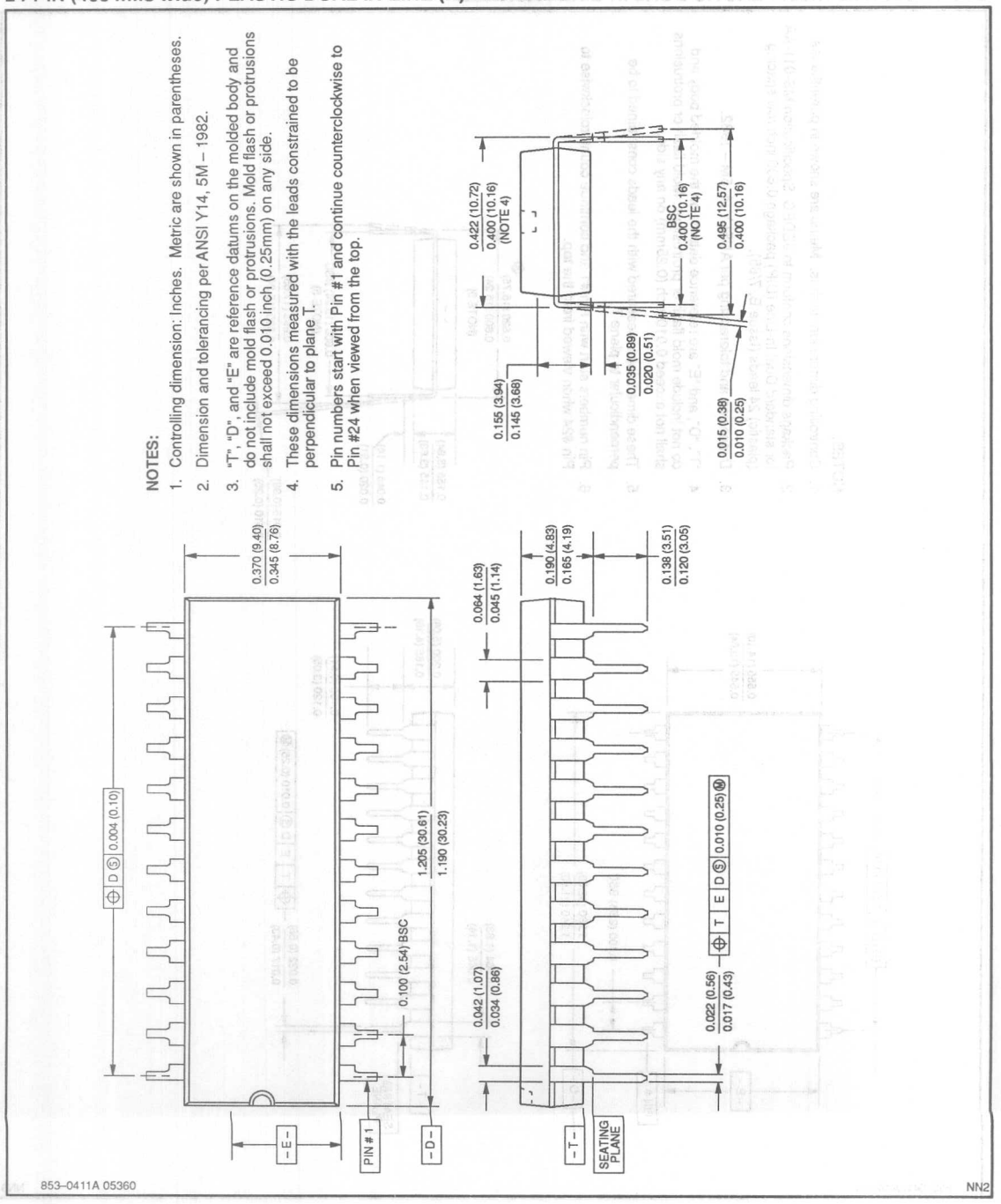
Package outlines

24-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



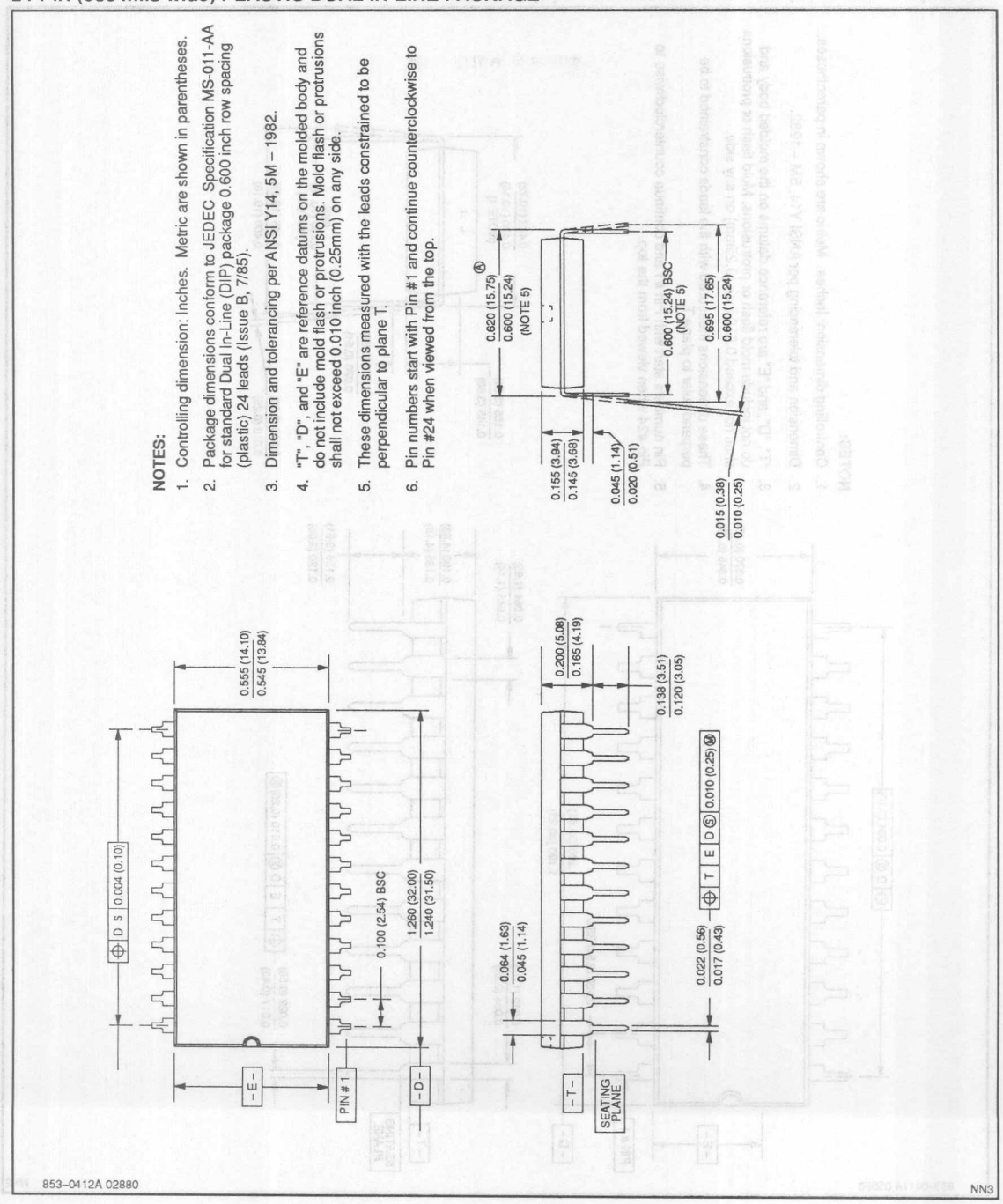
Package outlines

24-PIN (400 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



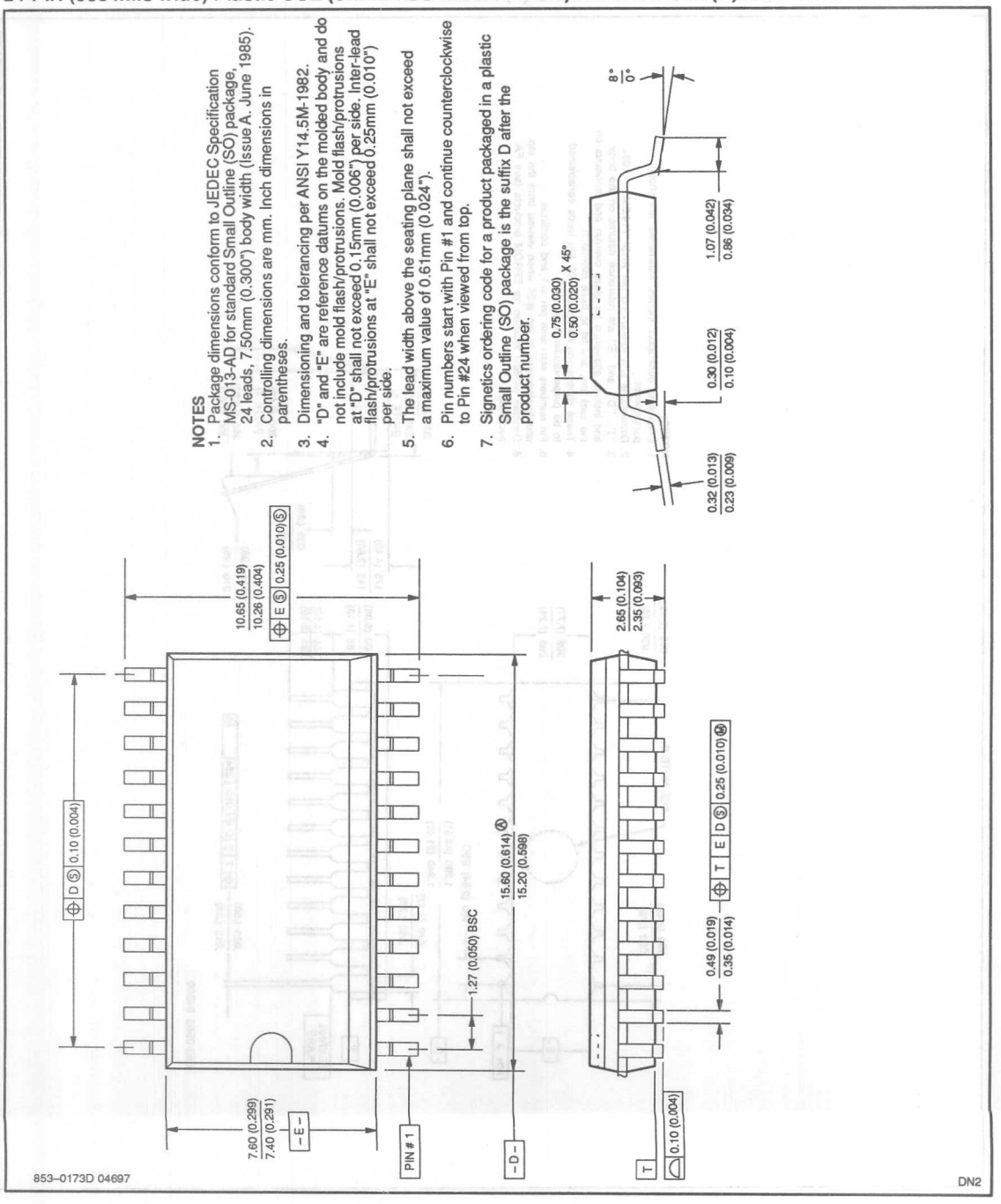
Package outlines

24-PIN (600 mils wide) PLASTIC DUAL IN-LINE PACKAGE



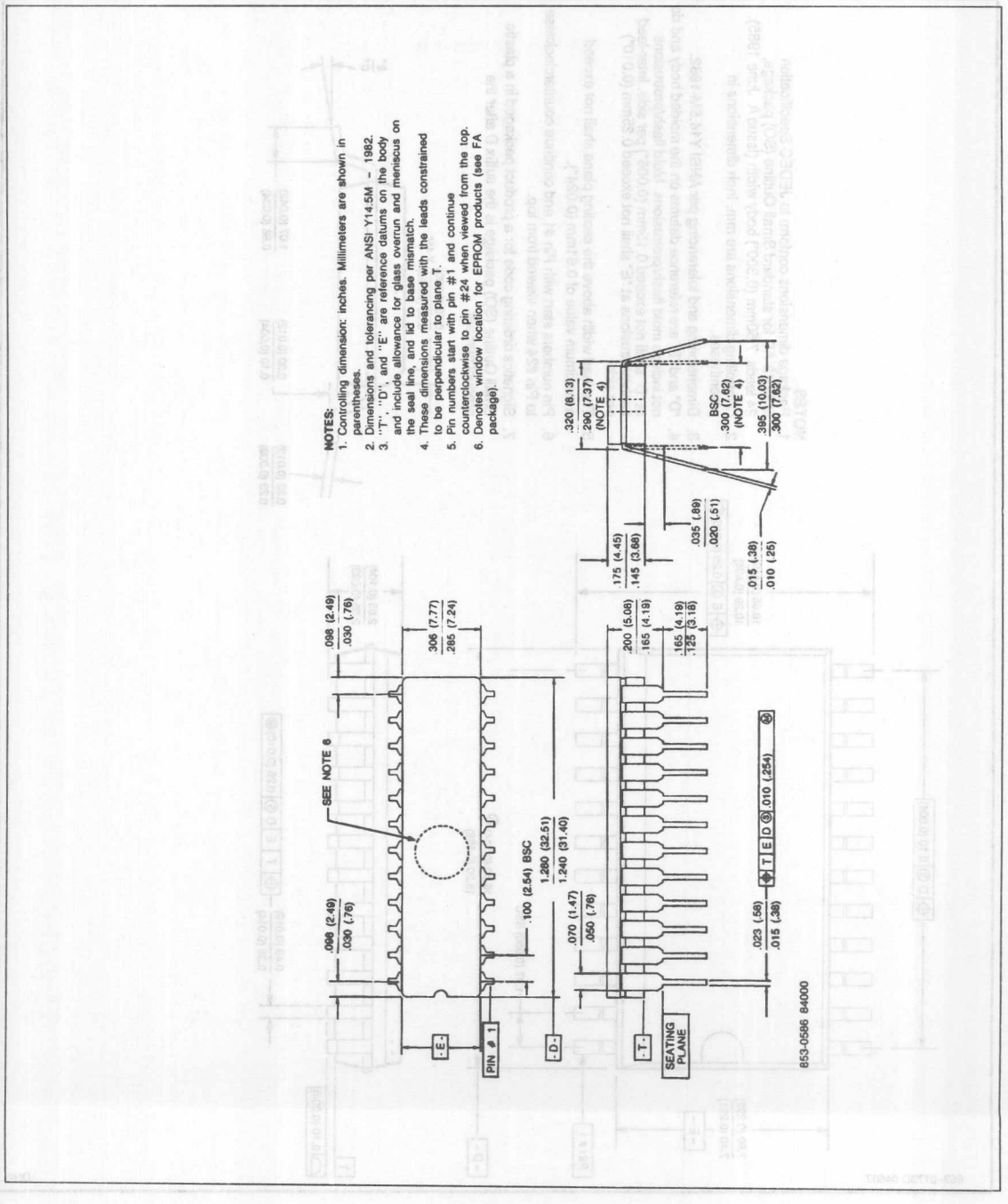
Package outlines

24-PIN (300 mils wide) Plastic SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



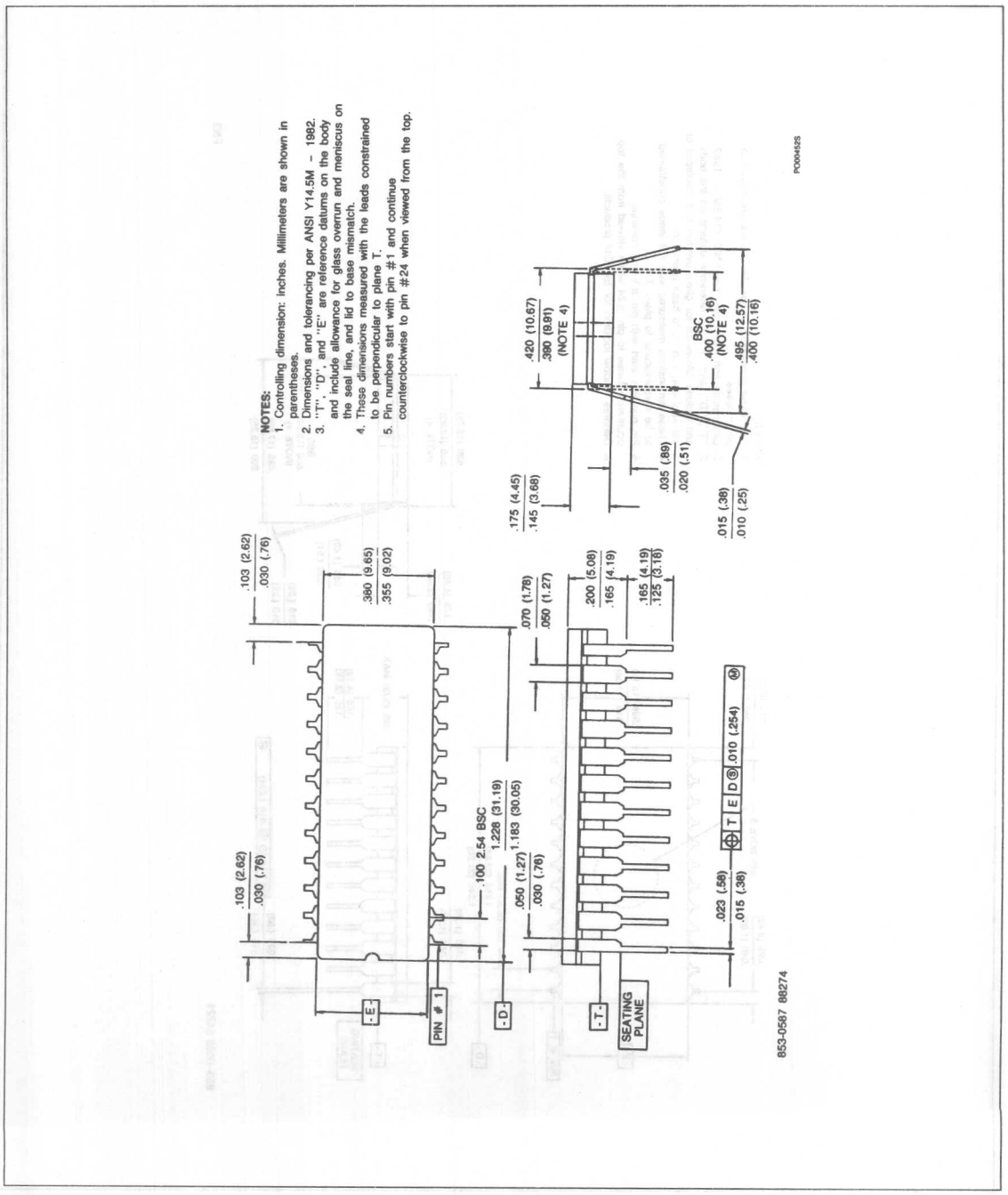
Package outlines

24-PIN (300 MILS WIDE) CERAMIC DUAL IN-LINE (F) PACKAGE



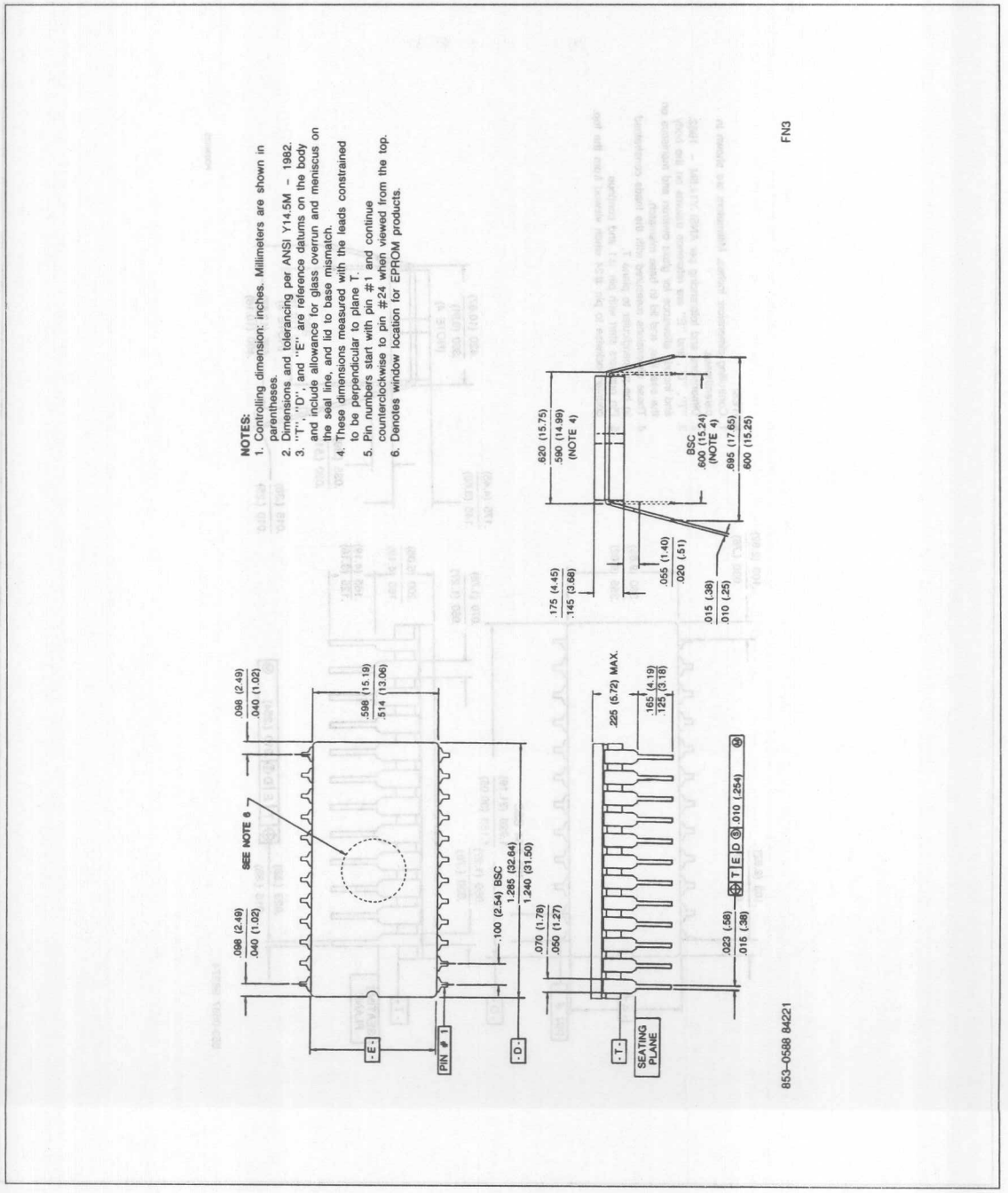
Package outlines

24-PIN (400 MILS WIDE) CERAMIC DUAL IN-LINE (F) PACKAGE



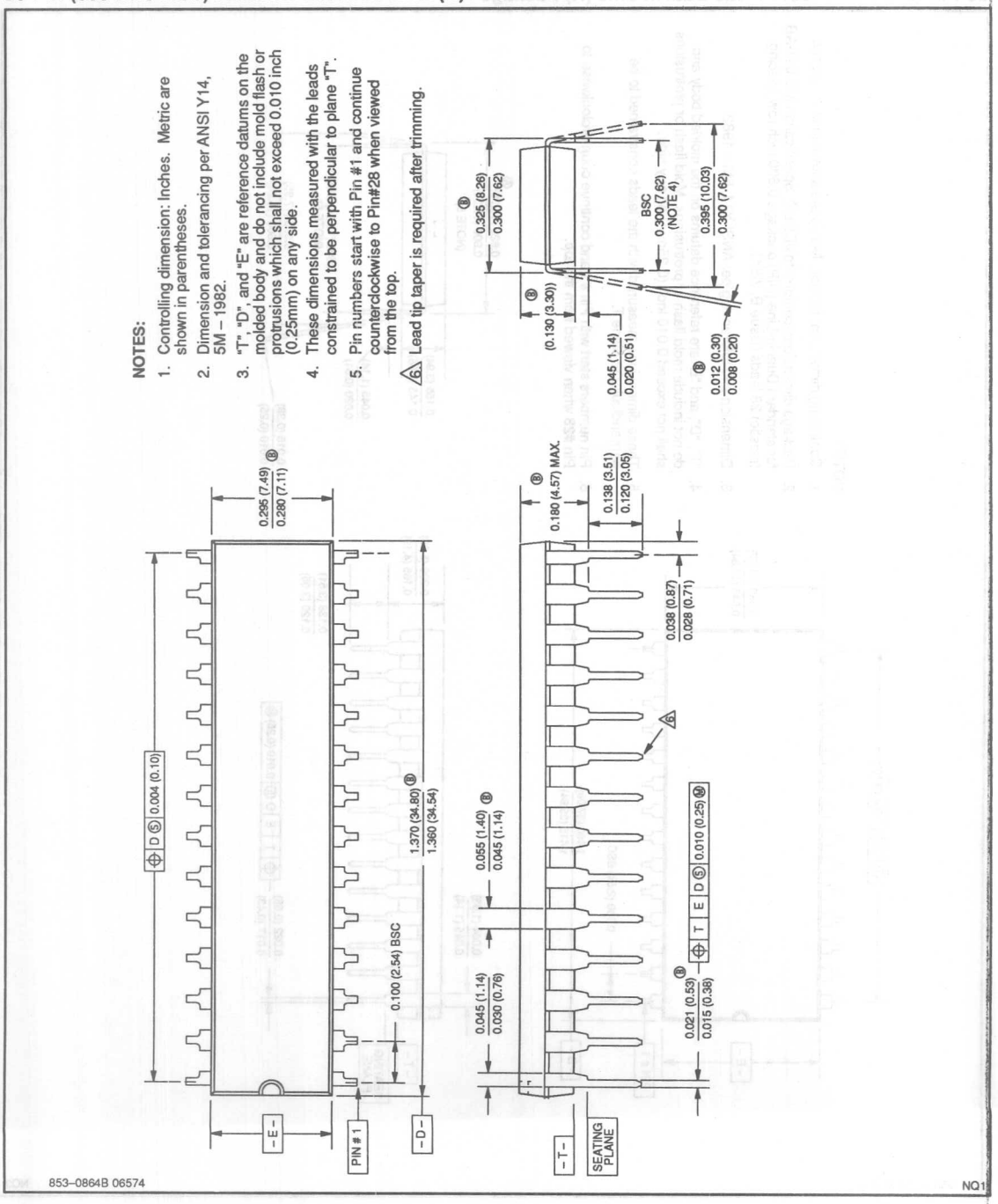
Package outlines

24-PIN (600 MILS WIDE) CERAMIC DUAL IN-LINE (F) PACKAGE



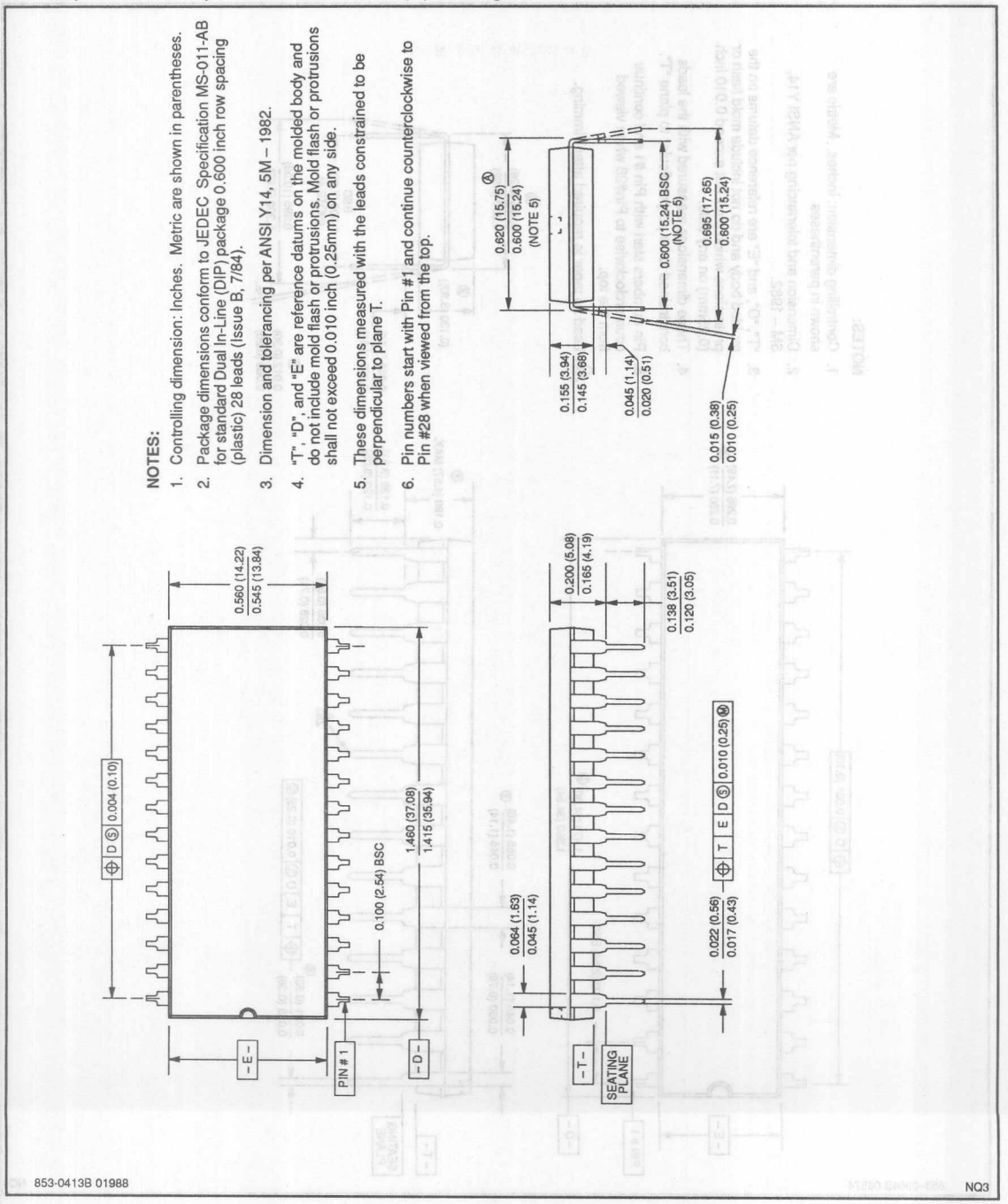
Package outlines

28-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



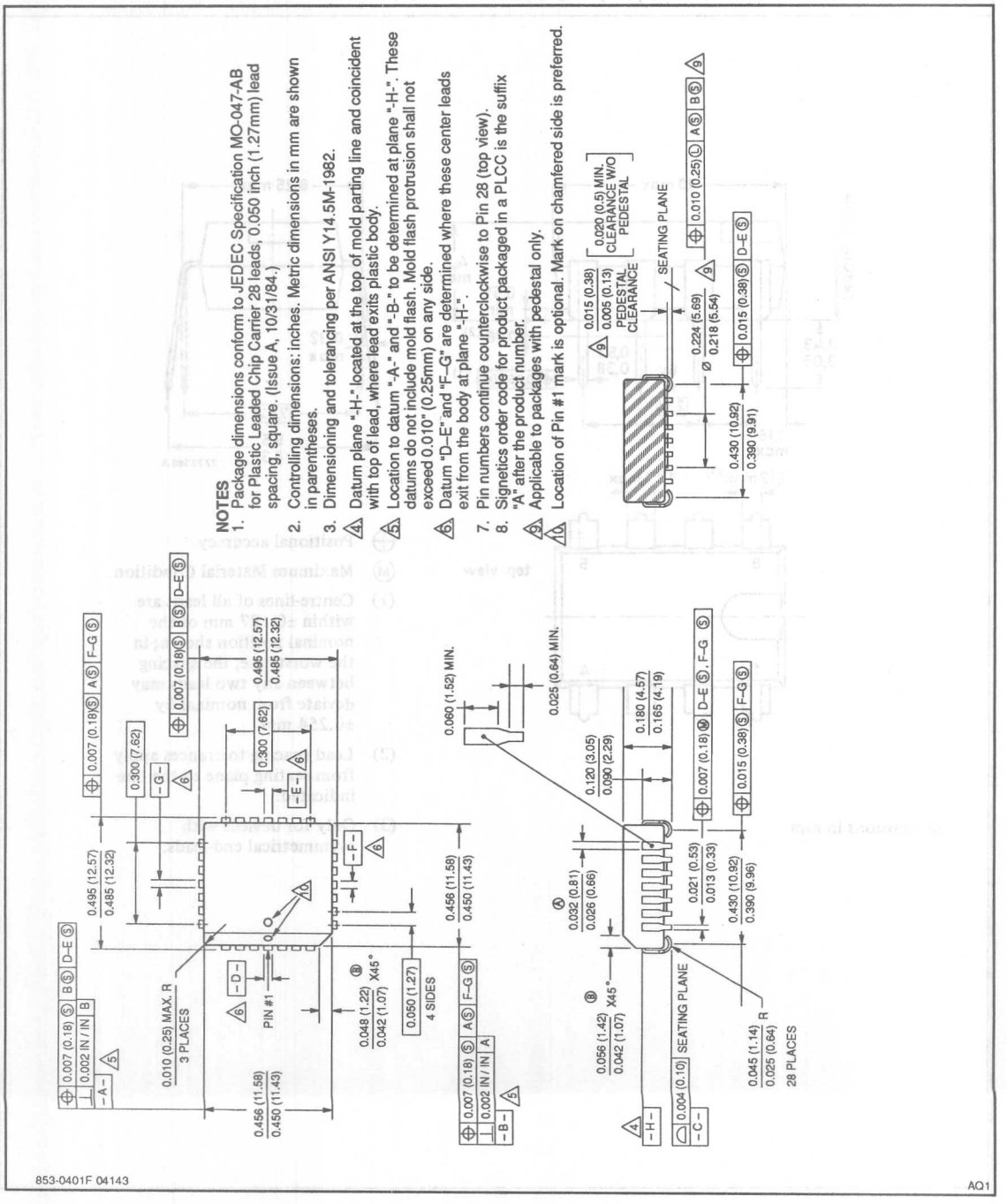
Package outlines

28-PIN (600 mils wide) Plastic Dual In-Line (N) Package



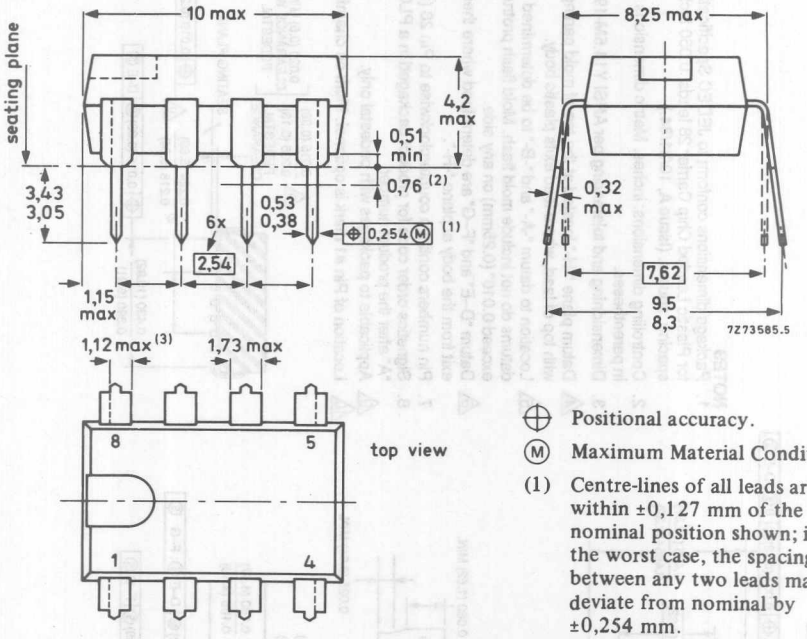
Package outlines

28-PIN PLASTIC LEADED CHIP CARRIER (A) PACKAGE



Package outlines

SOT97 8-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

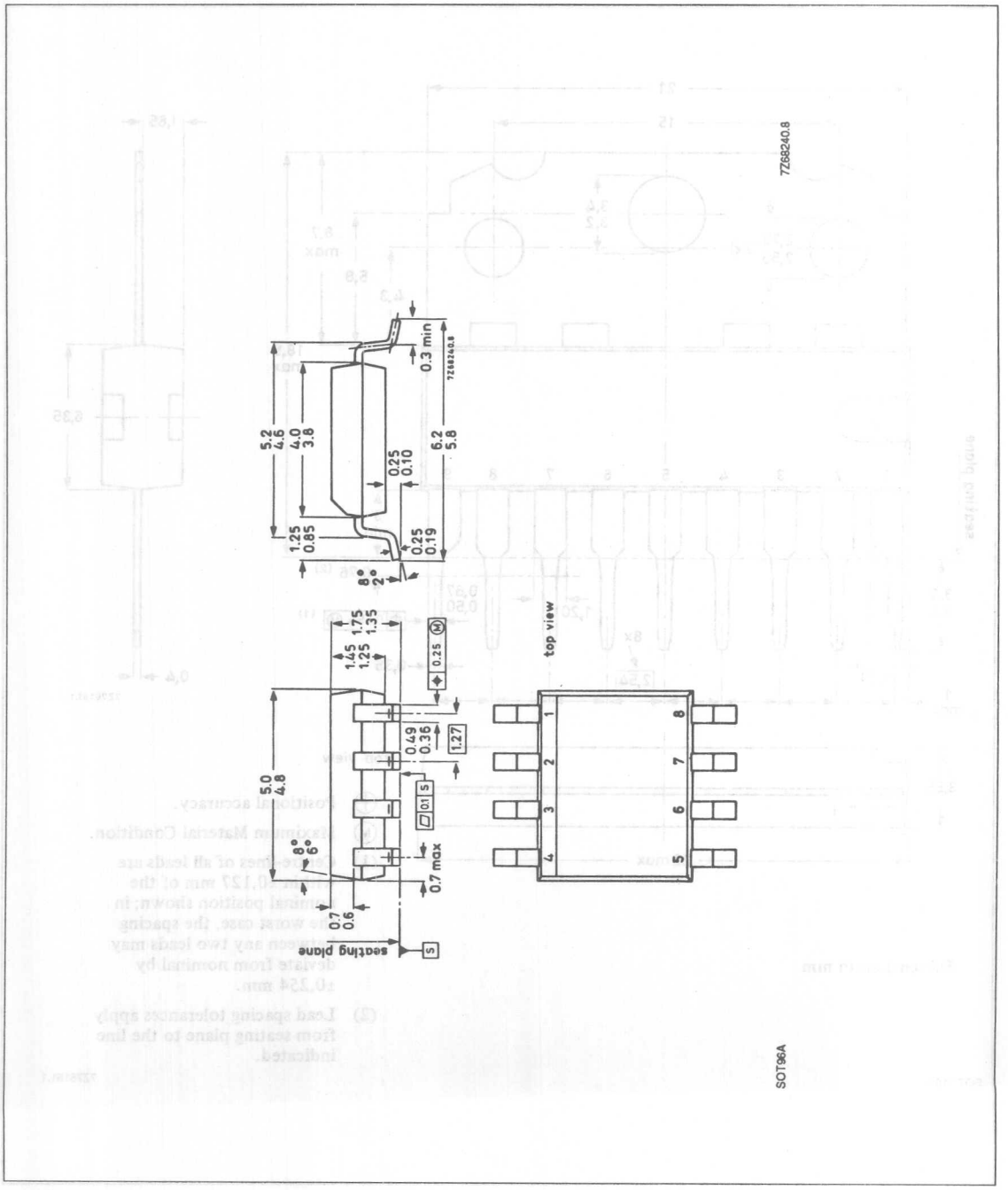
(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

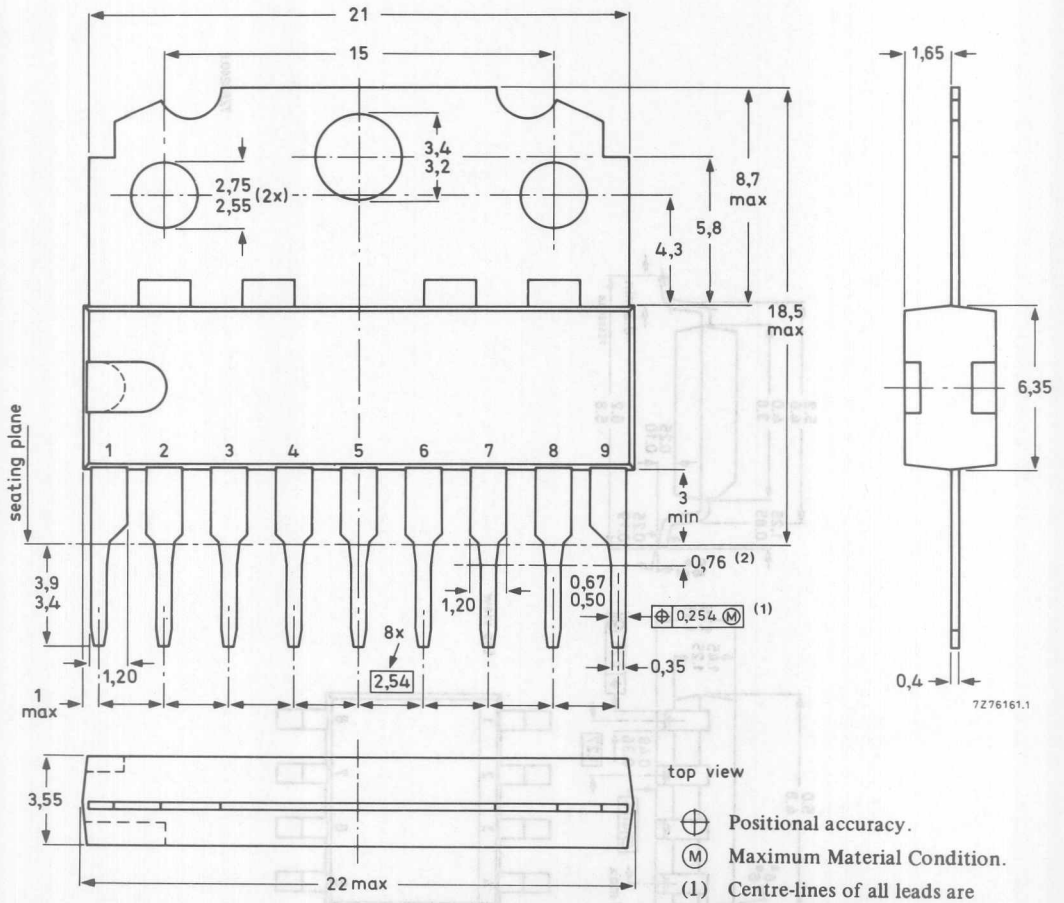
Package outlines

SOT96A 8-PIN PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D/T) PACKAGE



Package outlines

SOT110B 9-PIN PLASTIC SINGLE IN-LINE (U) PACKAGE



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

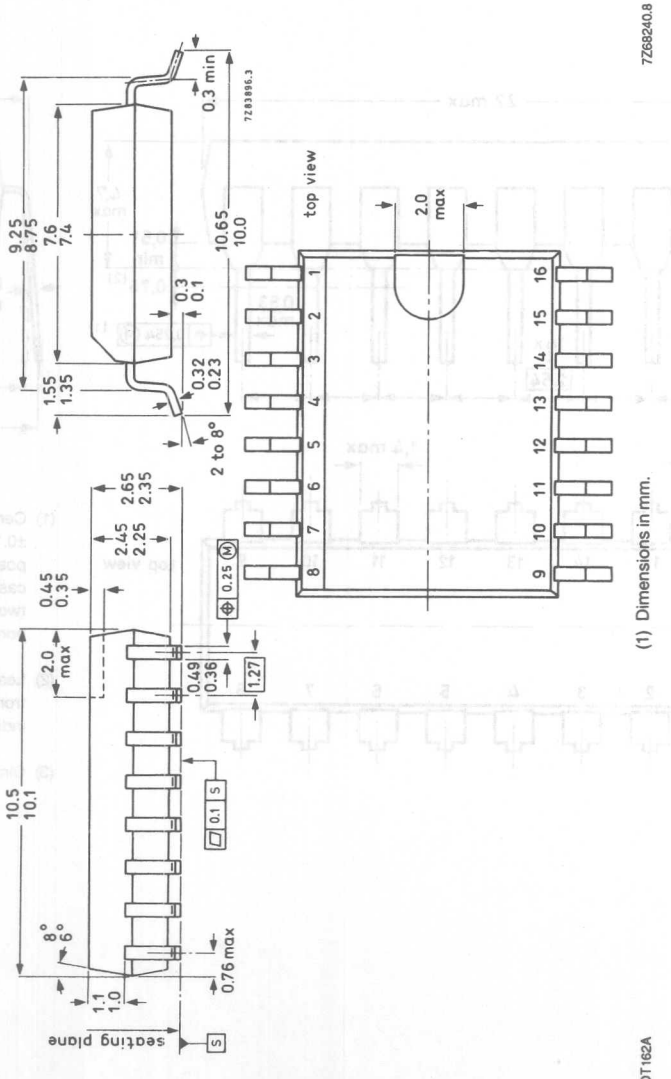
Dimensions in mm

SOT 110B

7Z76161.1

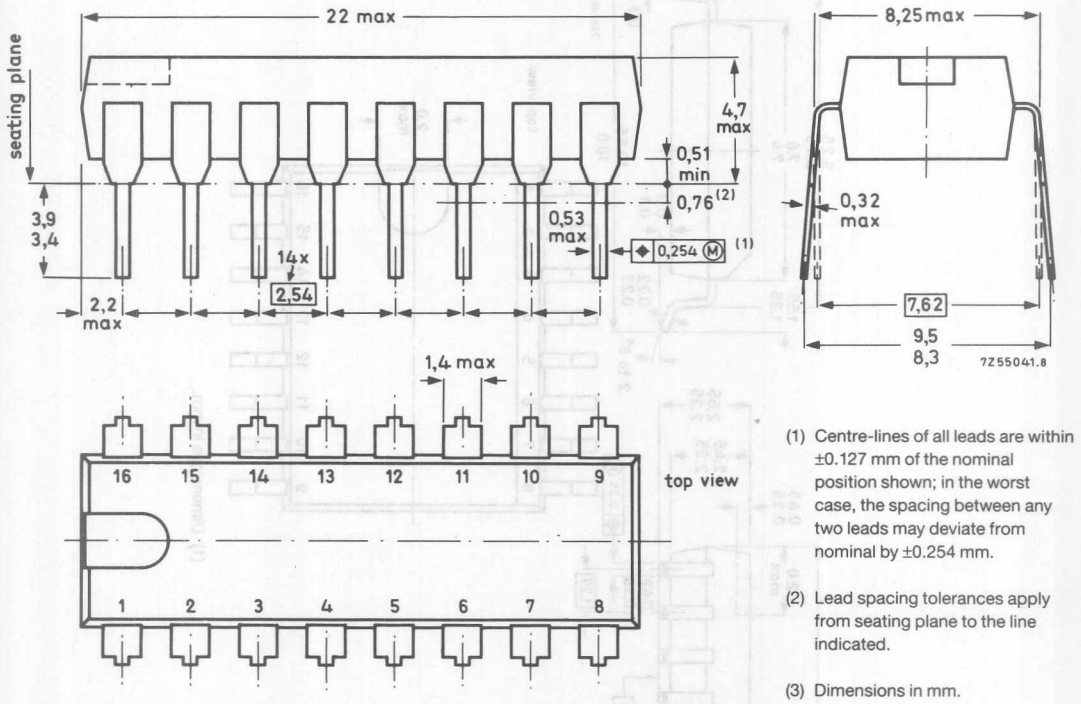
Package outlines

SOT162A 16-PIN PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D/T) PACKAGE



Package outlines

SOT38 16-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE



(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

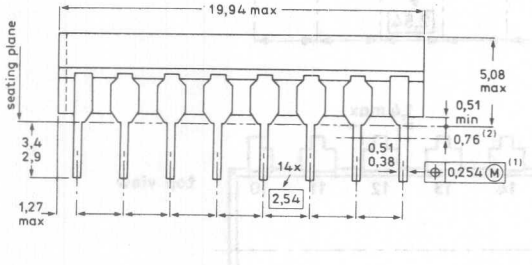
(3) Dimensions in mm.

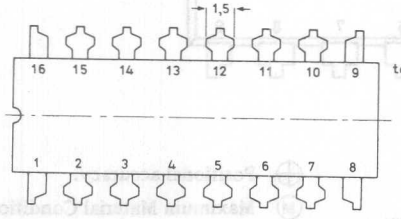
SOT 38

7Z55041.8

Package outlines

SOT74 16-PIN CERAMIC DUAL IN-LINE (F) PACKAGE





Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

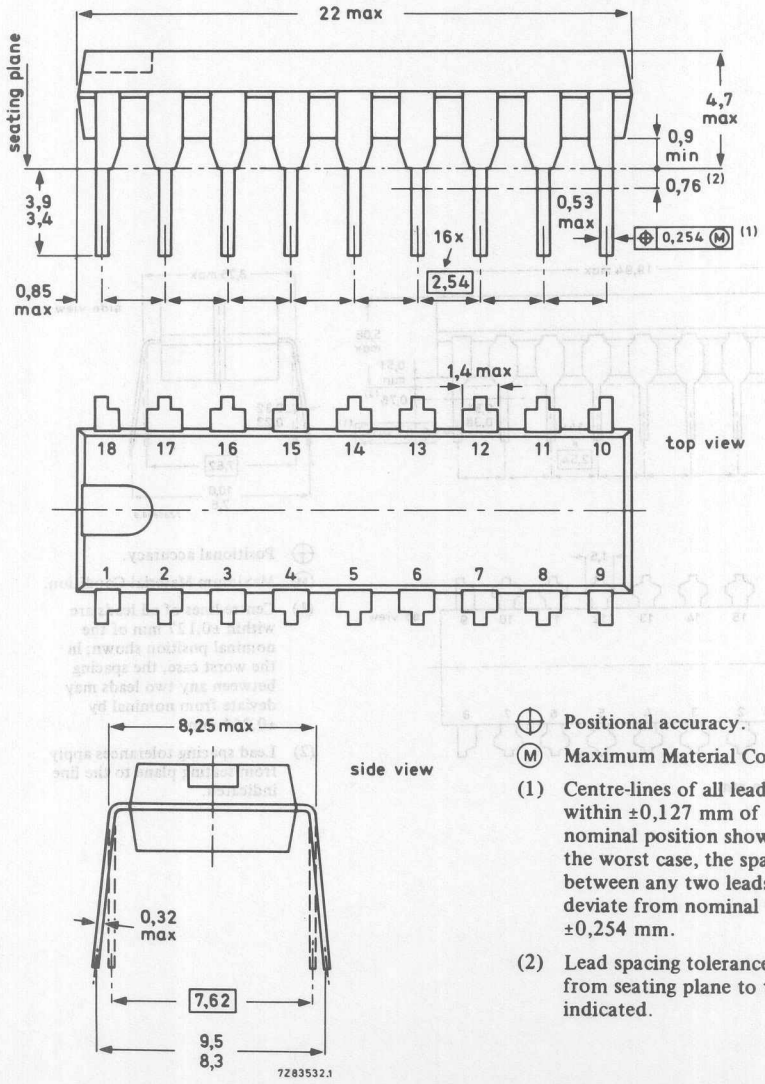
(2) Lead spacing tolerances apply from seating plane to the line indicated.

SOT74

7Z55544.9

Package outlines

SOT102 18-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE WITH INTERNAL HEATSPREADER



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

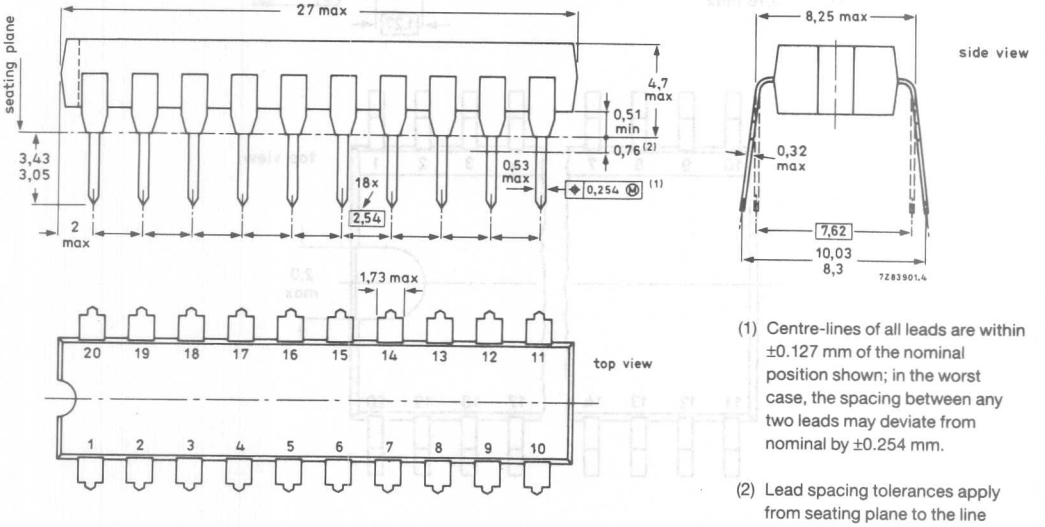
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Package outlines

SOT146 20-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE



(1) Centre-lines of all leads are within ±0.127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0.254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

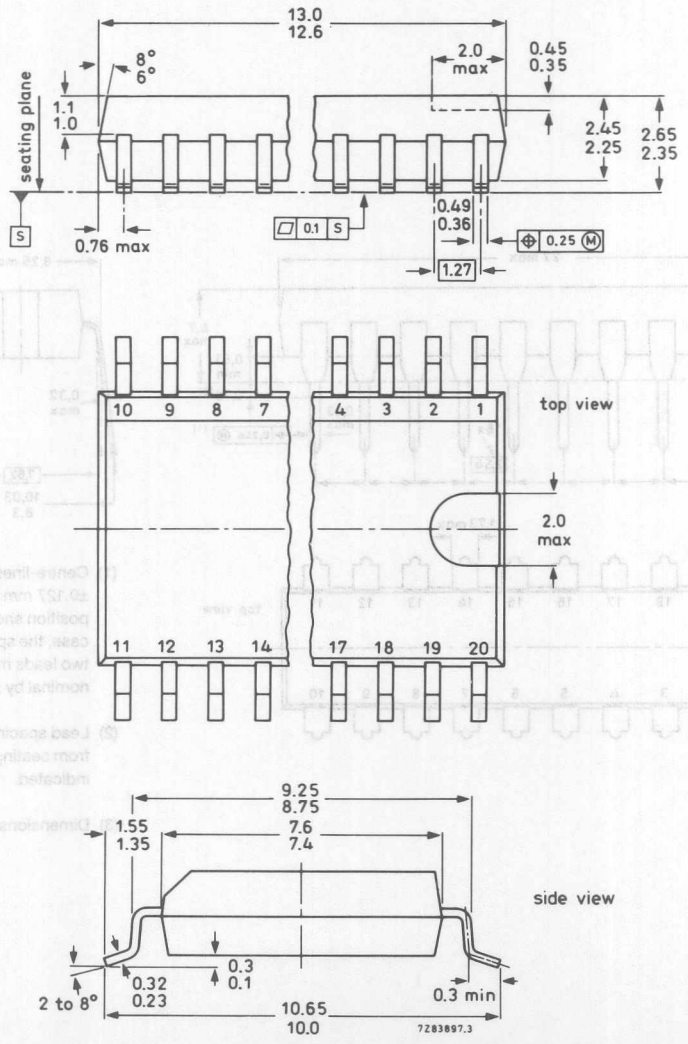
(3) Dimensions in mm.

SOT 146

7Z83901.4

Package outlines

SOT163A 20-PIN SO (SMALL OUTLINE) PLASTIC DUAL IN-LINE (D/T) PACKAGE



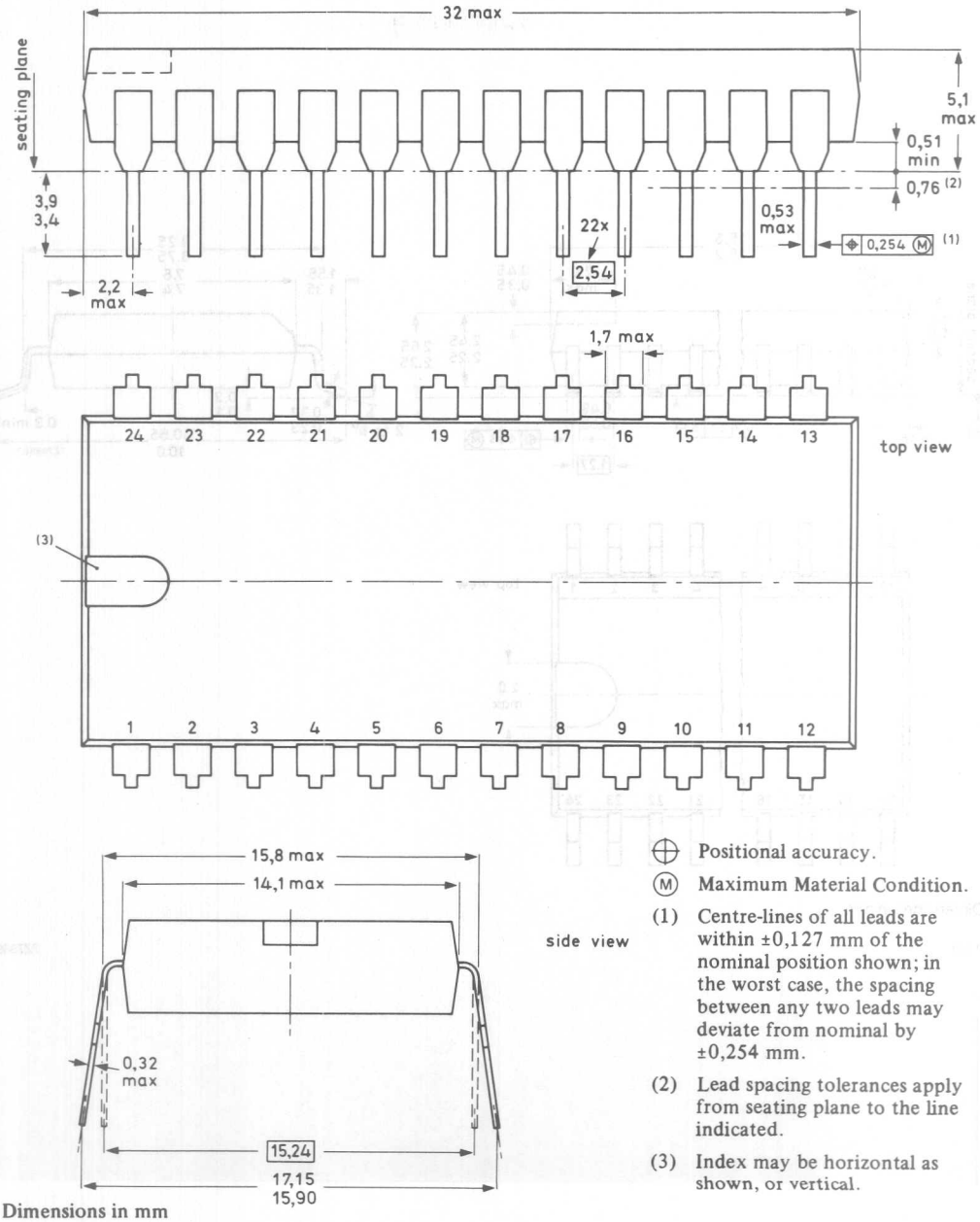
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

Package outlines

SOT101 24-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE WITH INTERNAL HEATSPREADER



Dimensions in mm

SOT101A, B, F, G, L

7Z73670.5

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

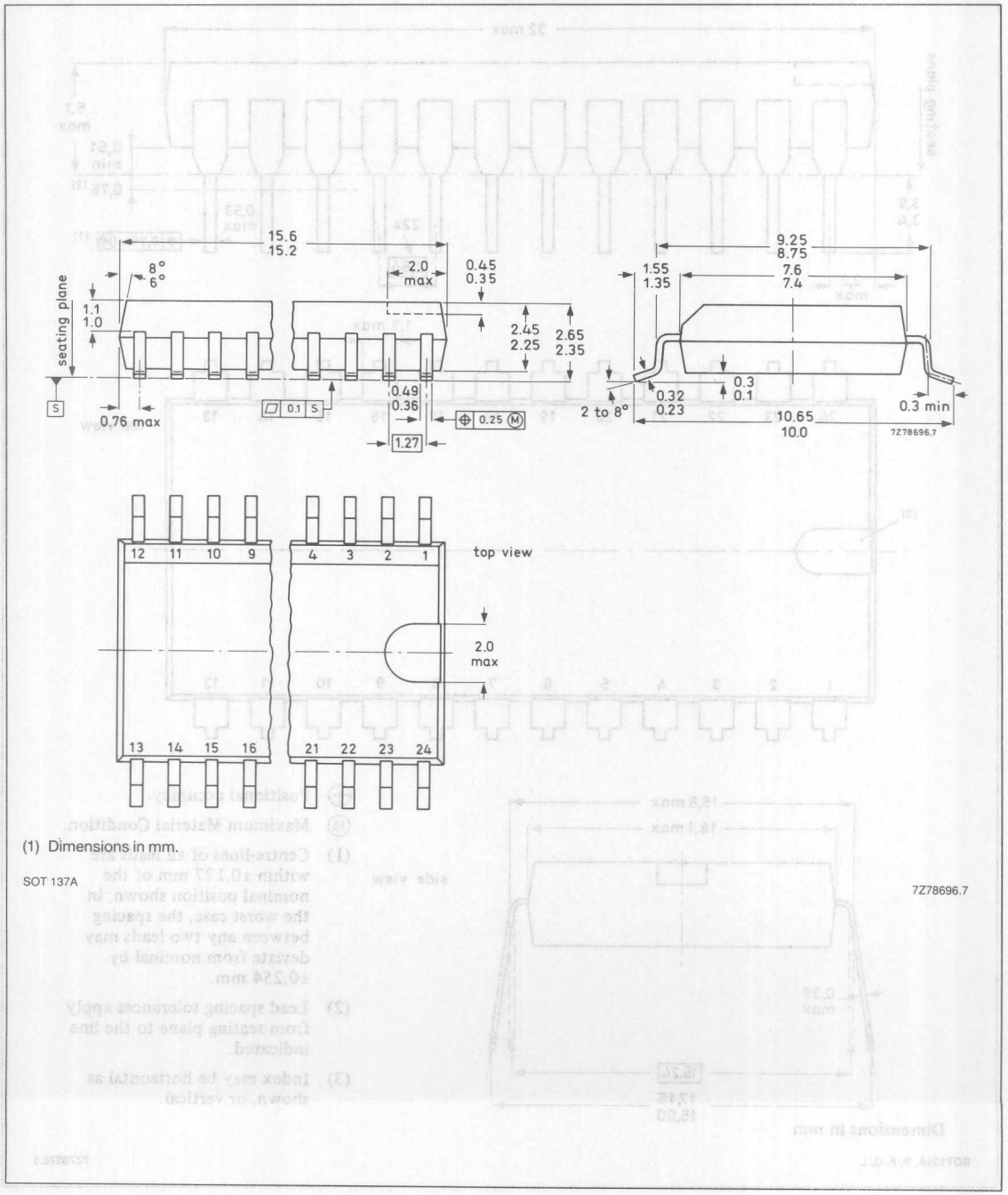
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Package outlines

SOT137A 24-PIN PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D/T) PACKAGE



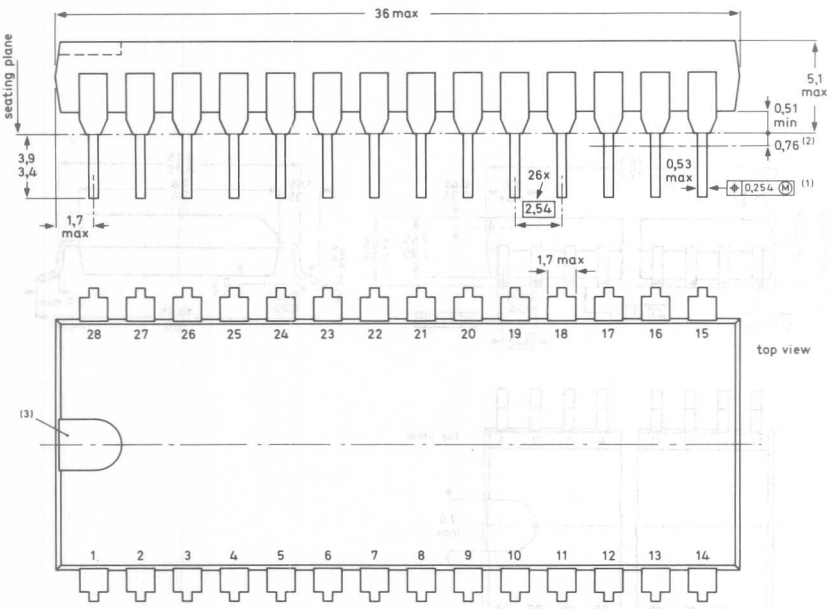
(1) Dimensions in mm.

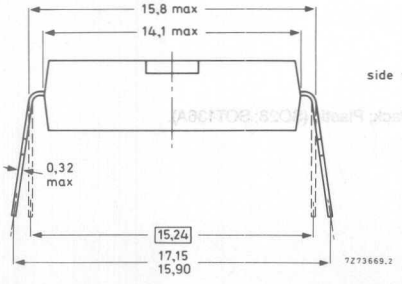
SOT 137A

7Z78696.7

Package outlines

SOT117 28-PIN PLASTIC DUAL IN-LINE (N/P) PACKAGE





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

Package outlines

SOT136A 28-PIN PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (N/P) PACKAGE

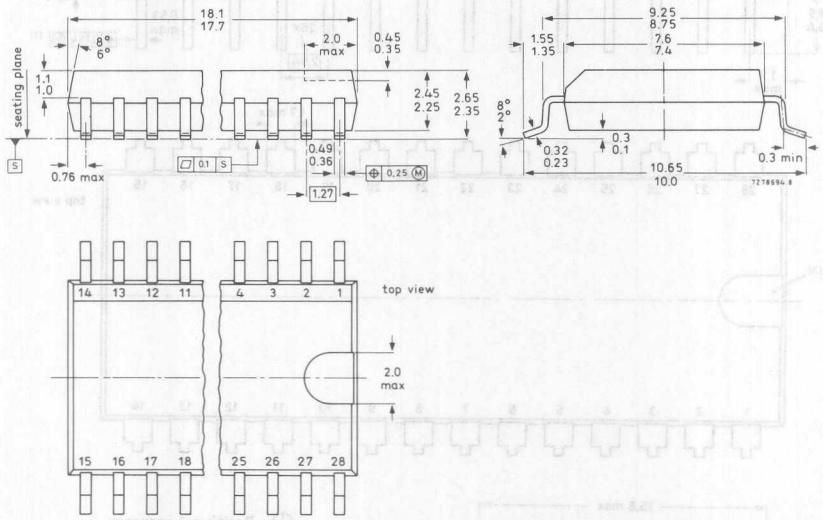
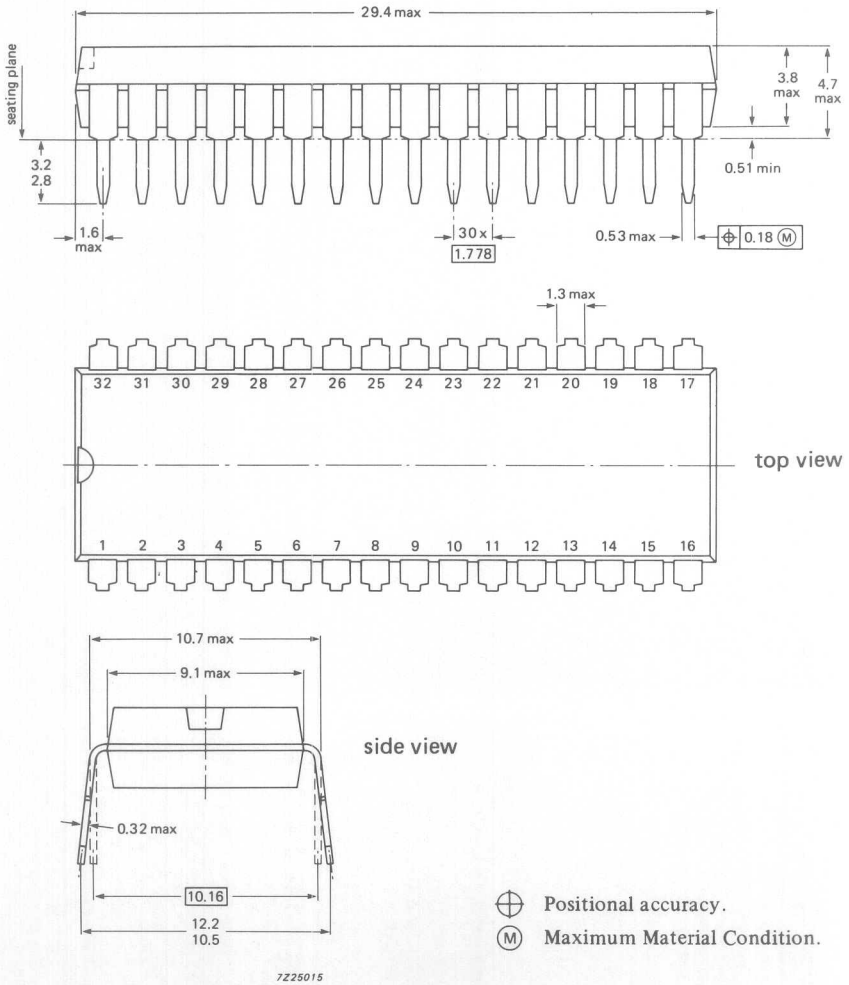


Fig.13.2 28-Lead Mini-Pack; Plastic (SO28; SOT136A).

SOT232 32-PIN PLASTIC SHRINK DUAL IN-LINE (N/P) PACKAGE



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm